AstroPix Status Update

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On behalf of the AstroPix team
NASA GSFC, NPP/ORAU

12 April 2024
ePIC BIC: Virtual Mini-Workshop

Status Summary

v3

- Application in larger NASA payloads
- Currently under test - characterization (signal, depletion)
- Single-chip and quad-chip testing
- Future testing in beamline

v4

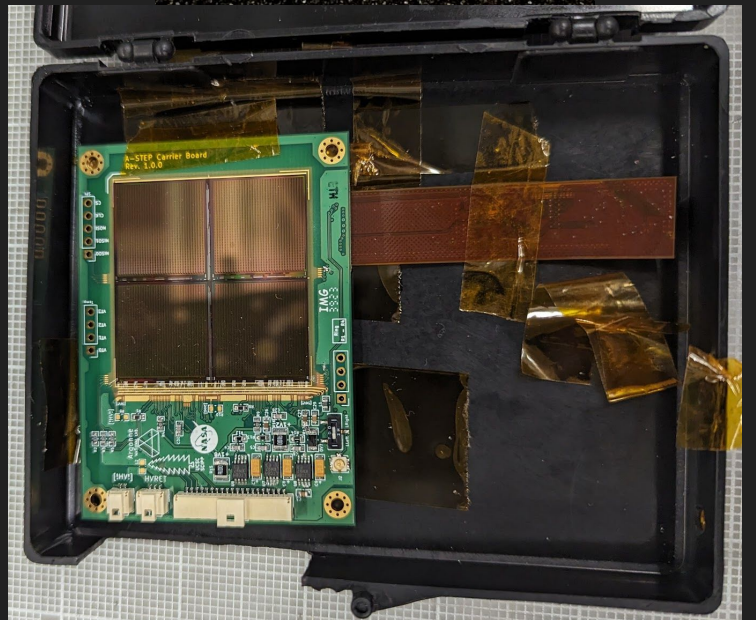
- Currently under test - operation

v5

- In design stage
- Definition of requirements
- For use in BIC

AstroPix_v3

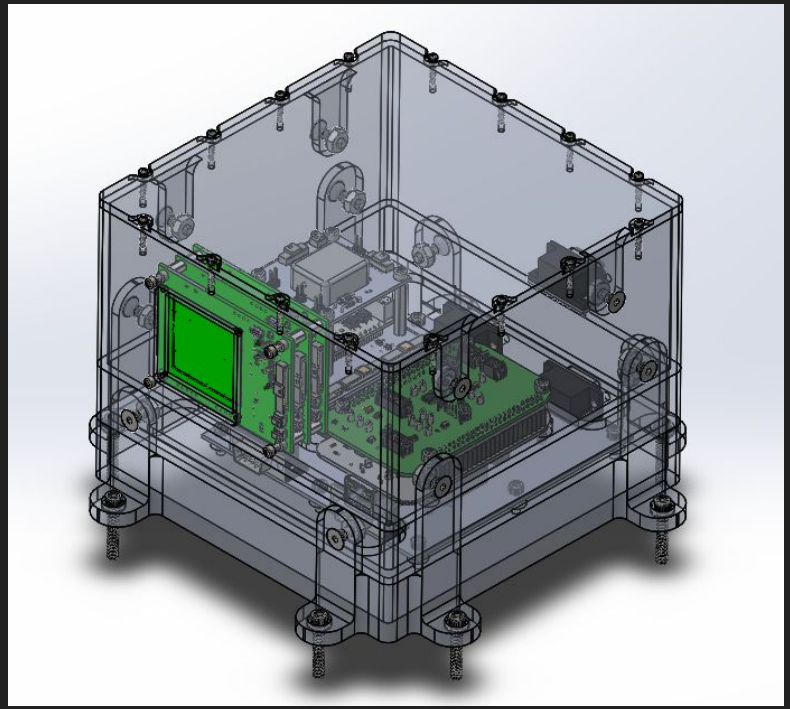
- Characterization testing on 3+ global benches
- Operational testing on 3+ global benches
- 3 wafer resistivities - 20, 300, 25k Ω*cm
- “Quad-chip” (bottom) = 4 daisy-chained arrays on one SPI bus
  - Only bottom two chips currently accessible
- 500 x 500 μm^2 pixel pitch, 35 x 35 pixels
  - Full size 2 x 2 cm^2 array
- Power consumption:
  - ~0.9 mW/cm^2 analog
  - 12 mW/array digital
- 25+ wafers at ANL



NASA payloads with v3

- Funded flight opportunities with heritage teams
- Test-bed for AstroPix systems development
  - Scaled FW and SW
  - Mechanical Structures
  - I&T development and testing
  - Robustness of glues, wire bonds, etc
  - Develop selection / test / calibration strategies

A-STEP (sounding rocket flight, 2025)



- 3 quad-chips (12 arrays, 3 SPI busses)
- V3

NASA payloads with v3

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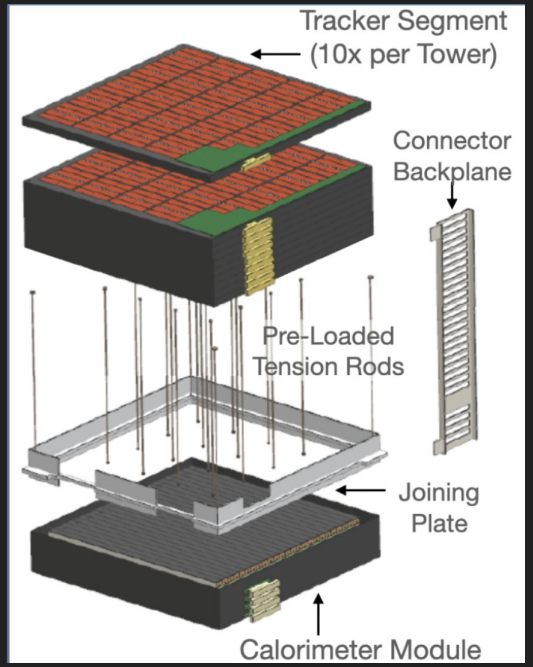
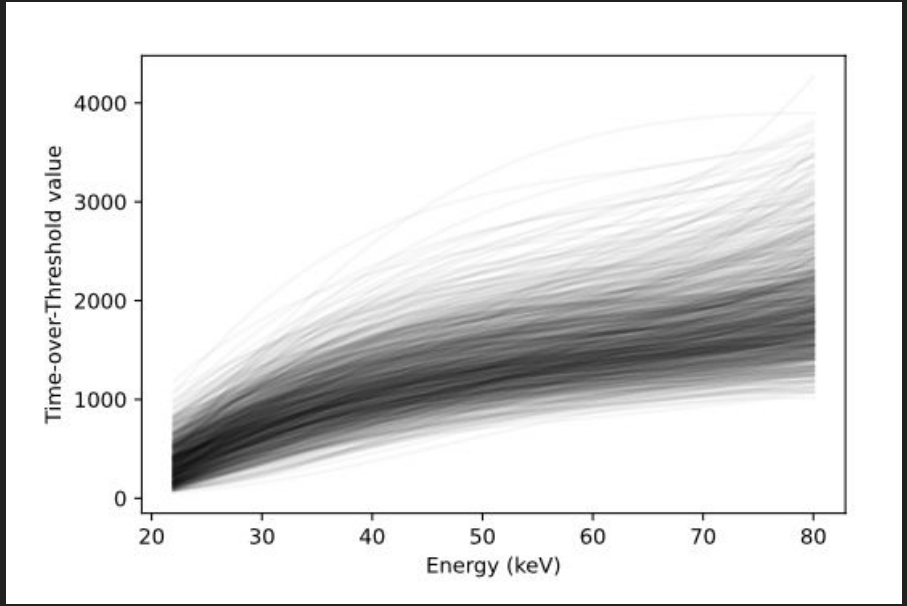
ComPair2 (gamma-ray beam, 2026)



- 10 layers, 96 quad chips/layer (3840 arrays, 20 SPI busses)
- V3 for testing, v5 for final

V3 characterization testing - Energy calibration

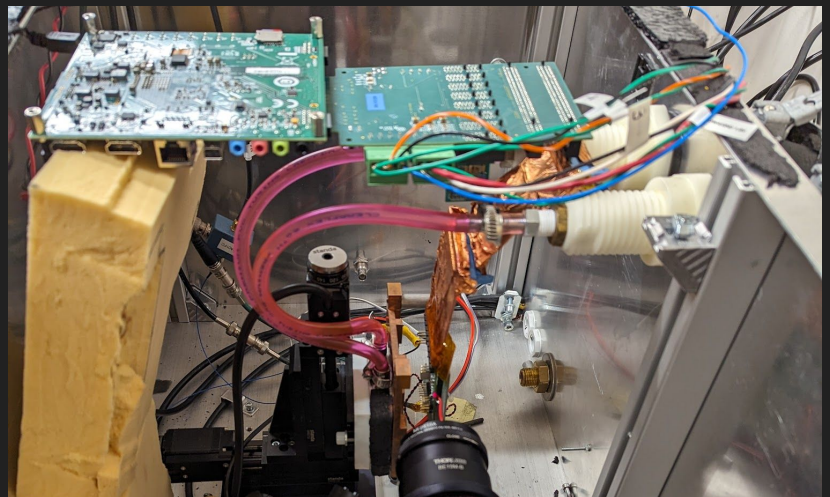
- Gain variation pixel-by-pixel
  - Must calibrate individually
- ToT limited by bit wrapping
  - Linear nature until ~80 keV
  - Nature of curve >80 keV under investigation at GSFC
- Will develop automated strategy for full-array calibration once these effects all understood



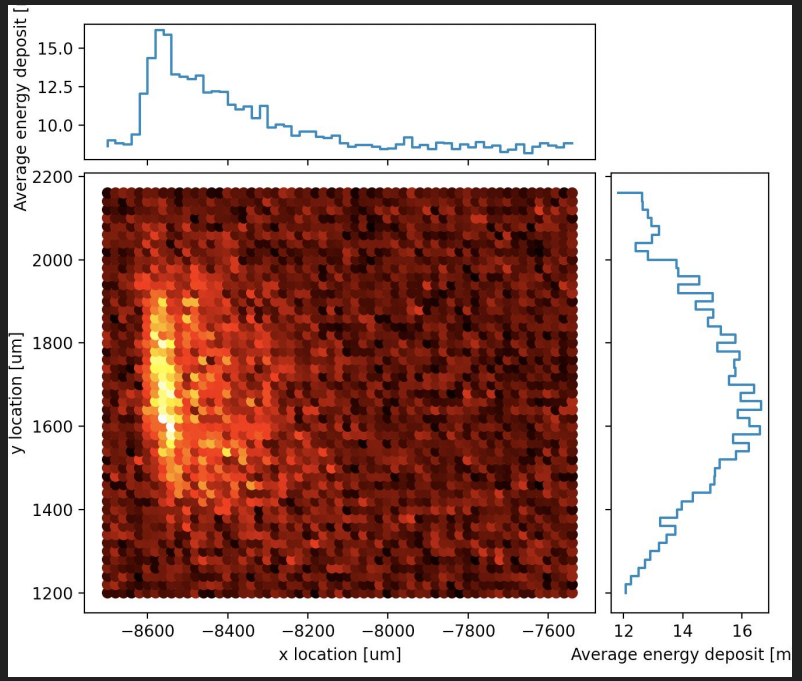
Y. Suda, in prep.

V3 characterization testing - Depletion

- November 2023 edge TCT test at UCSC to directly measure depletion depth
- Reflections, alignment complicate measurement
- Ongoing analysis at GSFC and UCSC



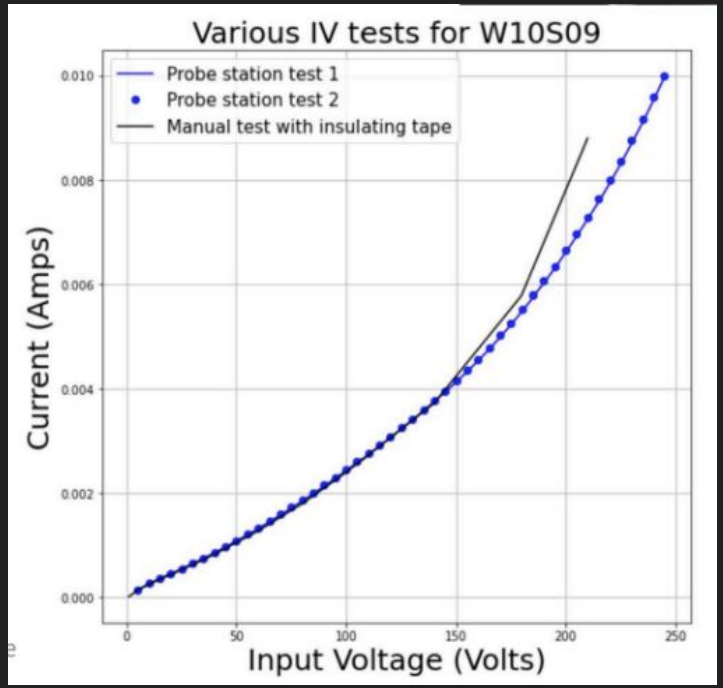
W02S09, -100V bias



Color scale = amplitude of analog pulse at scan point

V3 high-resistivity substrate

- >5 kΩ*cm substrate required for 500 μm depletion
- 25 kΩ*cm mounted chips for v3 saw breakdown <10 mV with high power dissipation on edges
- Probe testing breakdown >200V
- Conductive tape used for mounting to board caused voltage gradient
  - With insulating tape, breakdown >150V
- Future work : reconsider characterization with insulated chips

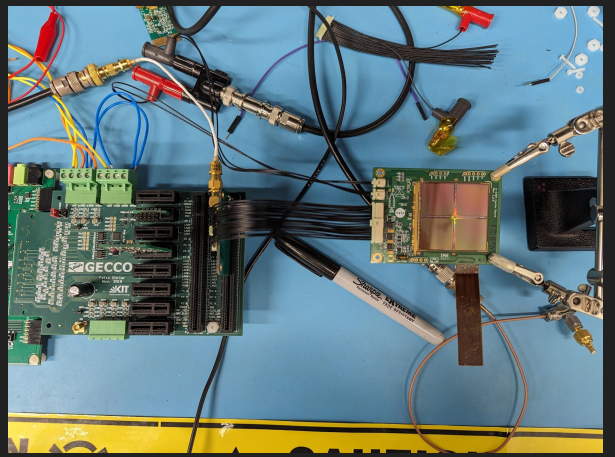


UCSC study

V3 Quad-chip testing

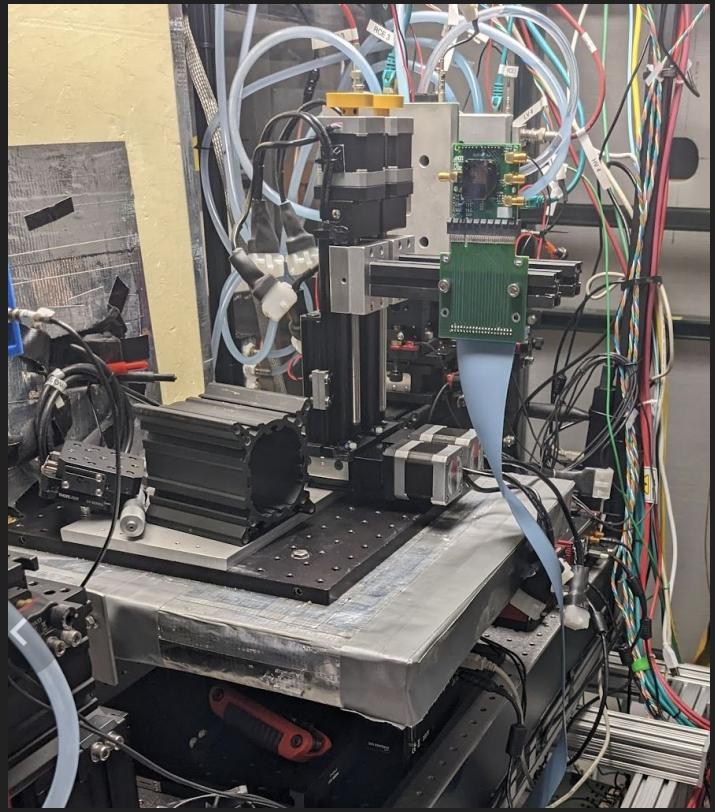
- First boards delivered Dec. 2023
- Full data collection not yet achieved
- Scaled-up FW:
  - Runs with single-chip board
  - Capable of configuring multiple chips along the daisy chain
- Board respin necessary
  - Correct pad locations for wire bonds to top two chips, update flex PCB bend to connector
  - Simplify voltage regulators for power to chip
- Full board redesign review after problems with current board fully understood/corrected

Highest priority = understand and correct quad-chip board



V3 testing in beamline

- More details in later talk
- Fermilab Test Beam time in May
  - 120 GeV protons
- Aim to test multiple layers of v3 quad-chips
  - Measure MIP peak
- Goal: get setup working in beam
  - Focus on tracking resolution study at next beam
- Goal: first beam data with v4



AstroPix_v4

- Operational testing on 2 global benches
- 3 wafer resistivities - 20, 300, 25k Ω*cm
- 500 x 500 μm^2 pixel pitch, 16 x 13 pixels
  - 1 x 1 cm^2 array
  - Component of multi-project wafer run
- Power consumption:
  - ~1.0 mW/cm^2 analog
  - 3 mW/array digital
- Asynchronous ToT, 3.125 (12) ns timing with external 20 (5) MHz power-saving clock
- Individual pixel tuneDACs
- Discontinue v3 row/col OR

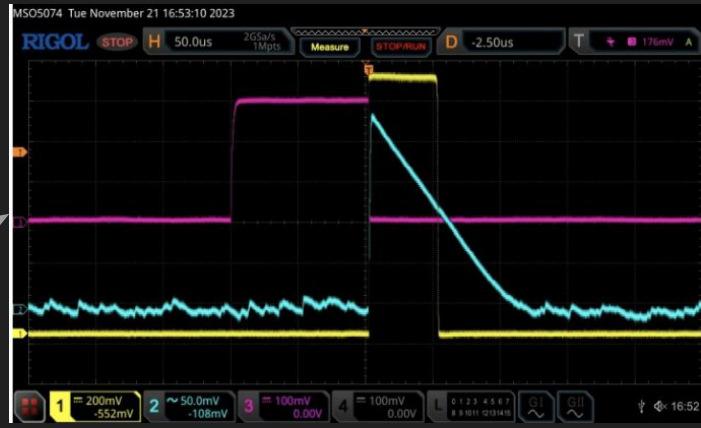
Mounted chips at ANL, distribution after preliminary operational testing

EIC workshop slides

V4 initial tests

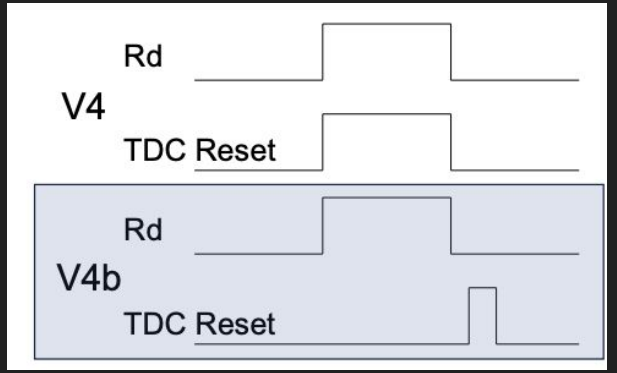
Successfully tested features

- FW and SW updated for operation
- Additional bits added to store ToT info (no digital ToT wrapping)
- Tune DACs
- PLL clock generation
- ~380V breakdown



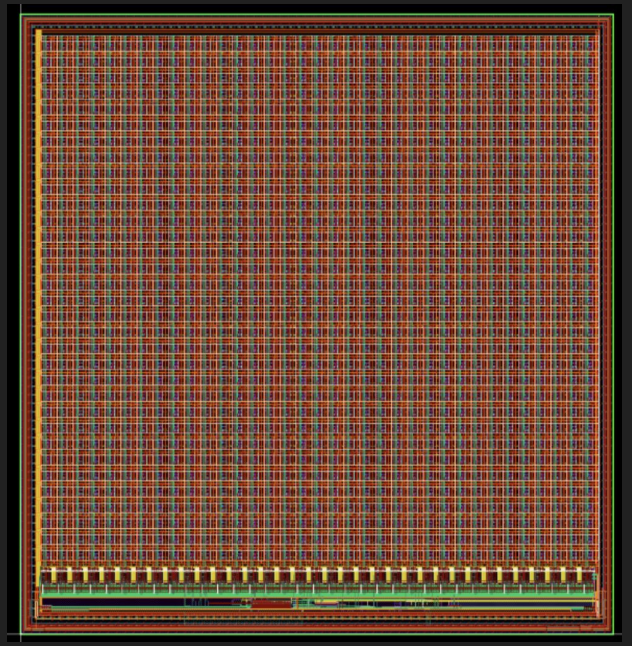
Fixes already implemented

- SPI readout noise - corrected carrier board design
- Flash-TDC timing corrected



AstroPix_v5

- Currently under design - submission within next few months
  - First fabrication with new foundry, AMS
- 2 wafer resistivities - 300, >5k Ω*cm
- 500 x 500 μm^2 pixel pitch, 35 x 33 pixels
  - Full size 2 x 2 cm^2 array
  - Component of multi-project wafer run
- Integrated voltage register for all neede input power lines
- Improved interrupt, readback config via SPI



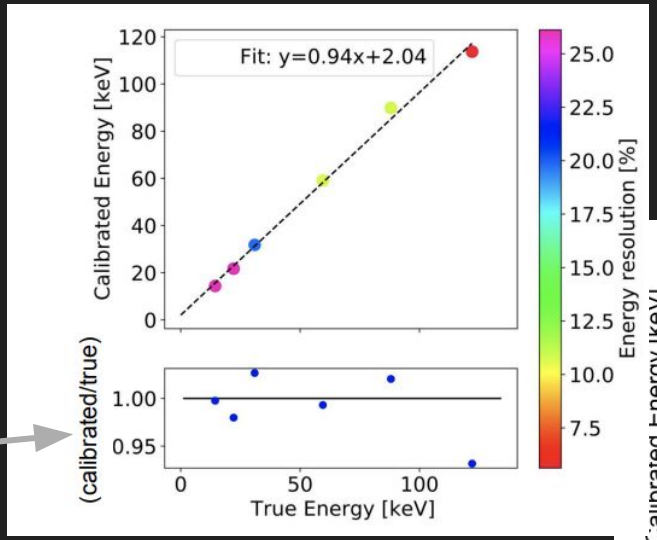
V5 Requirements

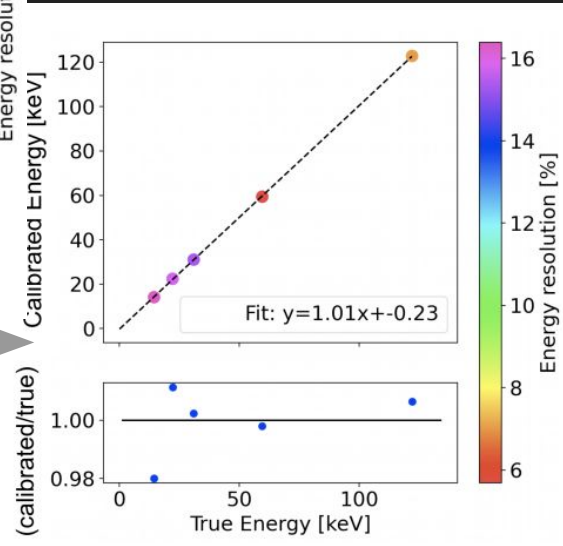
Parameter	Final Requirement	V5 requirement
E_res	5 keV σ @ 122 keV	5 keV σ @ 122 keV
Power	1.5 mW/cm2	Same as v4 or lower. (1.0 mW/cm2 analog, 3 mW digital)
Pixel pitch	1 x 1 mm2	500x500 um2
Si thickness	500um	525 um (thinned)
Depletion depth	500 um	500 um
Event Timing Resolution	1 us	<0.1 us (expect O(10)ns)

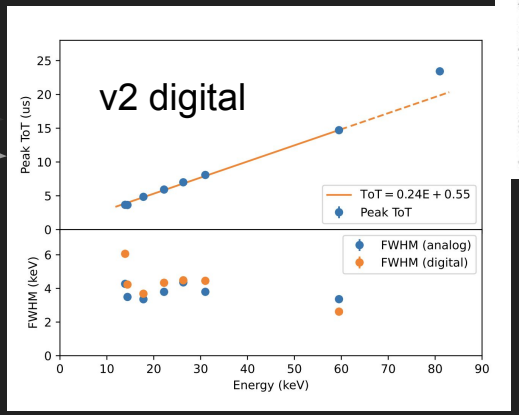
Backup

Publication history

- ATLASPix
  - https://arxiv.org/abs/2101.02665
  - https://arxiv.org/abs/2109.13409
- AstroPix_v1 (analog data)
  - https://arxiv.org/abs/2209.02631
- AstroPix_v2 (analog data)
  - https://arxiv.org/abs/2302.00101
- AstroPix_v2 (digital data), initial AstroPix_v3
  - https://pos.sissa.it/444/644/pdf
- A-STEP, utilizing AstroPix_v3
  - https://pos.sissa.it/444/579/pdf







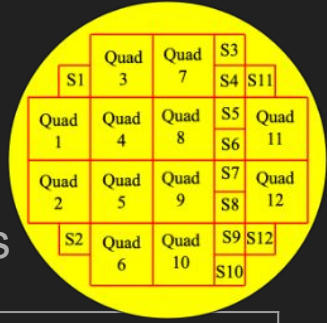
Digital Data

DIFFERENT DATA STRUCTURE IN V3 THAN IN V4

- OR row and column information to only two channels (row, col) are sent to digital top
  - Pixel array acting like strips
- Encoded digital information:
  - ChipID - relates chip to location in daisy chain
  - Payload - relates to SPI line
  - Location - row or column with comparator that measured over threshold
  - Timestamp - 8bit value counted with 2 MHz clock
  - isCol - boolean for row or column
  - LSB, MSB, ToT - time over threshold value, converted to us offline given clock speeds
- Each hit (row or column data packet) = 5 Bytes
- A “good event” requires:
  - One row and one column packet in same readout stream
  - Matching timestamp
  - No ToT matching requirement at GSFC

v3

V3 substrates

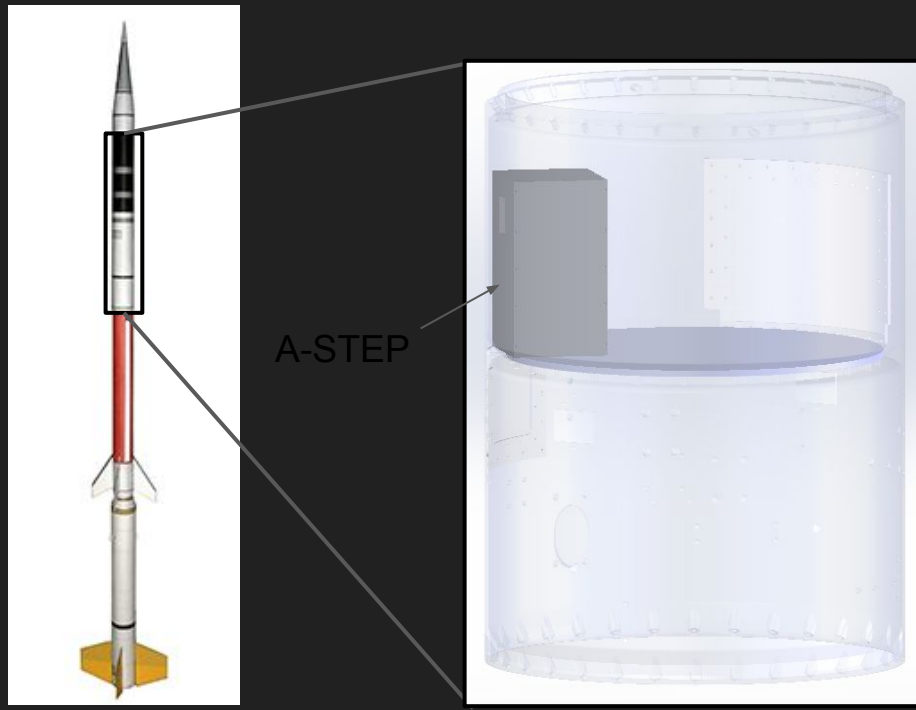


Fabricated chips (single chips and quad-chips) using 3 different substrates

	TSI Substrate	Okmetic Substrate	Topsil Substrate
Purpose	Testing	Backup	Flight
Resistivity [Ω*cm]	50	300-400	10,000
Number of wafers	2	2	3
Diced and mounted on test board?	Yes	No (in progress)	Yes
Breakdown voltage [-V]	250	290	High leakage current (uA) with any applied voltage
Leakage current, -150V [-nA]	40	40	High (80mA at -30V)
Testing notes	Low-quality substrate, high pixel variability	Primary test substrate, to fly on A-STEP	Challenging - WIP to understand

Work to be done for A-STEP

- First flex bus bar designed to connect upper 2 chips in quad chip ✅
- First test of chip daisy-chains
- Scaling of firmware to handle multiple chips / multiple layers ✅
- Mechanical testing of wire bonds, support structure (windowpane-like supports, not solid PCB)
- Flight software for data packetization and telemetry (new sophistication to DAQ)
- Eventual environmental testing of full system
  - Vibration, temperature/vacuum, etc



Firmware Development Highlights (2023)

Led by R. Leys and N. Striebig (KIT)

- Two FW lines
  - “simple” / easily hackable version for 1 chip and NEW multi-layer / multi-row FW
- Support for multiple targets
  - Different FPGA boards (bench testing vs A-STEP flight) and chip configs (single chip, multi-layer, etc)
- FW-driven SPI readout
  - Previously, SW-driven readout strategy introduced additional deadtime
  - Now chip itself triggers readout when there is data in buffers
  - Sensor data frame detection IDLE discard, Tagging/reframing, routing to single Readout Buffer
  - Readout config options: Continuous, interrupt driven, trigger support (in development), etc
- Scale-ability
  - Read through the daisy-chain in FW rather than SW
  - Each daisy-chained SPI input has own interface which feed into global buffer (one chip reads out a time)
    - Supports up to 20 SPI inputs but exact number in use can be easily modified

MORE Firmware Development Highlights (2023)

Led by R. Leys and N. Striebig at KIT

- Host communication
  - Interface with computer via Host SPI, USB-UART, FTDI USB-FIFO (for now)
- Simulated test structures and ease of coordinate development
  - Improved Python SW interfacing with FW type
  - Version discovery to ease SW development
  - Simulate hit data at “SPI interface to global buffer” level
  - Python-based verification (Cocotb) allows SW testing in simulation, regression testing
  - WIP: Generate physical SPI frames for verification simulations (N. Striebig, S. Scherl)
- Housekeeping
  - Include packets of housekeeping data in data stream, as defined by user (voltages on FPGA, FPGA temp, etc)
  - FPGA XADC driver for internal values, SPI channels for external ADC
  - Readout and external IC support fully SW driven