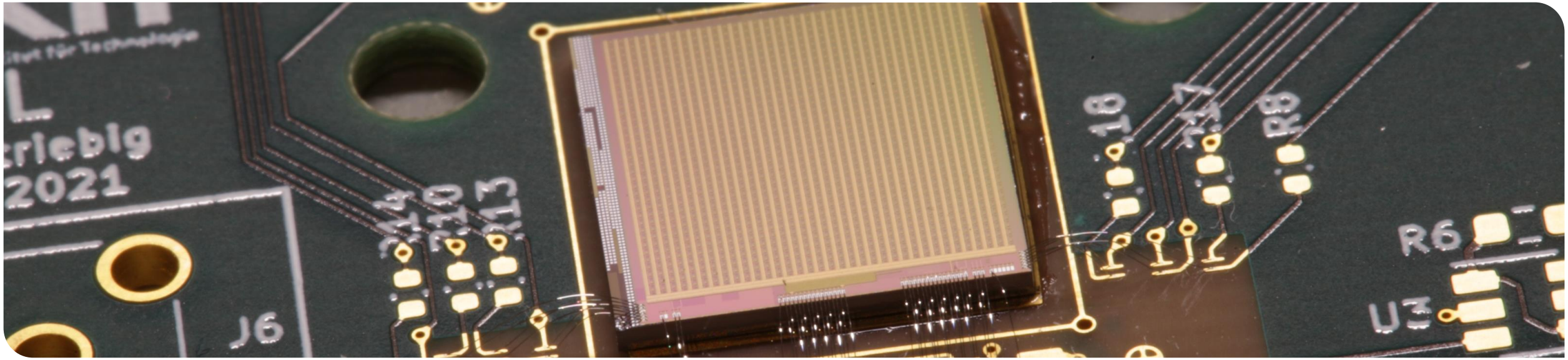
AstroPix5 Updates

Nicolas*, Richard
*striebig@kit.edu



Specifications

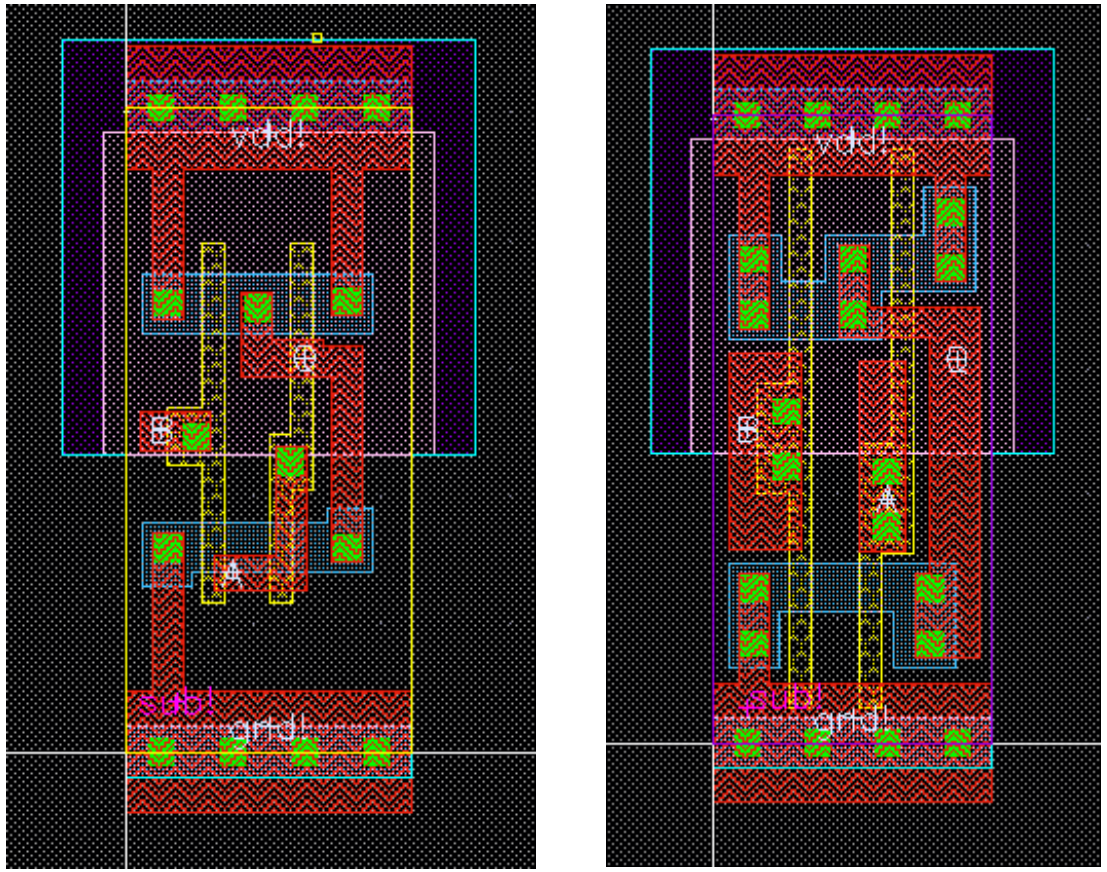
- AMS ah18 180nm process
- Only 6 metal layers vs 7 with TSI
- +/- 2 cm x 2 cm chip depending on quad chip size
  - Can be adjusted by modifying number of columns/rows or slightly increasing pixel size
  - Figure out with AMS how large a single chip has to be to get a quadchip of a certain size
- HiRes substrate >1kOhm

- Submission planned for Mid April -> Receive wafers back September

Digital Design Updates – AMS Designkit

- Additional double cut standard cell library
  - Minimum 2 vias instead of 1
  - Better yield
  - 15% higher dynamic power

NAND2X1

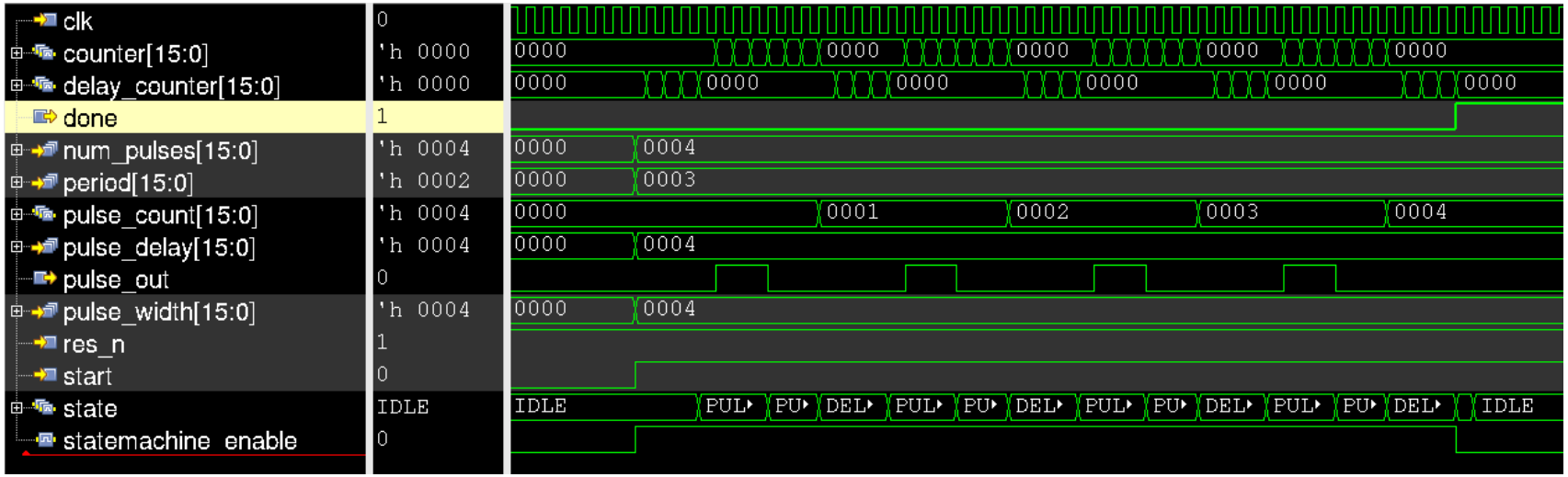


Standard DCV

Digital Design Updates – Pulse generator

- Integrated injection generator
  - Configuration via SPI/SR
  - Similar to patterngen in astropix-fw/astep-fw
  - External injection still possible
  - Parameters:
    - Delay
    - Number of pulses
    - Period
    - Pulse width

- Injection pulse generation now completely integrated with injection switch and VDAC from V3



Digital Design Updates – Improved interrupt

- Currently interrupt is deasserted if readout fifo is empty
- Issue:
  - Does not mean that data has been read out yet
  - Could still be somewhere in the chain
  - DAQ has to toggle spi clock much longer to be sure everything is read out
  - Not power efficient

- Improvement
  - New interrupt logic takes status of readout fifo and daisychain fifo into account
  - DAQ can stop when interrupt is deasserted
  - SPI active duty cycle is lower -> lower power consumption

Digital Design Updates – TS counter

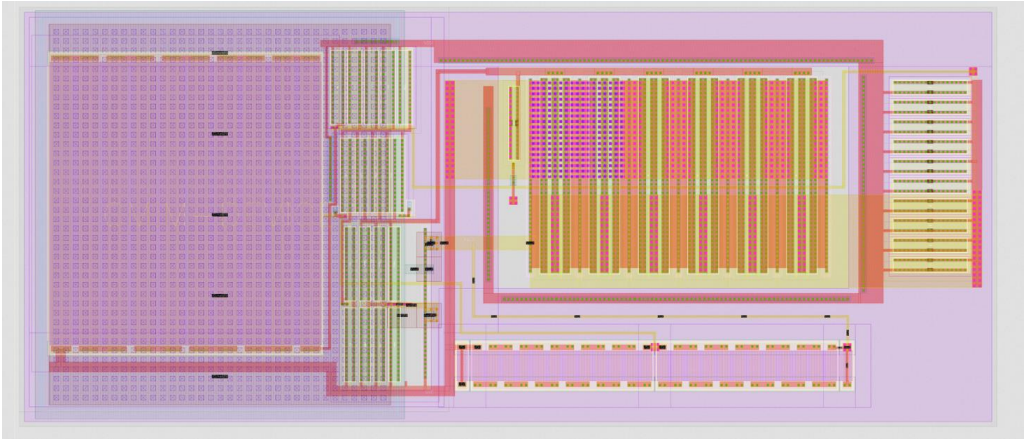
- Added syncreset input to reset TS counter for synchronization between chips
  - Currently TS counter only resettable via res_n
- Added configurable clockdivider
  - Divide 20 MHz TS clock to 10 MHz to save power
  - Max. resolution decreases to 6 ns

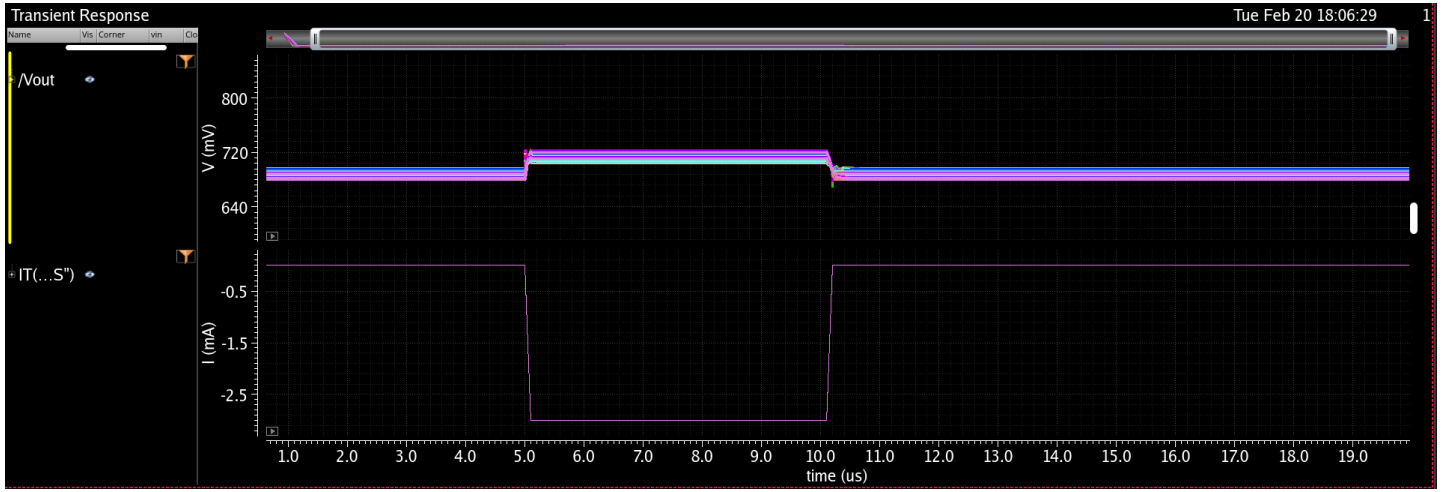
Digital Design Updates – SPI

- Increased SPI right fifo size by factor of 3
  - Lower risk of invalid frames due to congestion in the chain
- SR command now supports up to 7 load signals (Ld, LdTDAC, LdPulseGen)
  - With V4 TDAC was not configurable via SPI

Analog Design Updates – Vminus Regulator

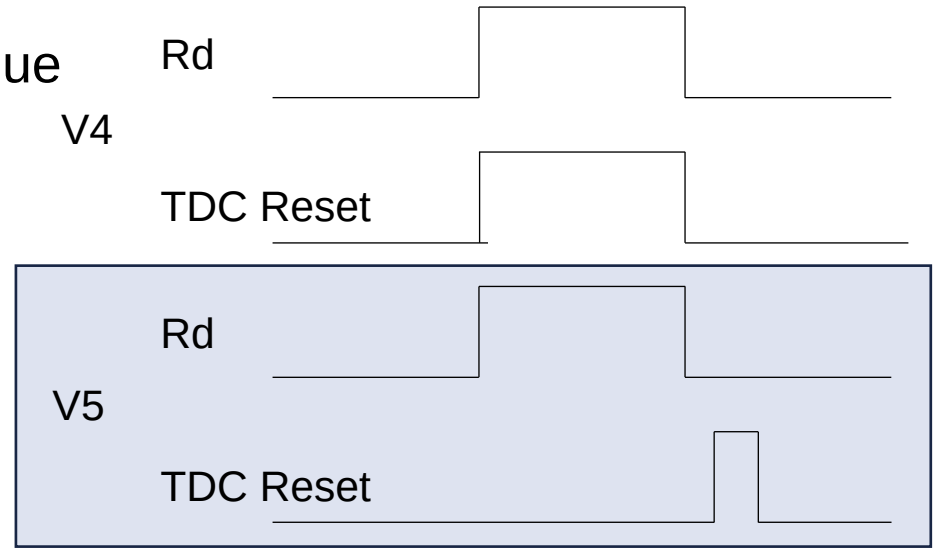
- Implemented a voltage regulator for vminus
- Voltage level can be set by VDAC
- Operating range: 1.62 - 1.98 V
- Power consumption: 180 uW
- Load current: 0 – 10 mA
- Phasemargin >40° for capacitive loads 1 fF to 100 nF
- Simulation pulse 0 to 3 mA
  - Corner simulation: ff, fs, sf, ss
  - Temp: -40, 25, 125
  - Capacitive load: 1pF – 100nF

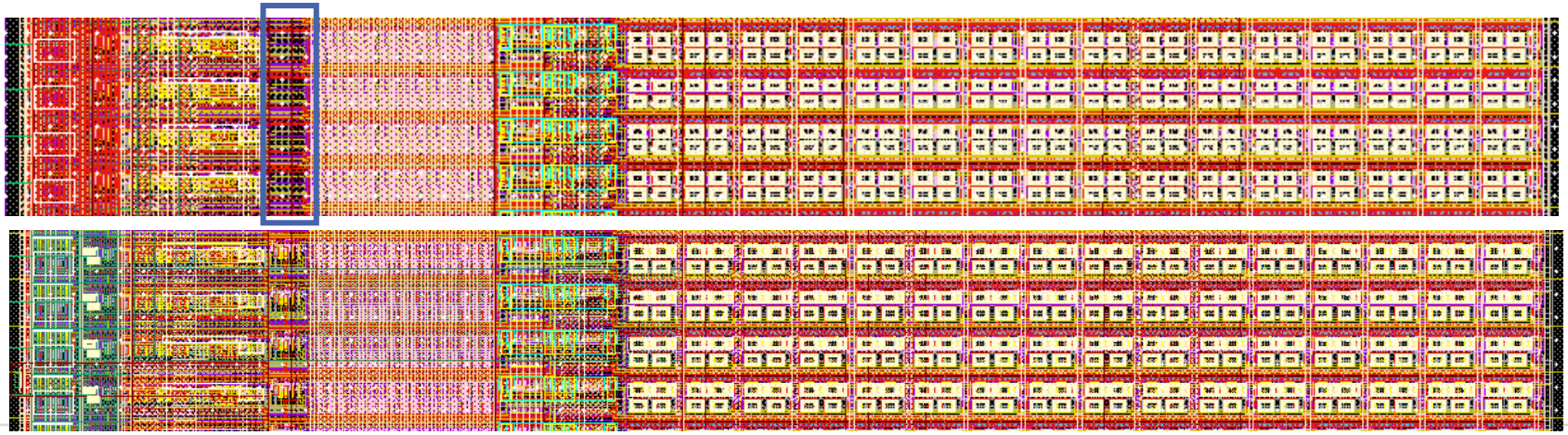




Analog Design Updates – TDC Bugfix

- Fixed TDC reset bug which prevented readout of TDC value
- Modified reset in a way
  that it can become active only after Rd and some delay





old

new

Analog Design Updates – General

- LVDS driver for differential SPI
  - works good besides from high supply voltage corner (1.98 V)
  - WIP
- Fix missing shielding of digital pads
- Add pads to monitor PLL clock and DLL output
- Pixel: Improve BLRes