Wafer QC probing overview

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Overview of chip production and test for ALICE ITS2

1500 raw wafers

Raw Wafer Production
MEMC (Italy)

5%

Raw Wafer QA
TMEC (Thailand)

1200 CMOS wafers

CMOS Manufacturing
TowerJazz (Israel)

8%
(2/25)

Wafer Probe Testing
CERN

60,000 chips

Thinning & Dicing
FUREX (South Korea)

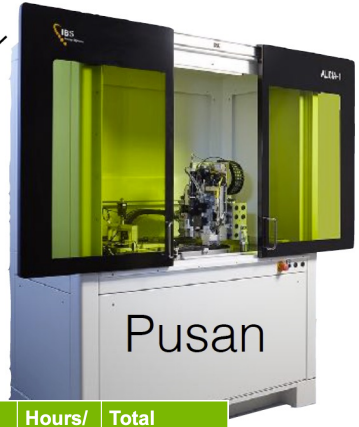
Currently,
checking the consistency

Pick & Place
FUREX (South Korea), tbc.

100%

Chip Series Testing
Yonsei, Pusan/Inha
(South Korea)

Detector assembly

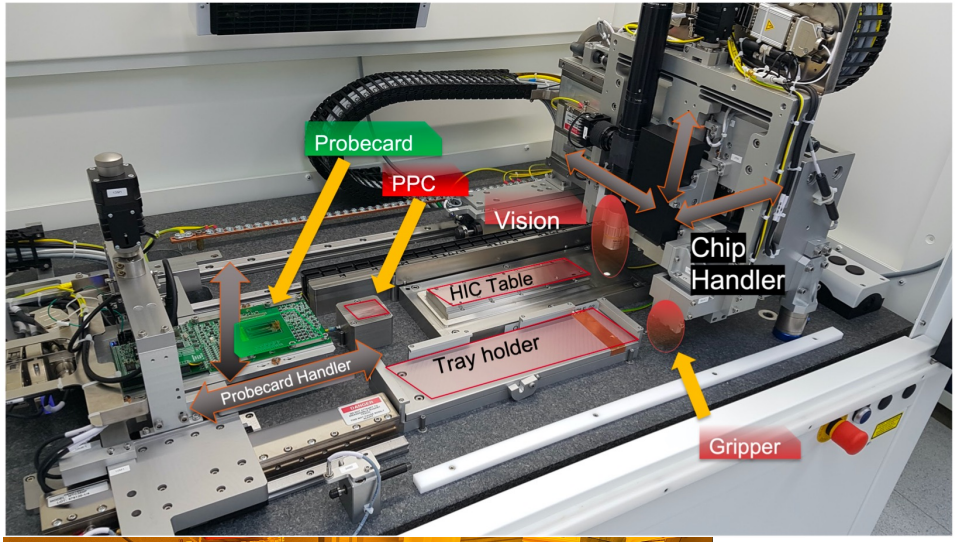


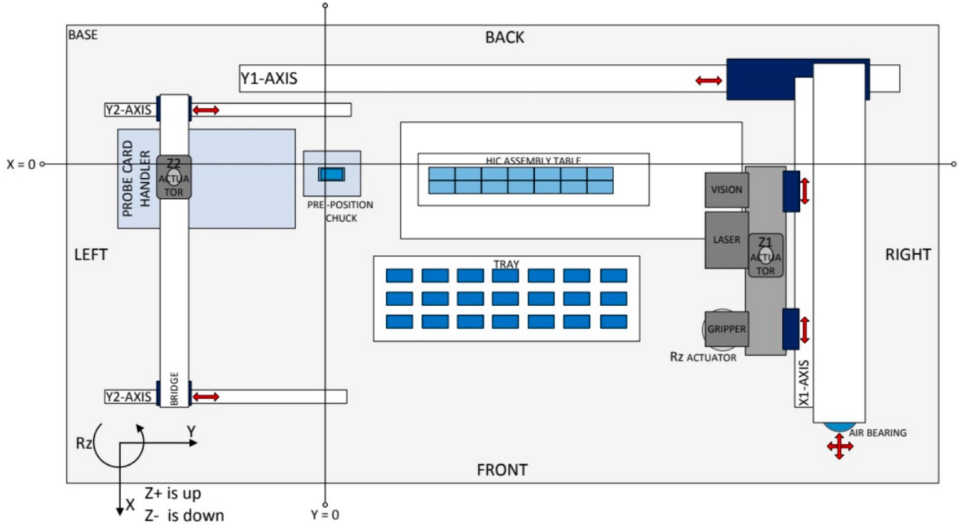
ALICE 3 Outer Tracker
2100 wafers, 120,000 chips

ePIC Barrel Imaging Calorimeter AstroPix
5000 wafers, 250,000 chips

	# On-Detector	Yield	Total to Build	Total Good After Yield	Hours/ piece	Total Hours*
wafers			4838			
chips	249,600	89%	290,304	261,274	0.05	14,515
modules	31,200	98%	32,659	32,006	0.21	6,858

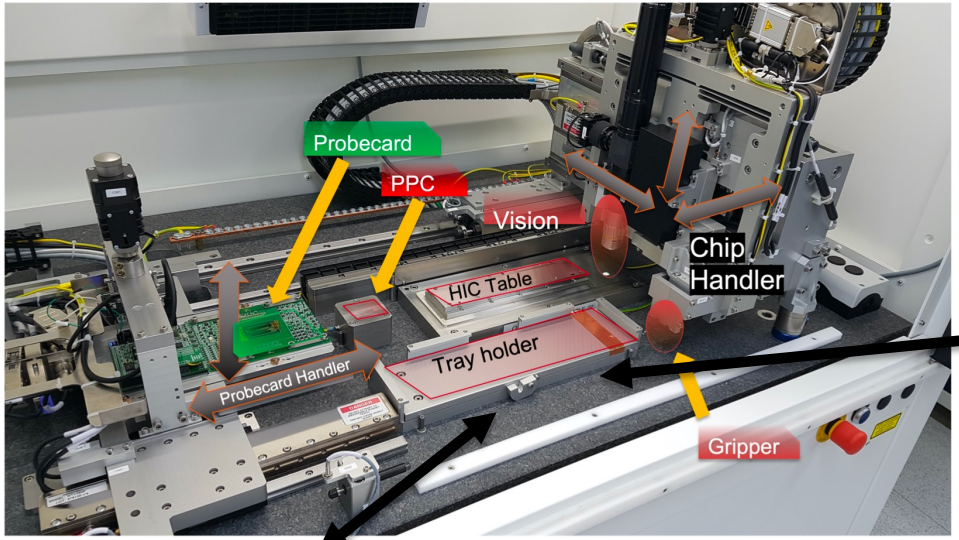
Chip test machine (ALICE ITS2, ALICIA)

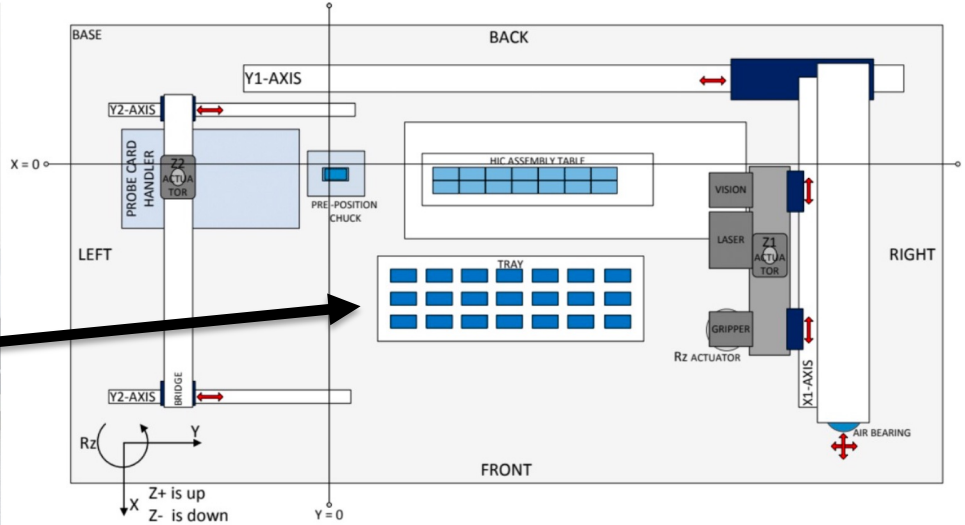


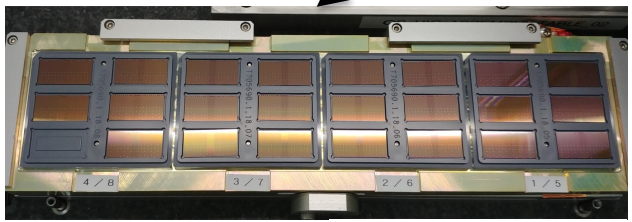


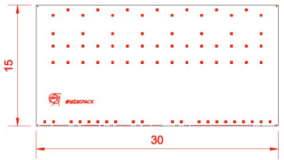
- Two PCs control the chip test system
- One (right) PC to control the chip handler
- Another (left) PC to control the probe card
- Two PCs are communicating to check the status and transfer test results

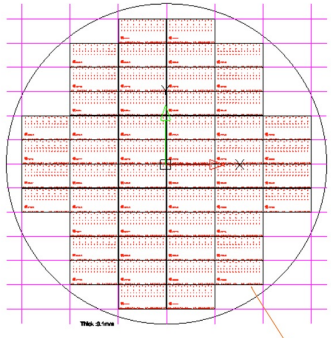
Chip test machine (ALICE ITS2, ALICIA)











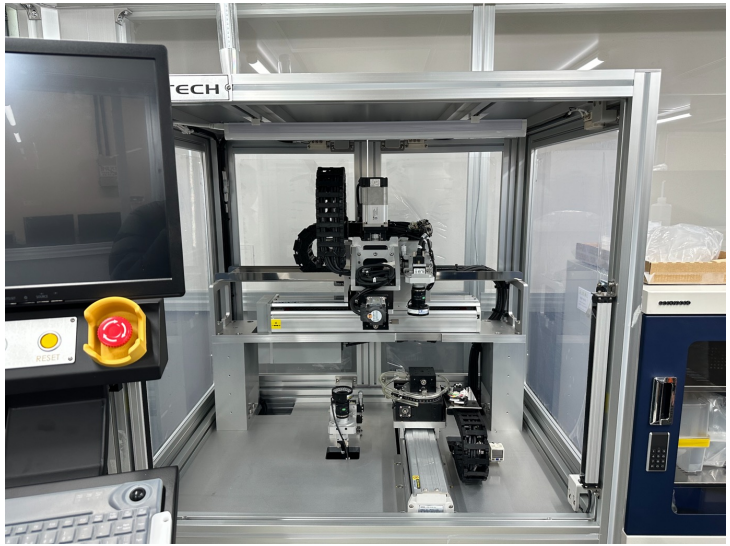
Wafer of dummy chip

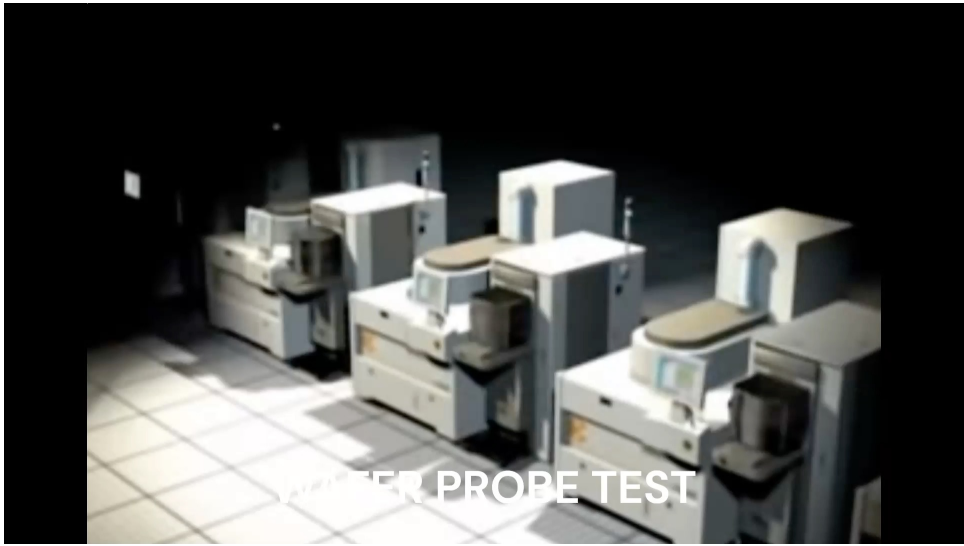
- Dummy AstroPix chips with bonding pads
- With a new tray, the operation of the chip handler can be customized for AstroPix
- Wafer-level chips can be also used for the wafer probe later

Preparation for development of chip test procedure

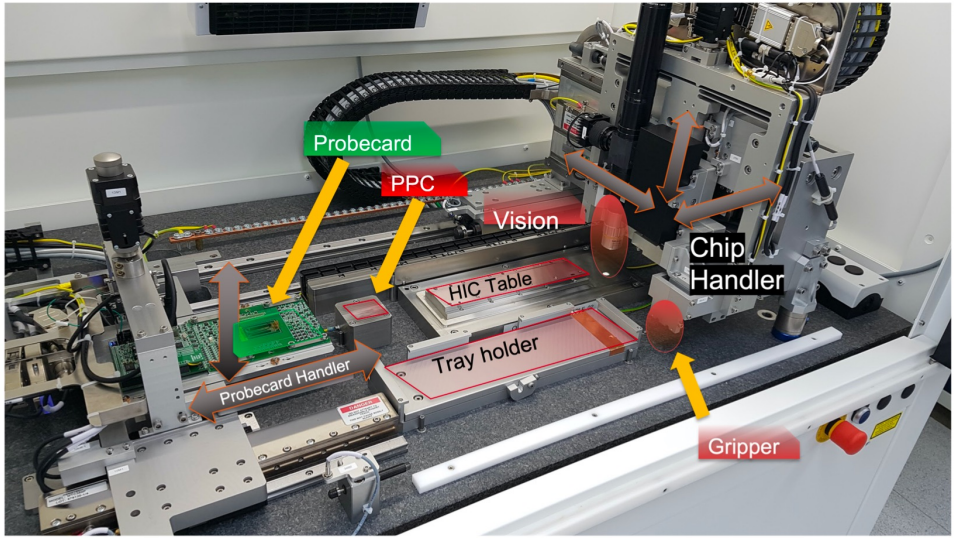
- Preparation for a setup to develop the chip test procedure
  - Tune up an automatic chip handler machine for various chip design
  - Plan to verify the performance by comparing it with the reference results (ALPIDE chip tested by ALICIA)
  - Plan to contact the ALICIA manufacturer for customizing

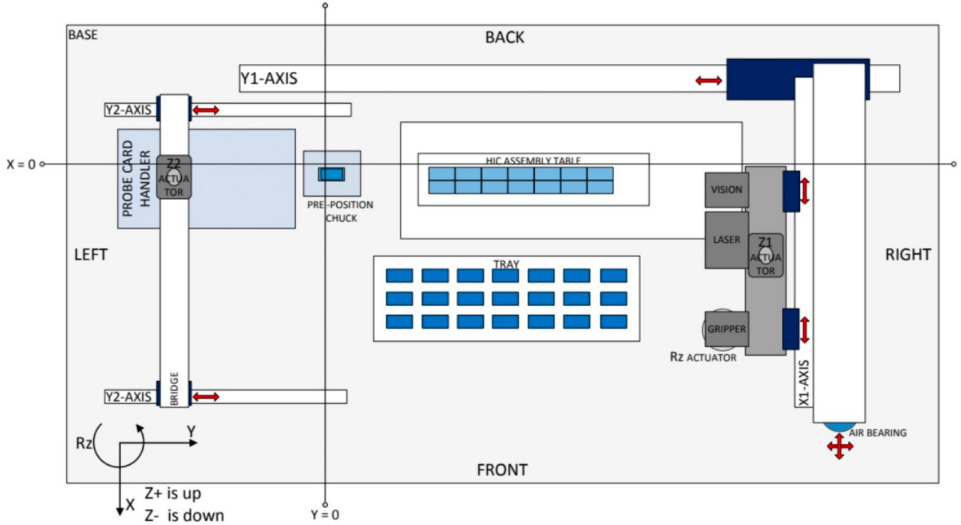
- Search for a local company working on wafer probing
  - Will have an initial discussion based on the mass chip test of ALPIDE (ALICE ITS2)

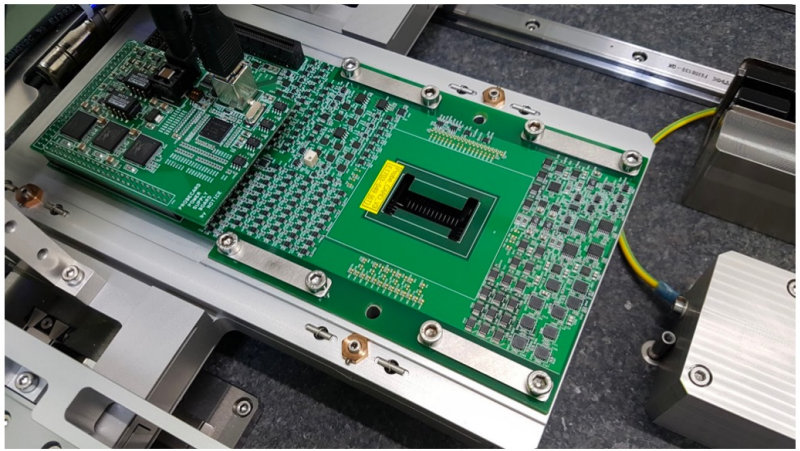


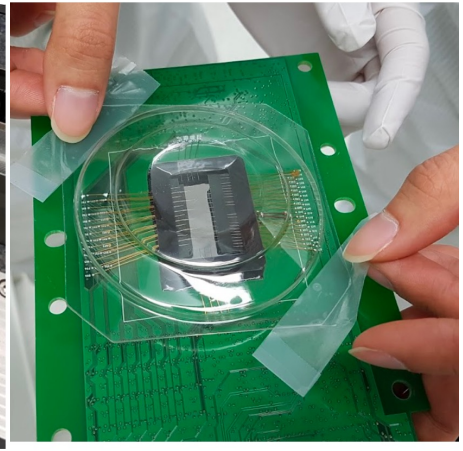


Chip test machine (ALICE ITS2, ALICIA)

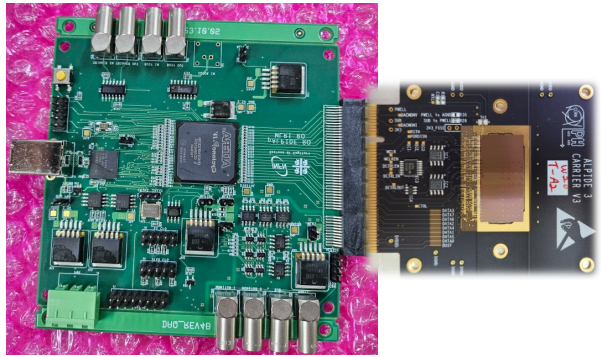




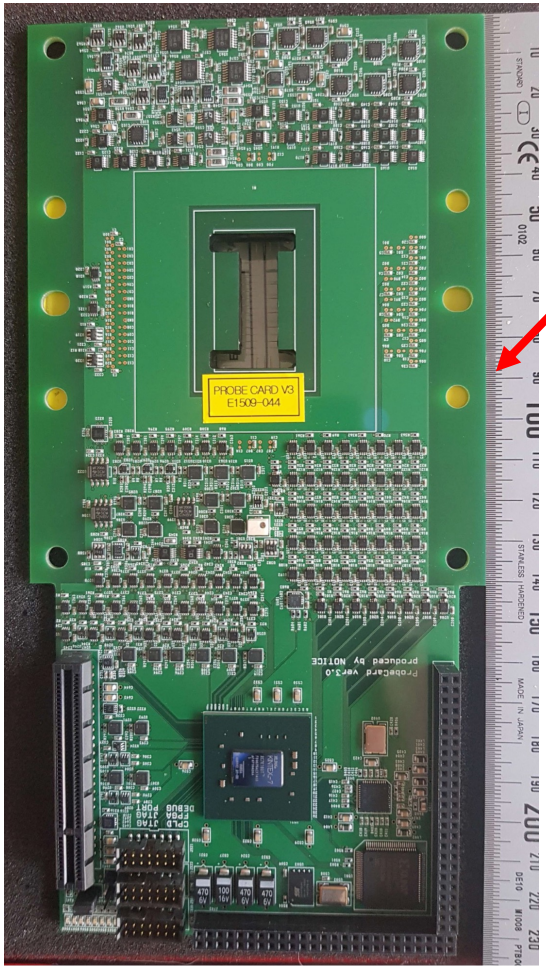




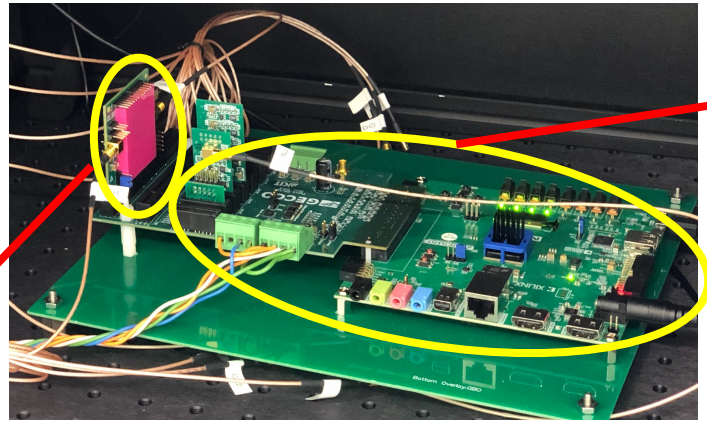
ALPIDE single-chip test bench

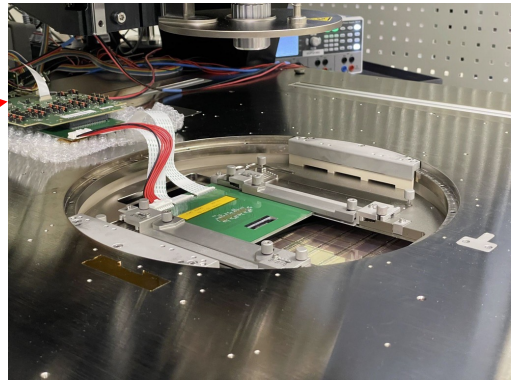


Probe card for AstroPix v3



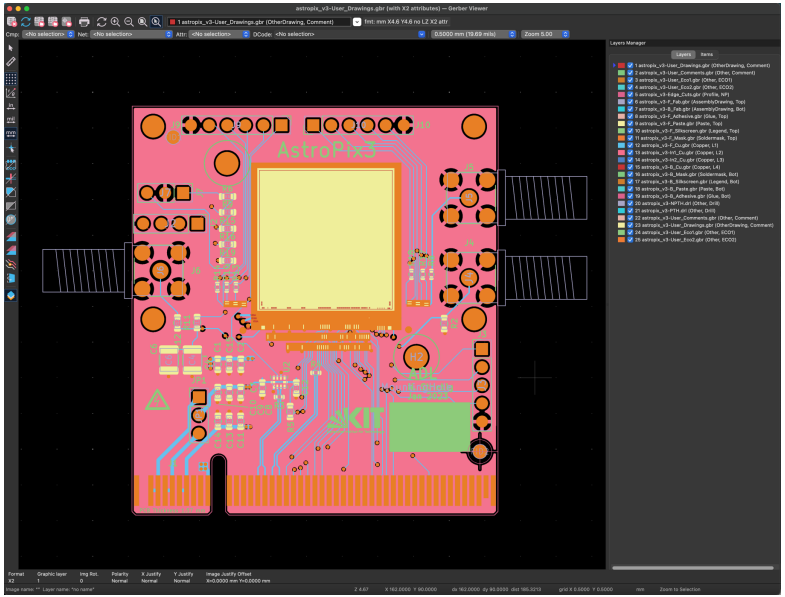
Probe card for ALPIDE

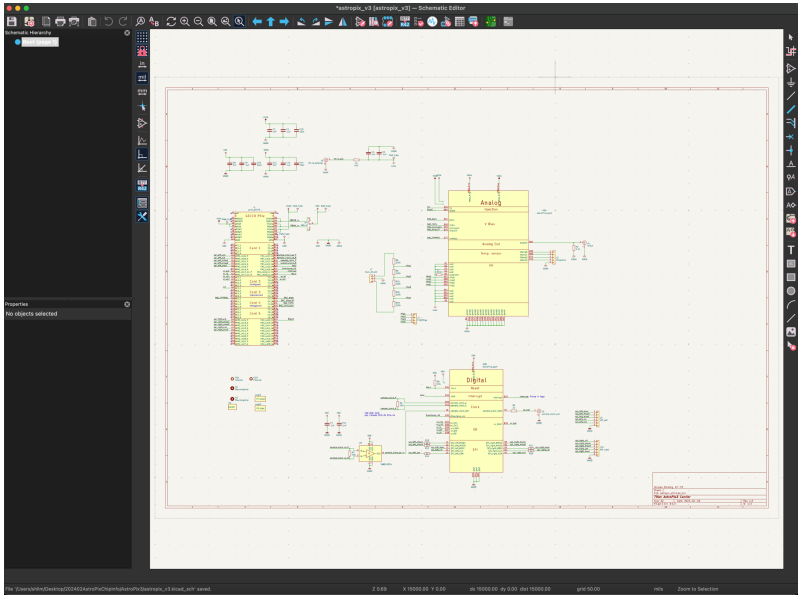


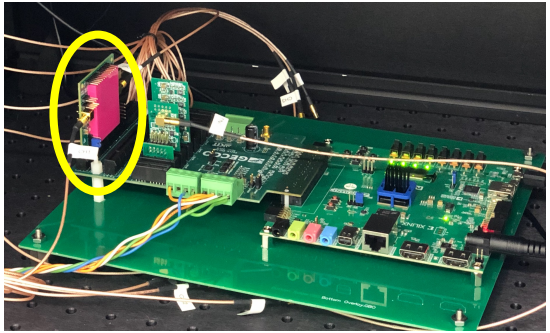


- Initial version for AstroPix v3:
  a simple version for the carrier card only
- Considering the same dimension as the ITS2 probe card to utilize the ALICIA machine for the initial test
- GRECO and FPGA development boards can be connected with flexible cables

Probe card for AstroPix v3



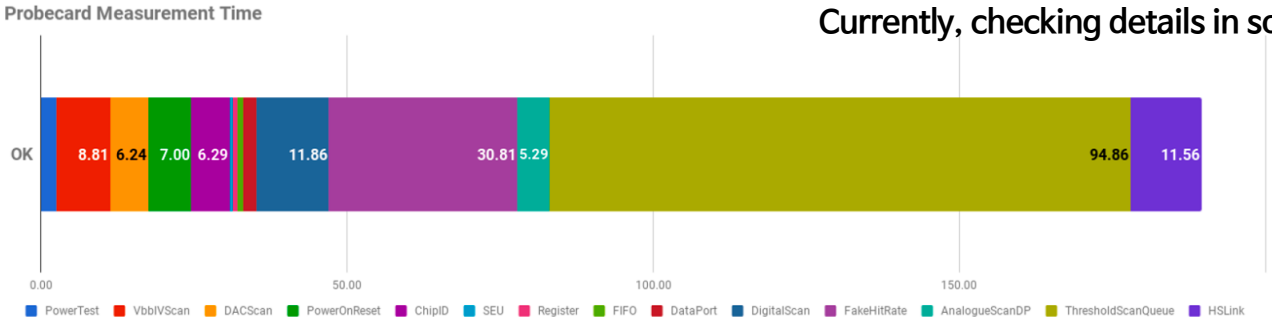




- Received design files for AstroPix v3 single chip carrier board and bonding pads
- Working with a local company (NOTICE) to design a probe card
  Received initial feedback today and will keep communicating with NOTICE
- Firmware and software of AstroPix v3

Chip test procedure (ALPIDE)

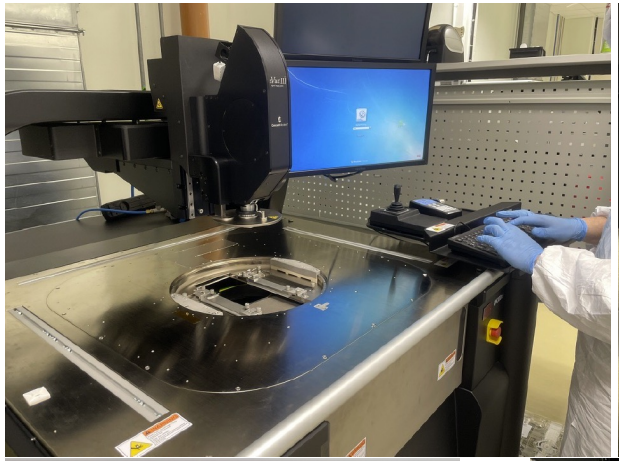
- **Powering test:** just power on/off
- **V_{bb} I-V test:** apply the reverse substrate bias from 0 V down to −6 V
- **DAC scan:** verify that each DAC is working by scanning through all its code words
- **Power on reset test:** check the functionality of power on reset
- **SEU check:** monitor the SEU counter and the flag bits on idle operation
- **Register test:** check all registers by writing and reading back to find stuck bit
- **FIFO test:** check all the generated memory blocks
- **Data port test:** verify its functionality to send quasi-static patterns in case of the readout test failure
- **Digital scan:** inject single hits directly into the in-pixel memories and read back
- **Fake hit rate:** measures the number of noisy pixels and faulty front-ends
- **Analog scan DP:** exercise the analog front-end and the full readout chain of ALPIDE
- **Threshold scan:** test all analog front-ends/pixels by using analog pulse injection
- **High speed link check:** check its functionality

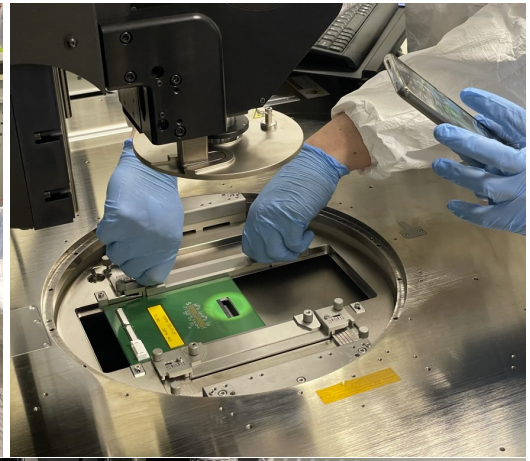


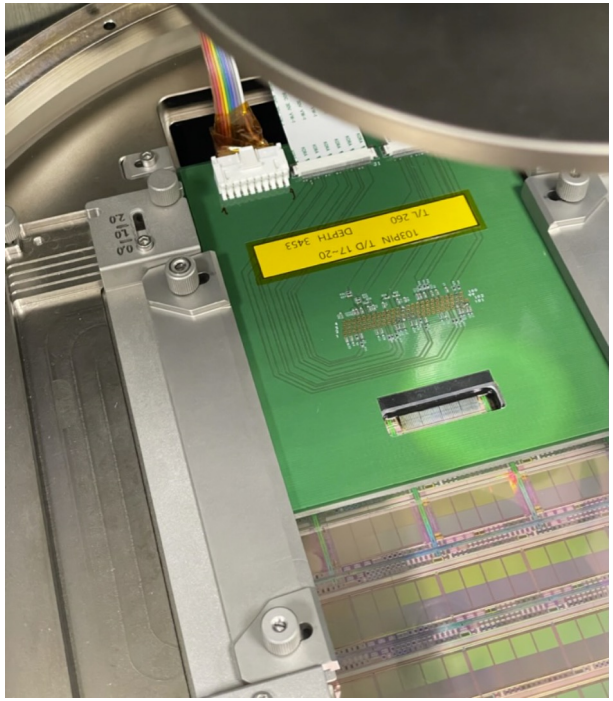
Currently, checking details in software and firmware

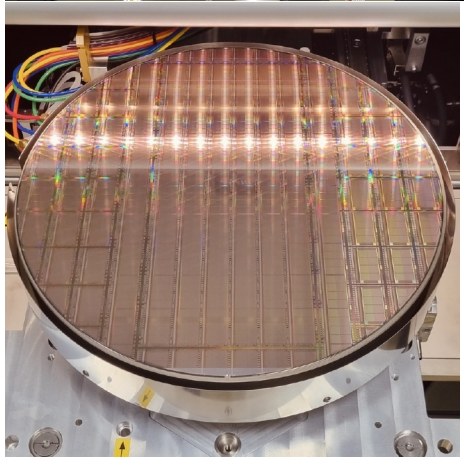
Preparation for development of chip test procedure

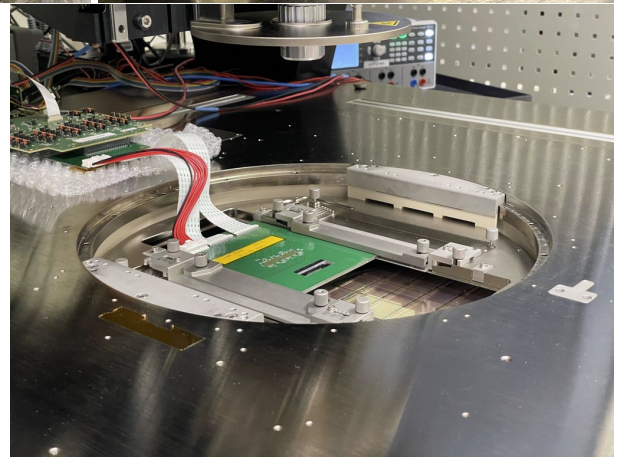
- Wafer testing system for ALICE ITS3 at CERN





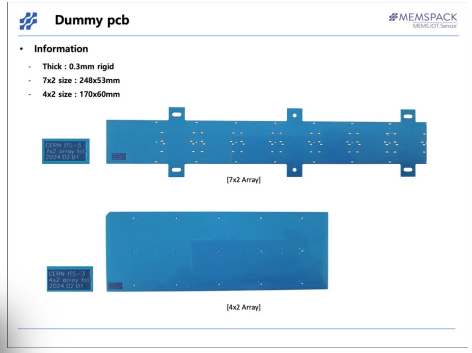


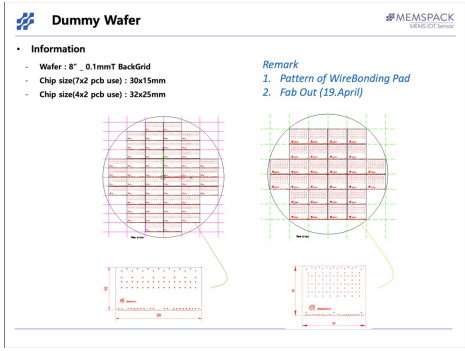




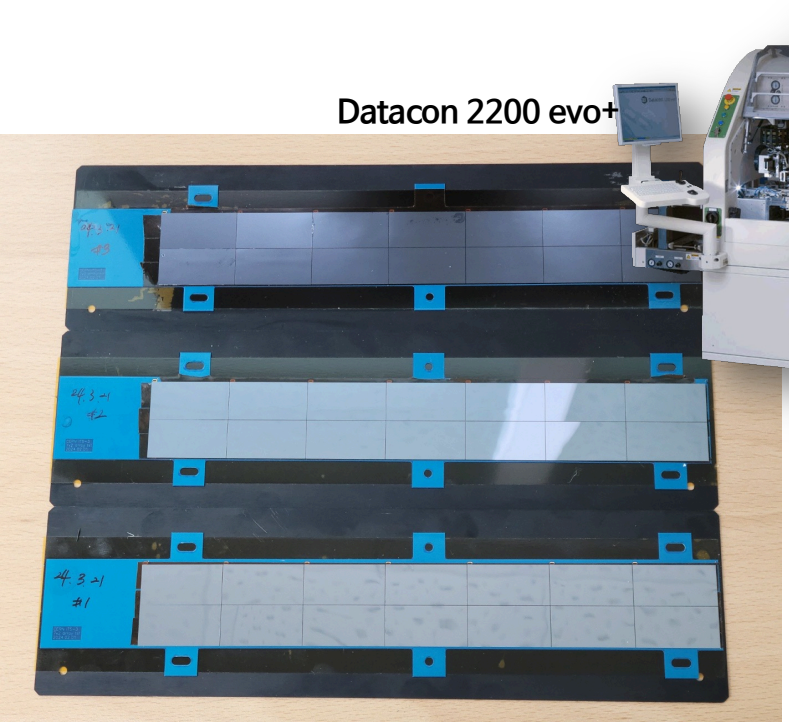
Short update on the module assembly (ALICE 3 Outer Tracker)

- Produced a few dummy modules with good position precision by a local company (MEMSPACK)
- Dummy modules will be used for stave design and test





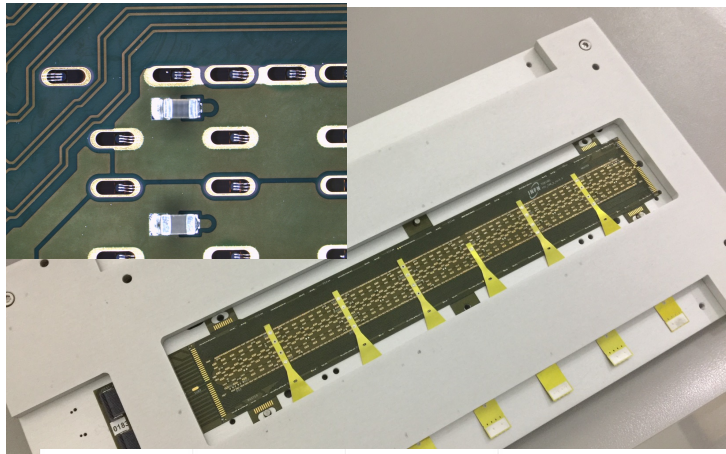
Datacon 2200 evo+



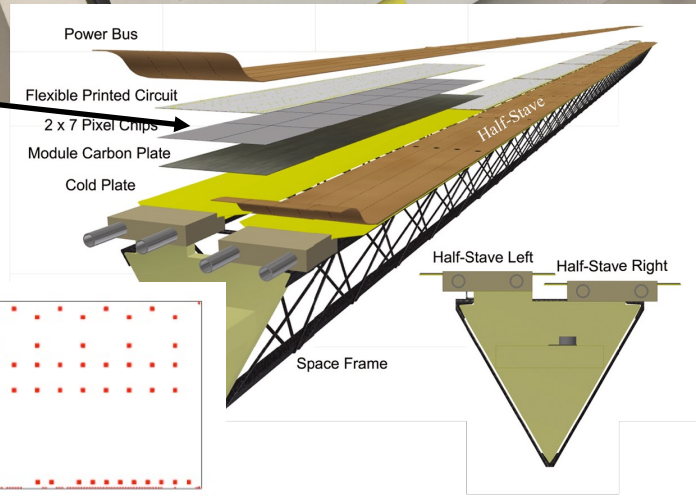
Short update on the module assembly (ALICE 3 Outer Tracker)

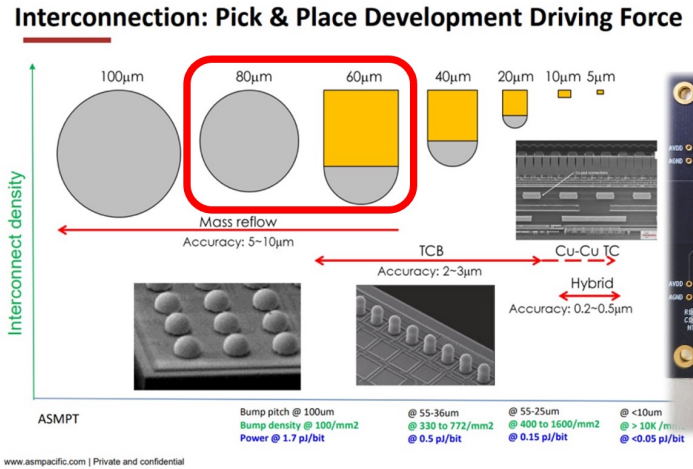
- Recently have an initial discussion about bonding
- ITS2 OB used wire bonding to connect FPCB and bonding pads spread through the entire surface area

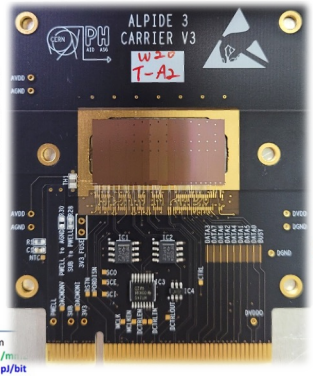
  Experienced some failures of wire bonding due to epoxy covering the bonding pads
- Plan to test different types of bonding with dummy chips:
  wire bonding with pad at the single edge
  bump bonding with and without epoxy

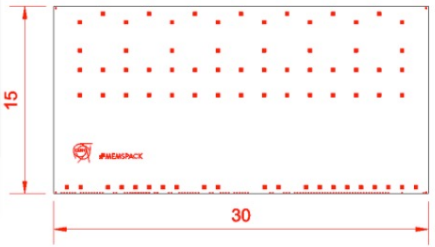


front side with bonding pads



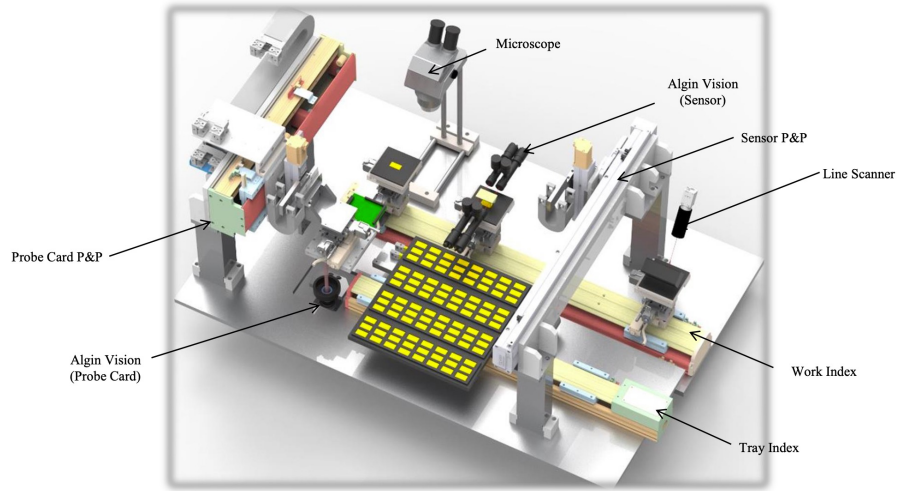


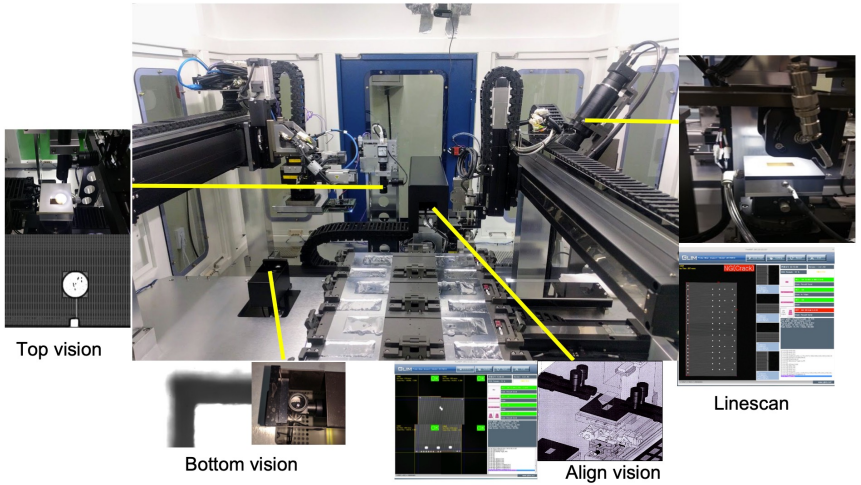




BACKUP

Chip test machine (ALICE ITS2, COREA-YS-01)



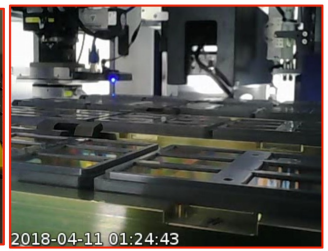


A simpler version of the machine dedicated to chip test

Arrival scan

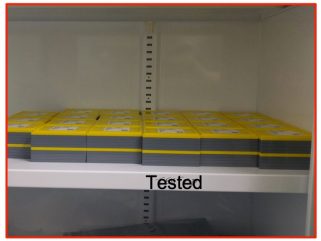
Sensor preparation

Class 100, ~10 min.

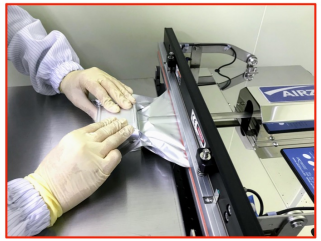


Fully automated test and remote control

Class 10, ~10 hours



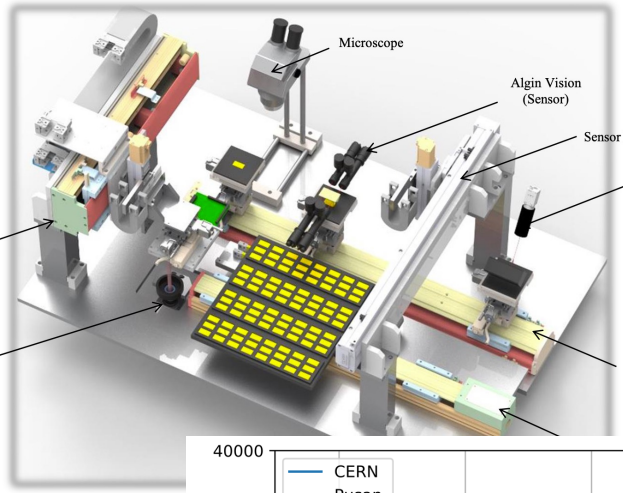
Storage inside cabinet

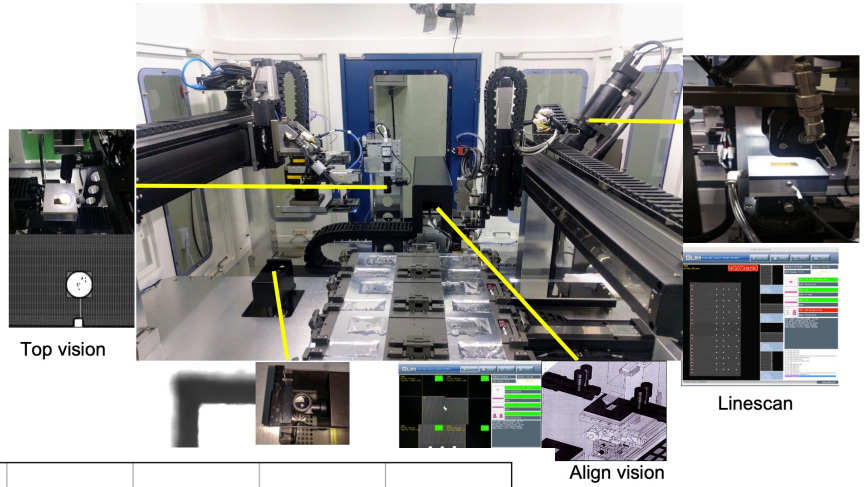


Packaging for shipment

Shipment

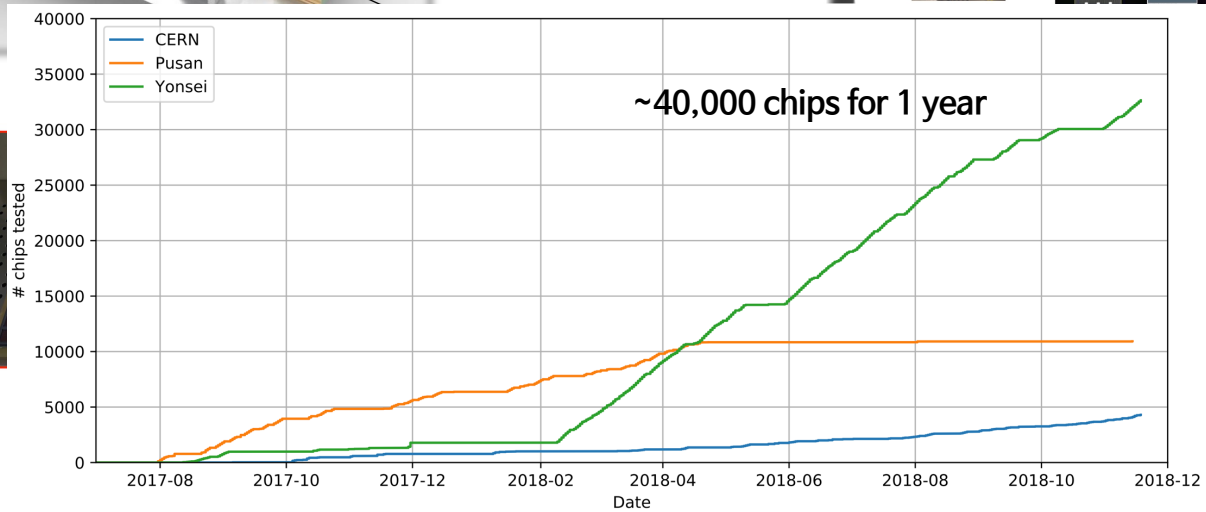
Chip test machine (ALICE ITS2, COREA-YS-01)





ed to chip test

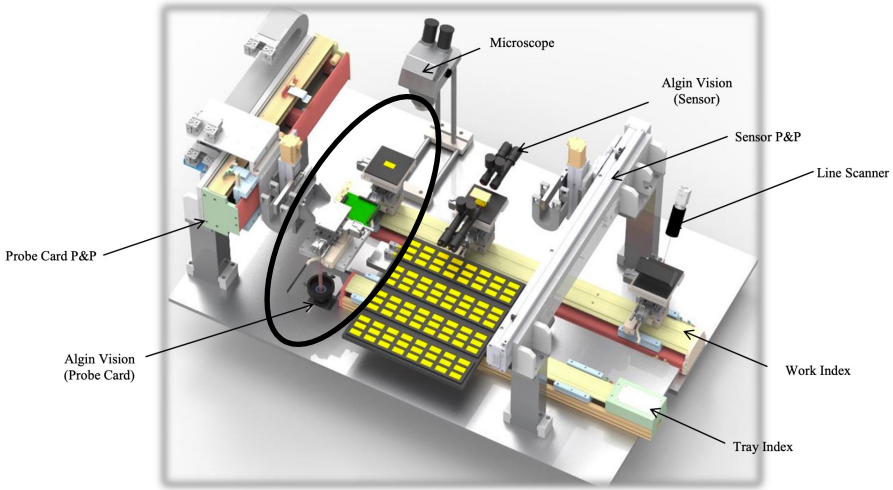
Arrival scan

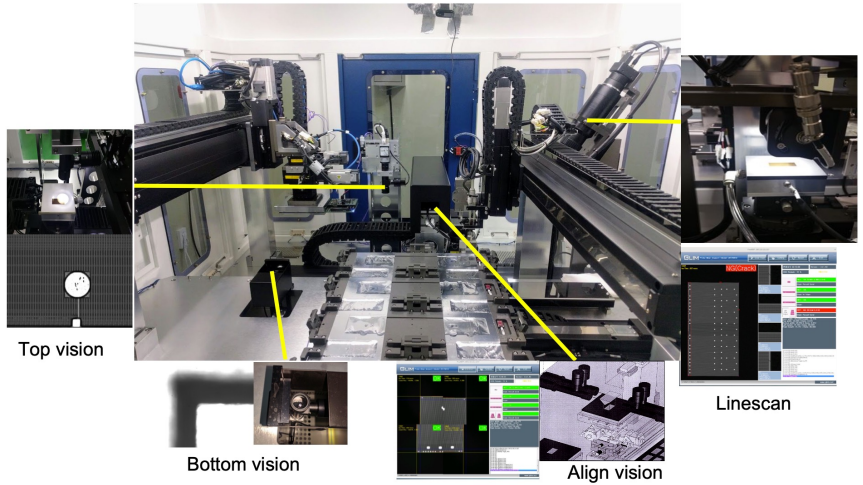


Shipment

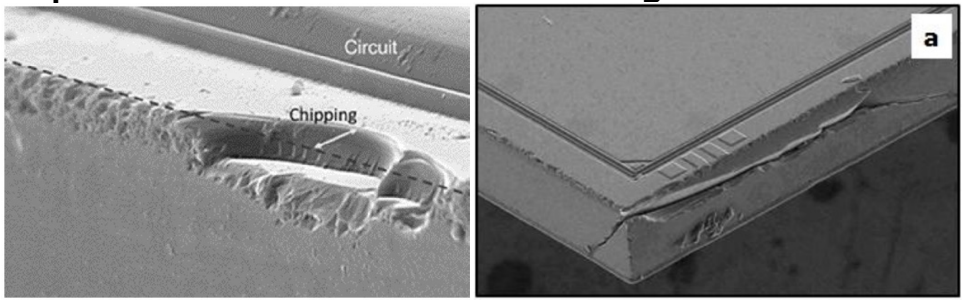
Preparation for development of chip test procedure

- One possible option: chip-level tests with multiple probe cards doing tests in parallel





- It depends on the failure rate from dicing



Chip test machine (ALICE ITS2, ALICIA)