

	Interface Documentation ePIC Barrel ECAL Project		
Project Document No.: epic-bic-xx-XXXX	Institute Document No.: xxx	Created: 11 April 2024 Modified:15th May 2024	Page: I of 44 Rev. No.: 0.1

Interface Documentation

ePIC Barrel ECAL Project

Abstract

This document will cover technical details on the Astropix Modules, AstroPix wafer quality control, End-of-Sector Board (EOSB), and Global Design interfaces.

Prepared by Manoj Jadhav, Please add your name here (title.tex)	Checked by	Approved by
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Distribution List title.tex to edit

History of Changes

<i>Rev. No.</i>	<i>Date</i>	<i>Pages</i>	<i>Description of changes</i>
Draft	11 April 2024	All	Draft
v0.1	11 April 2024	All	created the draft
v0.2	26 April 2024	6-7	Added calculations for Staves

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1 Introduction

The document will provide details on different interfaces for Barrel Imaging Electromagnetic Calorimeter (BIC) at electron-Proton/Ion Collider (ePIC) experiment at the Electron-Ion Collider (EIC). This document will cover technical details on the Astropix Modules, AstroPix wafer quality control, End-of-Sector Board (EOSB), and Global Design interfaces.

Part I

7

Global Design Interfaces

8

2 Global Design

9

Part II

AstroPix Module Interfaces

3 AstroPix Module

The Barrel Electromagnetic Calorimeter comprises two detector technologies: AstroPix, an HV-CMOS MAPS sensor, and Pb/SciFi. The AstroPix sensors are integrated into 4 barrel layers, sandwich between Pb/SciFi layers to construct an imaging part of the barrel ECAL.

The document will provide details on the AstroPix chip, Module design, Module electric schematic, Stave assembly, and interfacing with the end-of-stave FPGA card.

4 AstroPix Chip Specification

AstroPix is a low-power HV-CMOS monolithic active pixel sensor designed with 180 nm CMOS process technology. The AstroPix baseline performance requirements are listed in table 1, comprising effective area, angular resolution, and energy resolution.

Pixel size	$500 \times 500 \mu\text{m}^2$
Chip size	$2 \times 2 \text{ cm}^2$
Power usage	1.5 mW/cm^2
Dynamic range	20keV -700 keV
Energy resolution	5 keV σ @ 122 keV
Time resolution	25 ns
Noise Floor	5 keV
Signal threshold	20 keV

Table 1: The expected specifications of AstroPix readouts.

4.1 AstroPix Version 5

Currently testing AstroPix versions 3 and 4. The specifications of versions 3 and 4 will be added later. Version 5 is under design process and will be available at the beginning of FY2025. The specifications of AstroPix version 5 are listed in table 2.

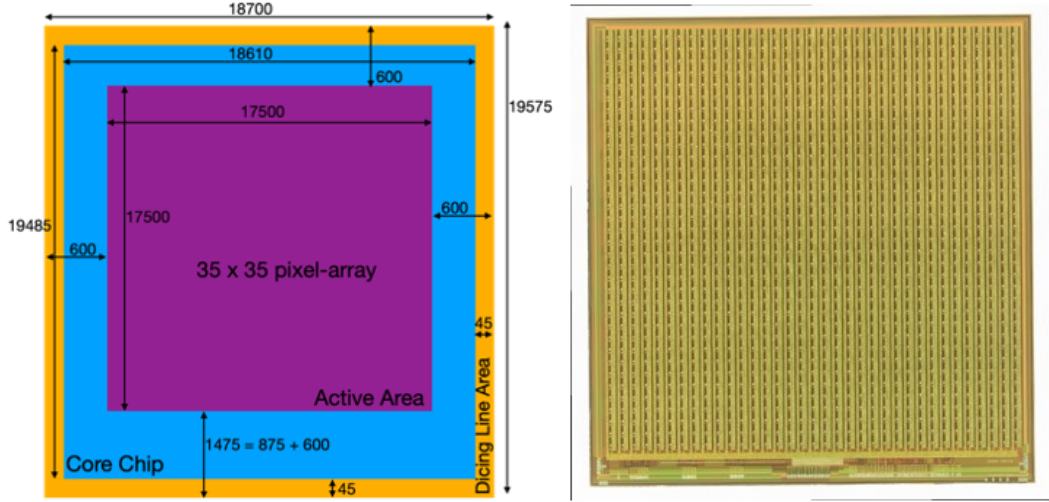


Figure 1: The AstroPix version 3 dimensions (left) and chip image (right). Version 5 dimensions match to the dimensions of version 3.

Pixel Pitch	500 μm (pixel size 300 μm)
Chip size	$1.87 \times 1.96 \text{ cm}^2$
Pixel matrix	35×33
Sensor thickness	525 μm
Power usage	1.63 mW/cm^2
Dynamic range	20keV -700 keV
Energy resolution	5 keV σ @ 122 keV
Time resolution	3.25 ns (25 ns without TDC)
Noise Floor	5 keV
Signal threshold	20 keV
Operating temperature (not tested)	-40 $^{\circ}\text{C}$ /+150 $^{\circ}\text{C}$

Table 2: The specifications of AstroPix version 5.

Analog VDDA	1.8V
Analog VSSA	1.2V
Digital VDDD	1.8V
Analog Ground	GNDA
Digital Ground	GNDD
Sensor Reverse Bias Voltage	0 to 400V

Table 3: External supply voltage required of AstroPix version 5.

4.2 Digital Interface

AstroPix version 5 has pixel-by-pixel readout with 1 Hitbuffer assigned per pixel. Each column has an end-of-column buffer. There are 3 timestamp clocks: 15-bit course TimeStamp at 2.5 MHz, 3-bit fine TimeStamp at 20 MHz, and 16-bit flash TDC, which provides time

response and Time-Over-Threshold resolution of 3.125 ns. The comparator output is con-

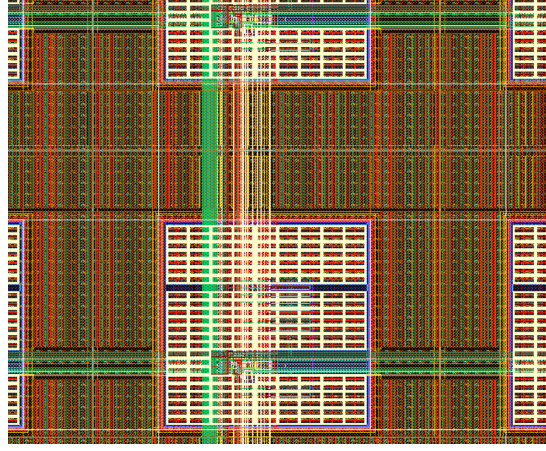


Figure 2: The pixel matrix structure for AstroPix with a pixel pitch of $500\ \mu\text{m}$ and pixel nwell/implant size of $300\ \mu\text{m}$.

31
32 nected to Hitbuffer in the periphery. At the signal's first (falling) edge, coarse and fine
33 TS are saved, and the Flash TDC is started. The TDC measures the exact difference
34 from the falling edge to the next rising edge of the FineTS clk.

35 DaisyChain Protocol

36 The data streaming from End-of-tray-card (EOTC) to AstroPix and AstroPix to EOTC
37 features a Header and Data format. The formats are different in two directions: EOTC to
38 the chip (Module) configures AstroPix chips by writing data and AstroPix chip (Module)
39 to EOTC only defines frames of data passing through the daisy chain with length. The
40 command set is framed by the chip selection, some of the commands can be chained.

41 EOTC to Chip protocol:

42

bits

7	6	5	4	3	2	1	0
Command				Chip Address			

BITS	FIELD	DESCRIPTION
[4:0]	Address	Requires 20 single addresses - 0x00 - 0x14 : Single addresses - 0x15 - 0x1F : Reserved - 0x1D: Invalid - 0x1E: Broadcast
[7:5]	Command	8 Commands: - 0x01 - NOCMD / IDLE - 0x02 - Routing: dispatch addresses - 0x03 - Shift Register Config

IDLE Byte represents no specific command and an invalid address: 0x1D for address and 0x1 for IDLE -> **0x3D**

Figure 3: Hyder Bytes.

COMMAND	NAME	LENGTH	DESCRIPTION
0x01	NOCMD	1 Byte	Nothing to do
0x02	Address Config	1 Byte	Header Address represents the new address of the Chip Chip forwards command to the next chip with Address = Address + 1 To configure Addresses with first Chip "00", send 0x40 to the first Chip, then send some IDLE bytes so that the Clock stays active and the addressing byte gets passed down the <u>chain</u>
0x03	Shift Register Config	N Bytes	Once this command <u>is send</u> , the whole SPI Frame is used - SPI Chip Select must be <u>deasserted</u> and reasserted to send a new <u>command</u>

Figure 4: Commands to AstroPix Chip.

Chip to EOTC protocol:

bits

7	6	5	4	3	2	1	0
Chip Address					Payload Length		

- Chip Address is the Configured Chip ID using the routing byte
- The PayloadLength is the number of bytes trailing the header

Hit Packet Type

At the moment we only need 1 Packet type:

bytes

0	1	2	3	4	5	6	7
Header	Row<0:5> ,Col<0:1>	Col<2:5> ,TSFromDet<0:3>	TSFromDet<4:11>	TSFromDet<12:14>,TSFromDet2<0:4>	TSFromDet2<5:12>	TSFromDet2<13:14>,TSFine<0:2>,TSFine<0:2>	TSTDC1<0:3>, TSTDC2<0:3>

Figure 5: Data Format from the Chip.

44

45 AstroPix version 5 will have 1x8 Bytes. Right now, they can be reduced by on-chip
46 subtraction. As shown in figure 5 the data bytes can be decoded as,

47 8b Header,

48 6b Row,

49 6b Col,

50 15b TS,

51 $15b + 2 \times (4b + 3b)$ ToT.

52

53 4.3 Digitization Data Rate

54 The whole Chip triggers at 10Hz. Only one counter per row/column with 8 Bytes. With
55 Chip array of 36×36 and $500 \mu\text{m}$ Pixels there are around 1300 Pixels.

56 $1300 * 8 \text{ Bytes Data} = 10400 \text{ Bytes}$

57 Protocol including daisy chain etc.. = 50% overhead i.e. +5200 Bytes

58 Total = 15600 Bytes /s / chip

59 Pixelator: 1 Chip, Full Module with 9 chips = $9 * \text{Pixelator} = 9 \text{ Chips}$

60 For one Module: $9 \times 15600 = 140 \text{ kByte/s}$

The maximum expected rate for Barrel Ecal using the following table 4: 61
 Avg hit rate/pixel [1/s] is 5.68E-02, so for a chip it is 70 hits and for a Module it is 840 62
 Considering double the hits per module, it is 1680 63
 The expected data rate for a Module is 1680*8 bytes = 13.44 kBytes/s. 64

Data rate for Barrel ECAL 65

Integration time [s]	6.00E-06
Nb of pixels	5.28E+08
Total rate [1/s]	3.00E+07
Avg hit rate/pixel [1/s]	5.68E-02
Propability of getting hit twice	1.94E-08
Propability of getting hit twice for entire detector	1.02E+01
Drop rate for the entire detector	3.41E-07
Nb of hits with one drop	2.93E+06

Table 4: Data hit rate

The expected hit rate for all imaging layers together Low rates is well below < 30 66
 MHz 67
 This translates to a maximum hit rate per tracker stave (1 x 108) < 36 kHz 68

This draft will also add more information about module design, electrical interface 70
 and power numbers. This information can temporarily be accessed at link here 71

4.4 AstroPix Chip Final Dimensions 72

Final size of the AstroPix chip reticle will be 2 cm × 2 cm. It will have pixel-by-pixel 73
 flash-TDC to provide fast time response with individual tune-DAC for the pixel tuning. 74
 Table 5 provide details of physical dimensions of AstroPix chip considered for the imaging 75
 layers of Barrel Electromagnetic Calorimeter at the ePIC. 76

Final chip size	2 cm × 2 cm ²
Pixel Pitch	500 μm (pixel size 300 μm)
Pixel matrix	39 × 37
Sensor thickness	525 μm
Dicing line clearance	45 μm
Pixel to chip edge distance	205 μm

Table 5: Physical dimensions of final AstroPix chip.

77 This dimension provides full coverage along the stave length spanning the length of
 78 218.16 using 12 modules with 9 chips each. The current AstroPix dimension is shorter
 79 than final dimensions and hence requires a design respin after version 5 has been tested.

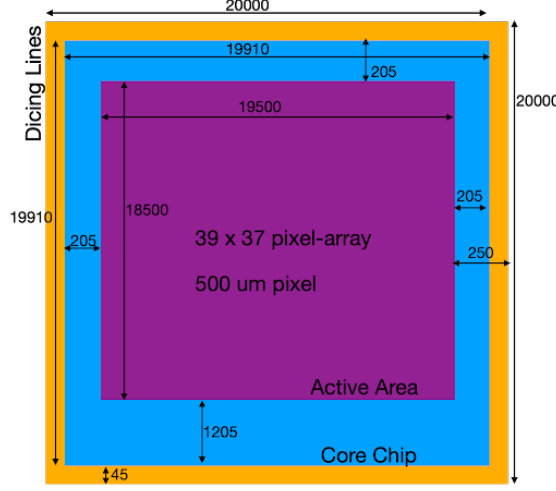


Figure 6: The AstroPix final dimensions.

80 Each module will have 9 chips with intermediate gap of $200 \mu\text{m}$. The module length
 81 is 18.11 cm with full stave length is 218.16 cm. The number of chips and modules are
 82 calculated by following consideration,

83

84 Total BIC length = 440 cm

85 Length to cover with single stave = 220 cm

86 AstroPix size + gap = 2.02 cm

87 Number of chips required = $220/2.02 = 108.91$

88 Round of number for required chips = 108 chips/stave

89 Which leads to 9 chips and 12 modules

90

91 The next section will describe Mechanical considerations of the module and stave
 92 designs.

93 5 Mechanical Structure Design

94 The imaging part of calorimetry has 4 layers of low-power HV-CMOS MAPS sensors,
 95 AstroPix. Layer numbers 1, 3, 4, and 6 will be integrated with AstroPix chips.

96 5.1 Total Active Area Calculations

97 This section calculates the active area on the Tray (along with the length and width).

5.1.1 Along the Tray length

Along the stave, we have a 20 mm AstroPix chip with an in-between gap of 0.2 mm (0.1 mm to stay within 435 cm). The active length on the chip is 19.5 mm (39 pixels).

0.2 mm gap between adjacent chips -

Length of the Stave = $20.2 \times 108 = 2181.6 \text{ mm} = 218.16 \text{ cm}$

Length of the Calorimeter = $2 \times 2181.6 \text{ mm} = 4363.2 \text{ mm} = 436.32 \text{ cm}$

Active chip array length = 19.5 mm

Inactive area on chip = 0.5 mm

Inactive area in-between two chips = 0.2 mm

Active area percentage = Active area / Total detector area = $19.5/20.2 = 96.53\%$

Inactive area percentage = $0.7/20.2 = 3.47\%$.

0.1 mm gap between adjacent chips -

Length of the Stave = $20.1 \times 108 = 2170.8 \text{ mm} = 217.08 \text{ cm}$

Length of the Calorimeter = $2 \times 2170.8 \text{ mm} = 4341.6 \text{ mm} = 434.16 \text{ cm}$

Active chip array length = 19.5 mm

Inactive area on chip = 0.5 mm

Inactive area in-between two chips = 0.1 mm

Active area percentage = Active area / Total detector area = $19.5/20.1 = 97.01\%$

Inactive area percentage = $0.6/20.2 = 2.97\%$.

5.1.2 Along the Tray width

In this direction, the chip and module will have considerable inactive areas. The calculation below provides numbers to minimize the dead area in this direction.

Active chip array length = 18.5 mm

Inactive area on top side = 0.25 mm

The inactive area on the bottom side (digital periphery) = 1.25 mm

Total inactive area on chip = 1.5 mm

The inactive area on the Module at the top of the chip = 0 mm

The inactive area on the Module at the bottom of the chip = 0 mm

Module flex will carry the bus bar (data and power lines) as well as power regulation circuitry.

Unavoidable dead area at top = Dead area on the (Chip + Module) = $0.25 + 0.0 \text{ mm}$.

Total unavoidable dead area = 0.5 mm. (Keeping top side outward on each sidewall)

134
135 There will be 4 Imaging layers in the Barrel Electromagnetic Calorimeter (BIC). Ap-
136 pendix **xx** provides design geometry for the BIC Sector.

137
138 Available space for imaging layers is,

139 Layer 1: 107.257 mm

140 Layer 3: 117.411 mm

141 Layer 4: 122.488 mm

142 Layer 6: 132.642 mm

143
144 Targeting minimum dead space in the detector acceptance region, the stave at one end
145 of the Tray will be flipped to align the minimum inactive area edge of the chip with the
146 side wall.

147 The calculation shows the number of staves required to cover Tray with the minimum
148 inactive area possible.

149
150 **The AstroPix detector Staves are arranged to provide maximum active area**
151 **along the beam direction and in a barrel region.**

152
153 **Layer 1: 107.257 mm**
154 Number of Staves = $(107.257-0.5)/18.5 = 106.757/18.5 = 5.77 \rightarrow \mathbf{6 \text{ Staves}}$
155 Total active length available = $18.5*6 = 111 \text{ mm}$
156 Additional **overlap** needed to fit 6 Chips (in addition to 1.25 mm at the bottom and 0.25
157 at the top) = $111 - 106.757 = 4.243 \text{ mm}$
158 Additional overlap per Stave = $4.243/6 = 0.707 \text{ mm}$

159
160 **Total dead area percentage = $0.5/107.257 = 0.47\%$**

161
162 **Layer 3: 117.411 mm**
163 Number of Staves = $(117.411-0.5)/18.5 = 116.911/18.5 = 6.3195 \rightarrow \mathbf{6 \text{ Staves or } 7}$
164 **Staves?**

165
166 **- 6 Staves:**
167 Total active length available = $18.5*6 = 111 \text{ mm}$
168 Additional **dead** space = $116.911 - 111 = 5.911 \text{ mm}$
169 Additional dead area per Stave = $5.911/6 = 0.9852 \text{ mm}$

170

$$\text{Total dead area percentage} = (5.911+0.5)/117.411 = 5.46\%$$

- 7 Staves:

$$\text{Total active length can be available} = 18.5*7 = 129.5 \text{ mm}$$

$$\text{Additional overlap needed to fit 7 Chips} = 129.5 - 116.911 = 12.589 \text{ mm}$$

$$\text{Additional overlap per Stave} = 12.589/7 = 1.7984 \text{ mm}$$

$$\text{Total dead area percentage} = 0.5/117.411 = 0.43\%$$

Layer 4: 122.488 cm

$$\text{Number of Staves} = (122.488-0.5)/18.5 = 121.988/18.5 = 6.5939 \rightarrow \text{6 or 7 Staves?}$$

- 6 Staves:

$$\text{Total active length can be available} = 18.5*6 = 111 \text{ mm}$$

$$\text{Additional dead space} = 121.988 - 111 = 10.988 \text{ mm}$$

$$\text{Additional dead area per Stave} = 10.988/6 = 1.831 \text{ mm}$$

$$\text{Total dead area percentage} = (10.988+0.5)/122.488 = 9.38\%$$

- 7 Staves:

$$\text{Total active length can be available} = 18.5*7 = 129.5 \text{ mm}$$

$$\text{Additional overlap needed to fit 7 Chips} = 129.5 - 121.988 = 7.512 \text{ mm}$$

$$\text{Additional overlap per Stave} = 7.512/7 = 1.073 \text{ mm}$$

$$\text{Total dead area percentage} = 0.5/12.2488 = 0.41\%$$

Layer 6: 132.642 mm

$$\text{Number of Staves} = (132.642-0.5)/18.5 = 132.142/18.5 = 7.1428 \rightarrow \text{7 Staves or 8 Staves?}$$

- 7 Staves:

$$\text{Total active length available} = 18.5*7 = 129.5 \text{ mm}$$

$$\text{Additional dead space} = 132.142 - 129.5 = 2.642 \text{ mm}$$

$$\text{Additional dead area per Stave} = 2.642/7 = 0.3774 \text{ mm}$$

$$\text{Total dead area percentage} = (2.642+0.5)/132.642 = 2.37\%$$

208 - 8 Staves:

209 Total active length can be available = $18.5 \times 8 = 148$ mm

210 Additional **overlap** needed to fit 8 Chips = $148 - 132.142 = 15.858$ mm

211 Additional overlap per Stave = $15.858/8 = 1.982$ mm

212

213 **Total dead area percentage = $0.5/132.642 = 0.38\%$**

Table 6: Summary of AstroPix coverage (layer 6 - 7 Staves).

Layer#	Length (mm)	# Staves	Overlap or Inactive (mm)	Overlap/Inactive per Stave (mm)	Overlap/Inactive per Gap (mm)	Inactive (%)
1	107.257	6	4.243	0.707	0.8486	0.47
3	117.411	7	12.589	1.7984	2.0982	0.43
4	122.488	7	7.512	1.073	1.252	0.41
6	132.642	7	2.642	0.3774	0.4403	2.37

Table 7: Summary of AstroPix coverage (layer 6 - 8 Staves).

Layer#	Length (mm)	# Staves	Overlap or Inactive (mm)	Overlap/Inactive per Stave (mm)	Overlap/Inactive per Gap (mm)	Inactive (%)
1	107.257	6	4.243	0.707	0.8486	0.47
3	117.411	7	12.589	1.7984	2.0982	0.43
4	122.488	7	7.512	1.073	1.252	0.41
6	132.642	8	15.858	1.982	2.2654	0.38

214

Table 8: Summary of AstroPix all coverage calculations.

Layer#	Length (mm)	No. of Staves	Inactive (mm)	Overlap (mm)	Overlap or Inactive per Stave (mm)	Total Inactive (%)
1	107.257	6	-	4.243	0.707	0.47
3	117.411	6	5.911	-	0.9852	5.46
		7	-	12.589	1.7984	0.43
4	122.488	6	10.988	-	1.831	9.38
		7	-	7.512	1.073	0.41
6	132.642	7	2.642	-	0.3774	2.37
		8	-	15.858	1.982	0.38

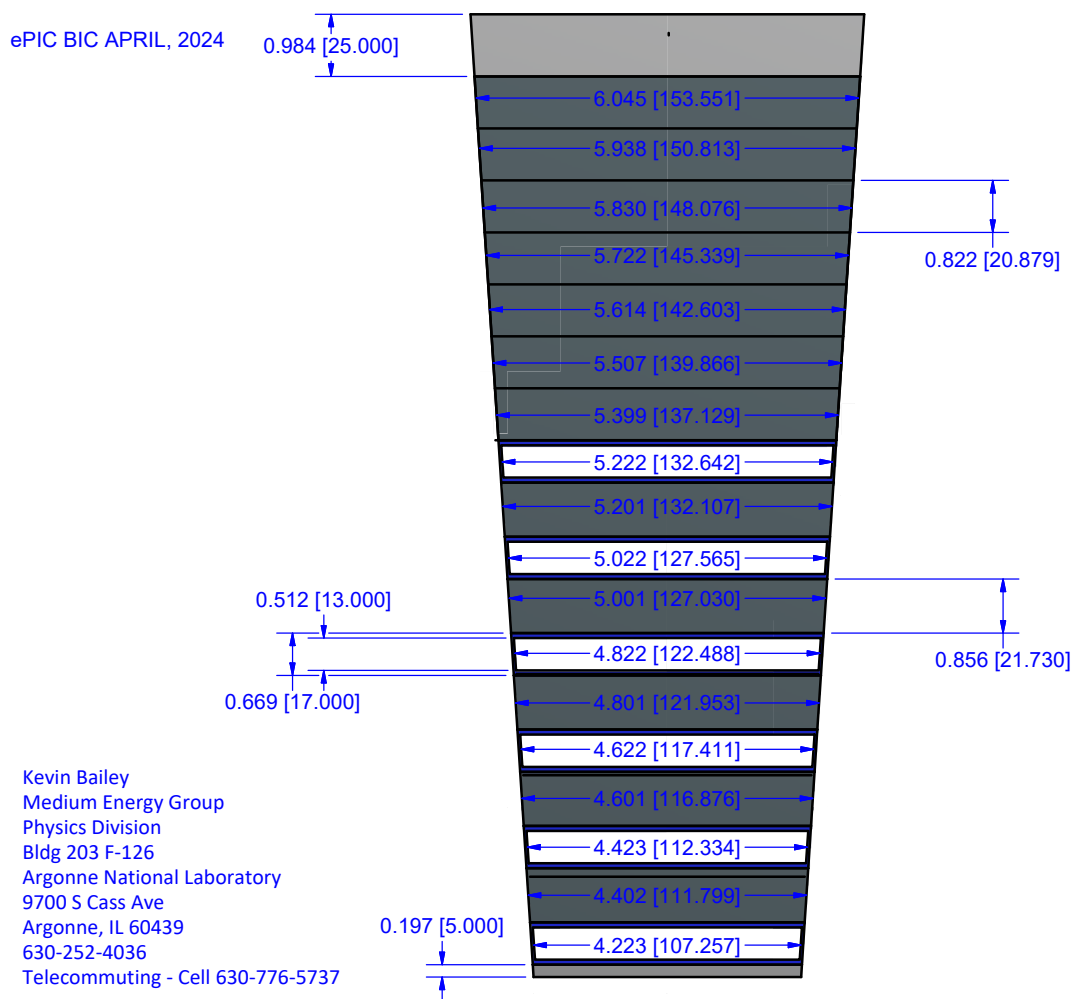
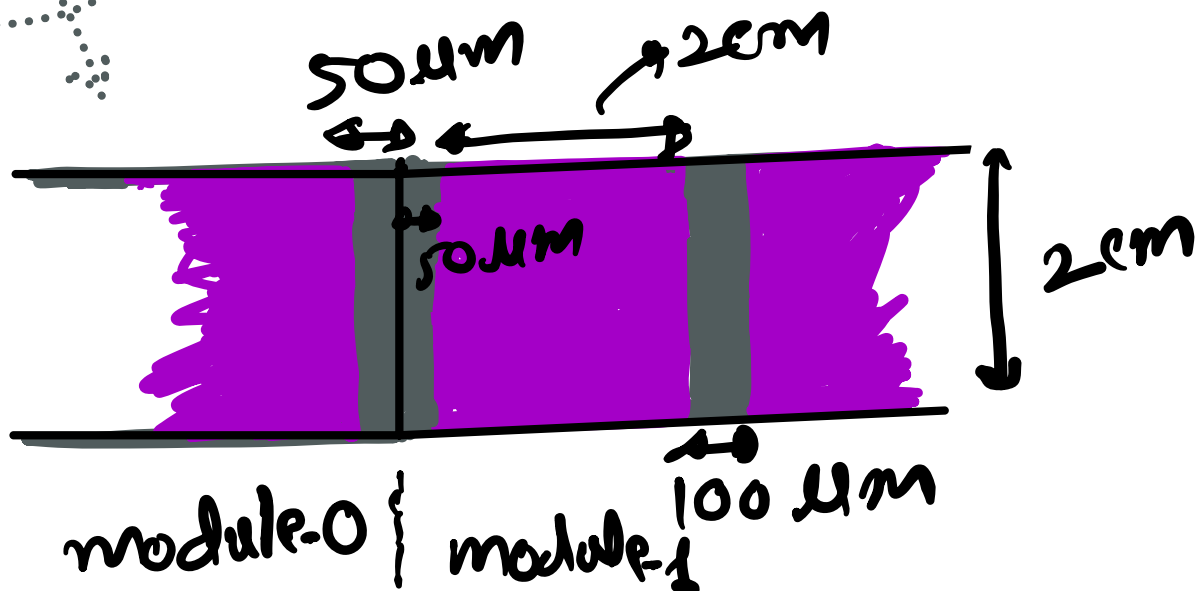
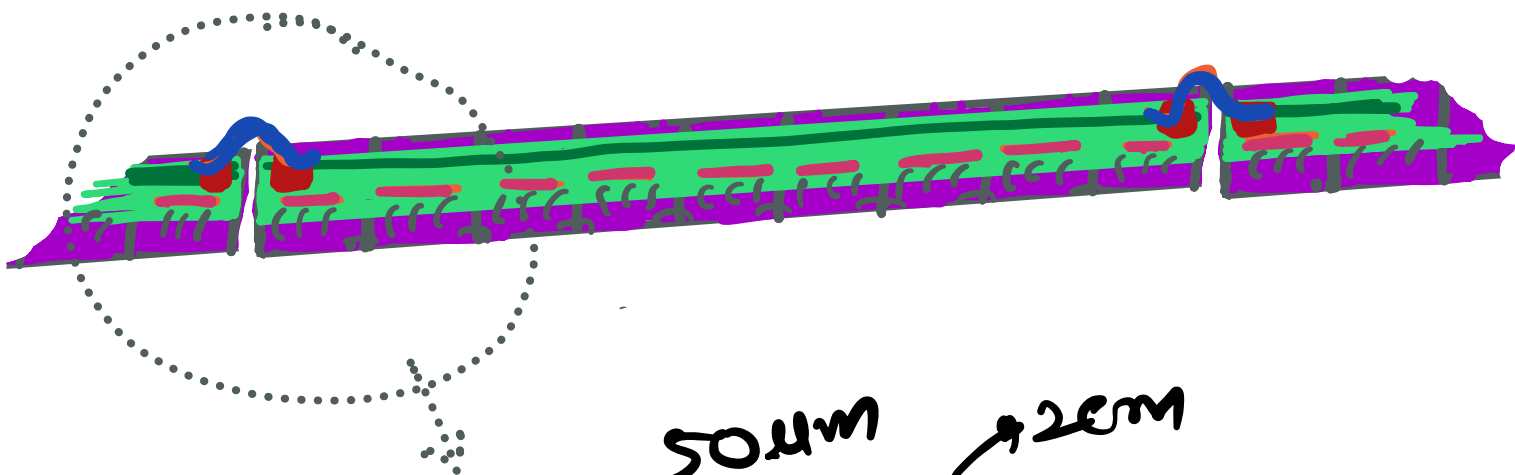
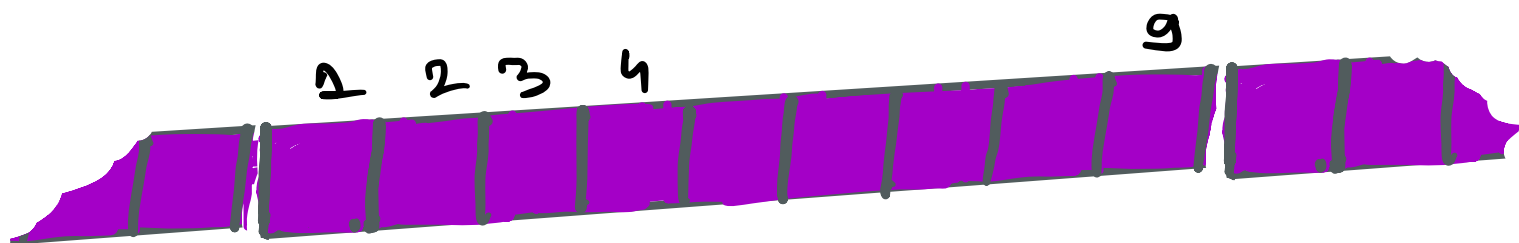
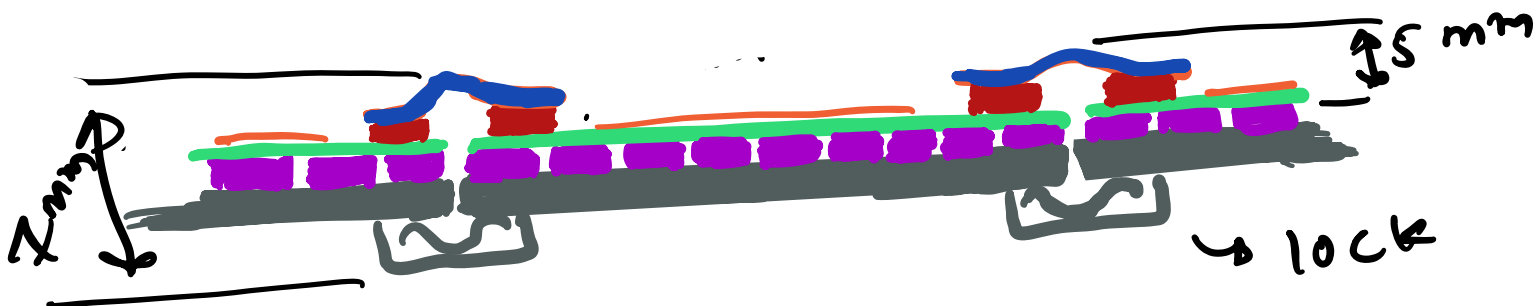
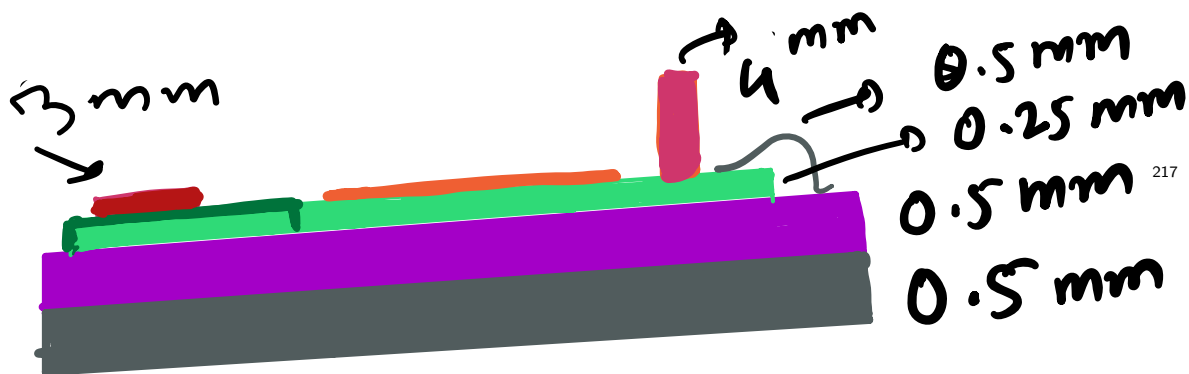


Figure 7: AstroPix Tray envelope for BIC layers.

②



AstroPix chip - $2\text{ cm} \times 2\text{ cm}$ (0.5 mm)

AI module carrier (0.5 mm)

width $\rightarrow 2\text{ cm}$

length $2.01 \times 9 = 18.09\text{ cm}$

[will have some locking system
on back - 1 mm height]

Flex Bus bar / PCB (0.25 mm)

width $\rightarrow 18.5\text{ mm}$

length $\rightarrow 18.09\text{ cm}$

$\rightarrow$ Bus Bar / power-data lines

width $\rightarrow 8.5\text{ mm}$

$\rightarrow$ Bus Bar PCB
Power Regulation (LDO)
4 traces to wirebond

width $\rightarrow 10\text{ mm}$

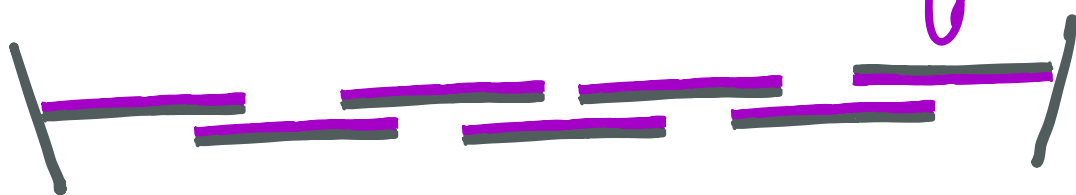
→ module-to-module connector (3 mm)

- module to module Pigtail (1.75 mm)

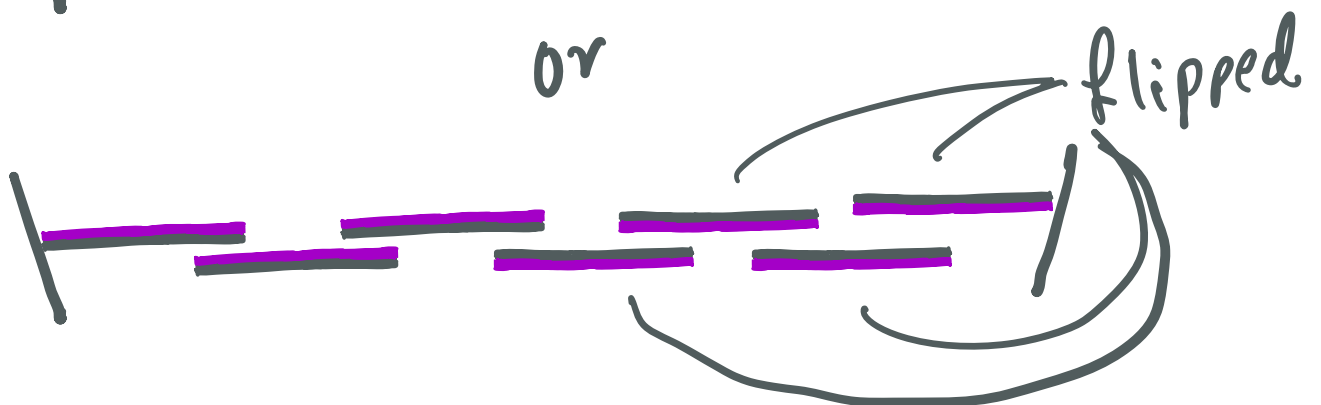
→ wirebond protector (4 mm)

layer-1 (107.257 mm)

8 staves



or



AstroPix Module Interfaces

220

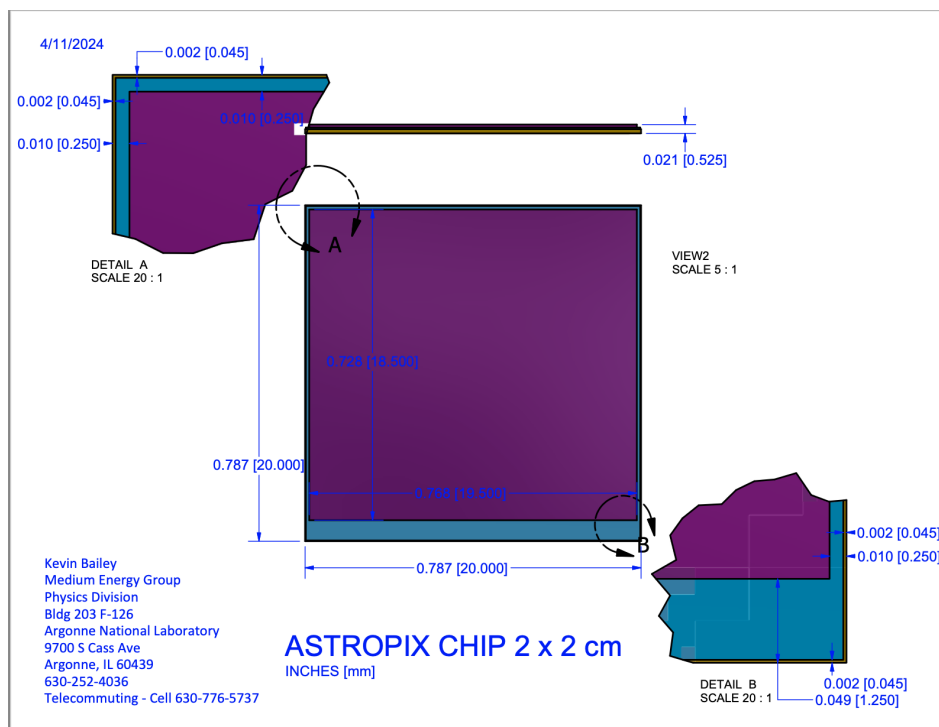
Module Mechanical Design:

The imaging part of calorimetry has 4 layers of low-power HV-CMOS MAPS sensors, AstroPix. Layer numbers 1, 3, 4, and 6 will be integrated with AstroPix chips

- ~ 2 cm x 2 cm chip area
- 100 μ m gap between two chips
- 9 chips per module
- 12 modules per stave
- 6 or 7 staves per tray
- 12 or 14 staves per layer (first 3 layers have 12 staves and 4th have 14 staves)
- 54 staves per sector
- Total 48 sectors
- Total number of AstroPix chips = $9 \times 12 \times 54 \times 48 = 279936$

BaseLine Detector Coverage

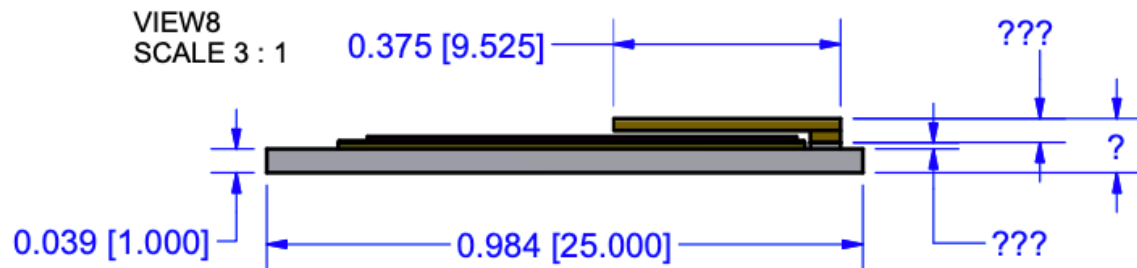
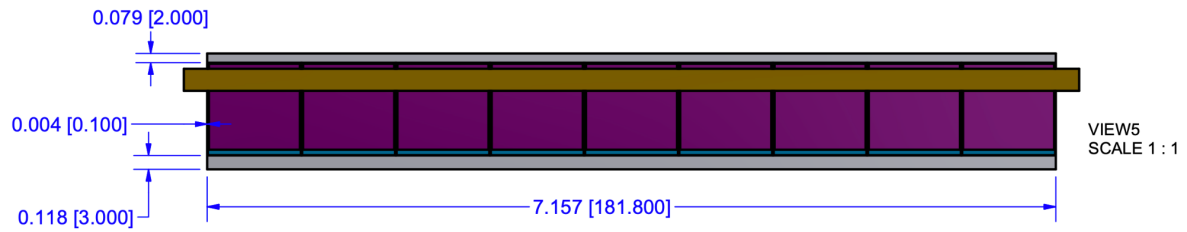
- New baseline module layout: 12 modules of 9 chips
- Length assuming 100 μ m gap and 2cm chips: $2.01 \text{ cm} \times 12 \times 9 \times 2 = 434.16 \text{ cm}$
- Sector length:
 - 434.16 cm (no longer than 440 cm as the upper limit)
- End-of-sector box length:
 - 15 cm (keep at least 2 cm reserved for connectors)



AstroPix Module Interfaces

221

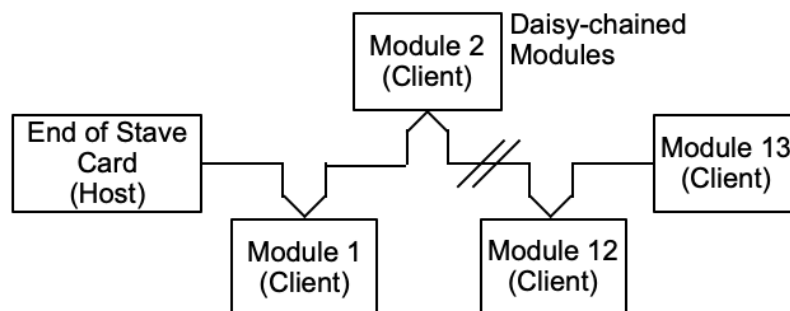
Initial Module Design



Stave length



Electrical Interfaces:



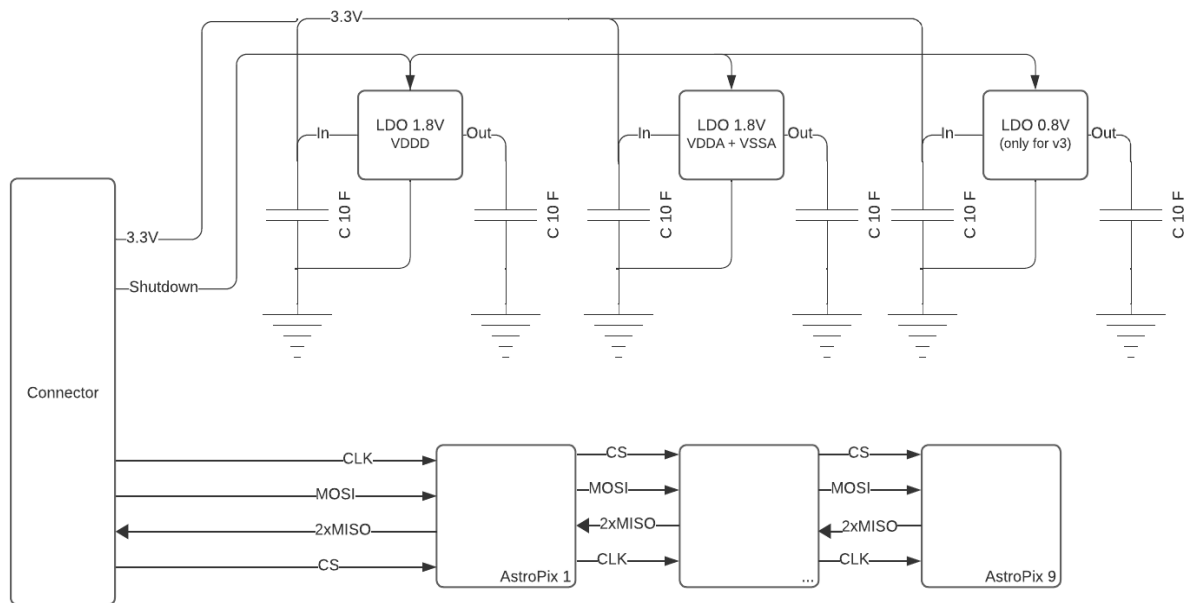
- Daisy Chain on the Module and Module will directly take command and stream data to EOSC
- What are our options?
 - Differential SPI (KIT confirmed - ePIC meeting)
 - Multi-drop data transmission using flex bus

AstroPix Module Interfaces

222

- Power distribution on bus bar or cable harness
- Daisy-chained chips on the module will be parallel to chips on other modules.
- Host End-of-Stave will connect to Client Modules through a daisy-chain (LVDS on Modules)
- Module enable control
 - Allows to control Module operation individually
 - This will allow to save stave by switching off bad Module

Electric Block Diagram for Module



LDOs

LT3041, LT3097, or LT3045

Connectors

Right angle connectors:

the Samtec connector series Edgerate (ERM8), Razor Beam(LSHM), or the TigerEye series

Vertical Connectors:

- Need inputs

[AstroPixModule](#) datasheets of LDOs and Connectors.

AstroPix Module Interfaces

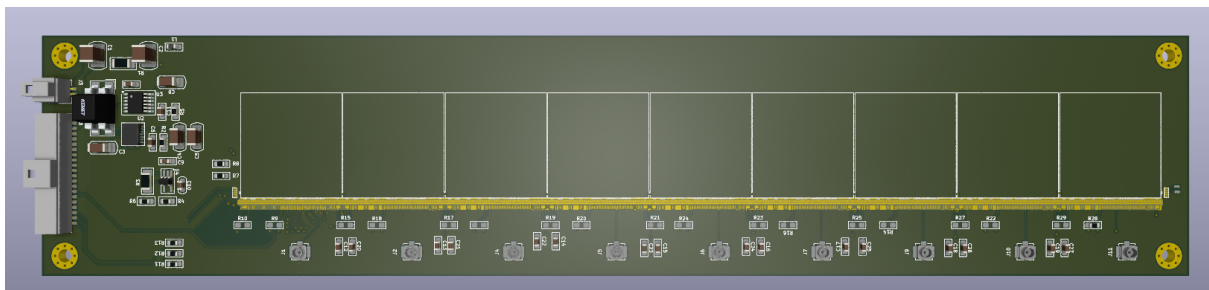
Bus Bar and Cable Harness:

- Pending

223

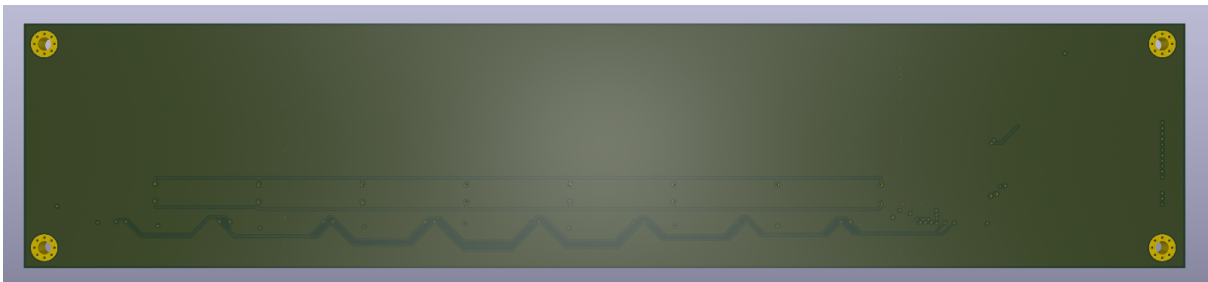
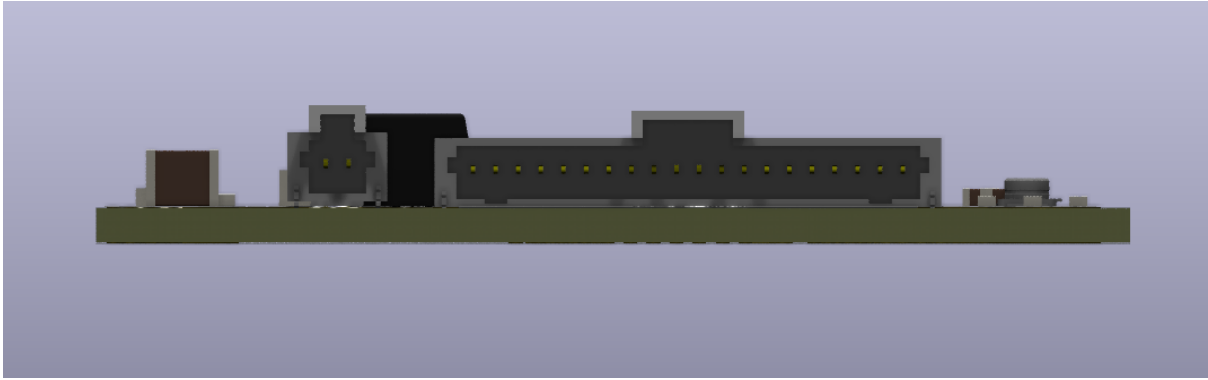
PCB board design:

Module PCB Test Board -



AstroPix Module Interfaces

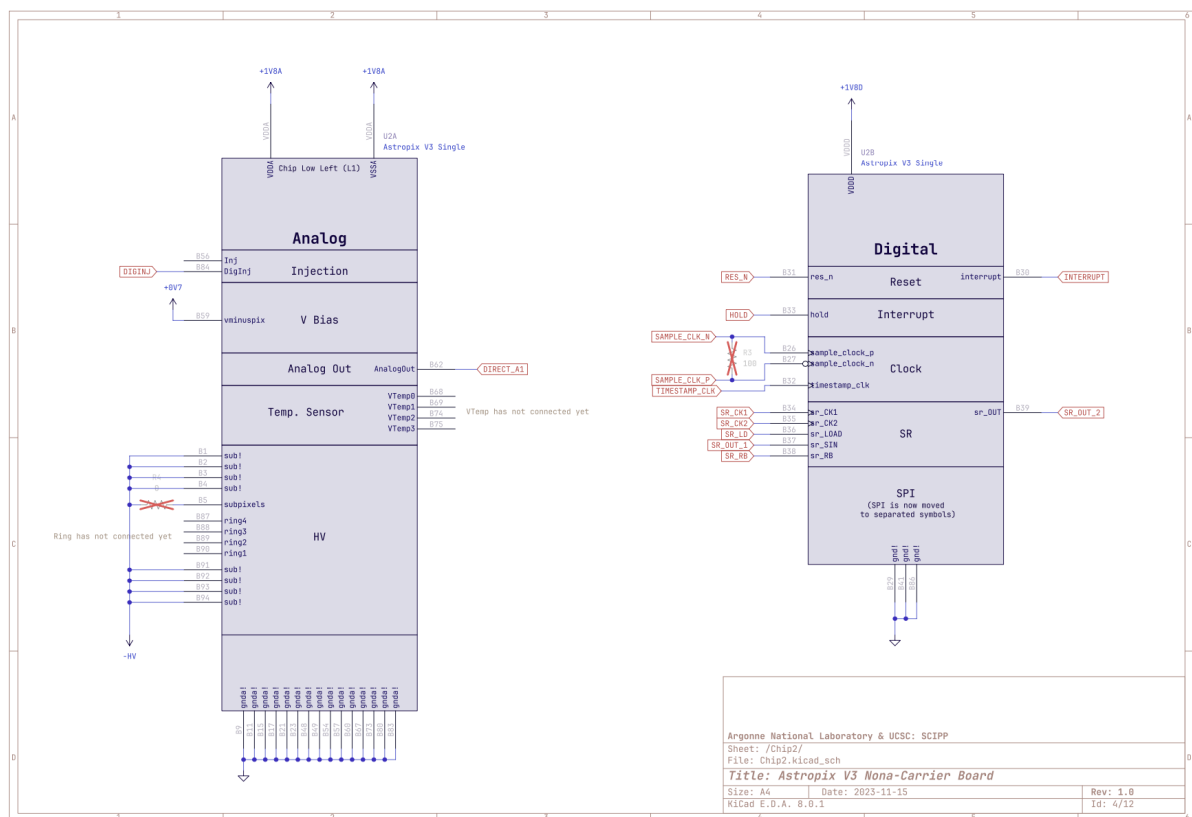
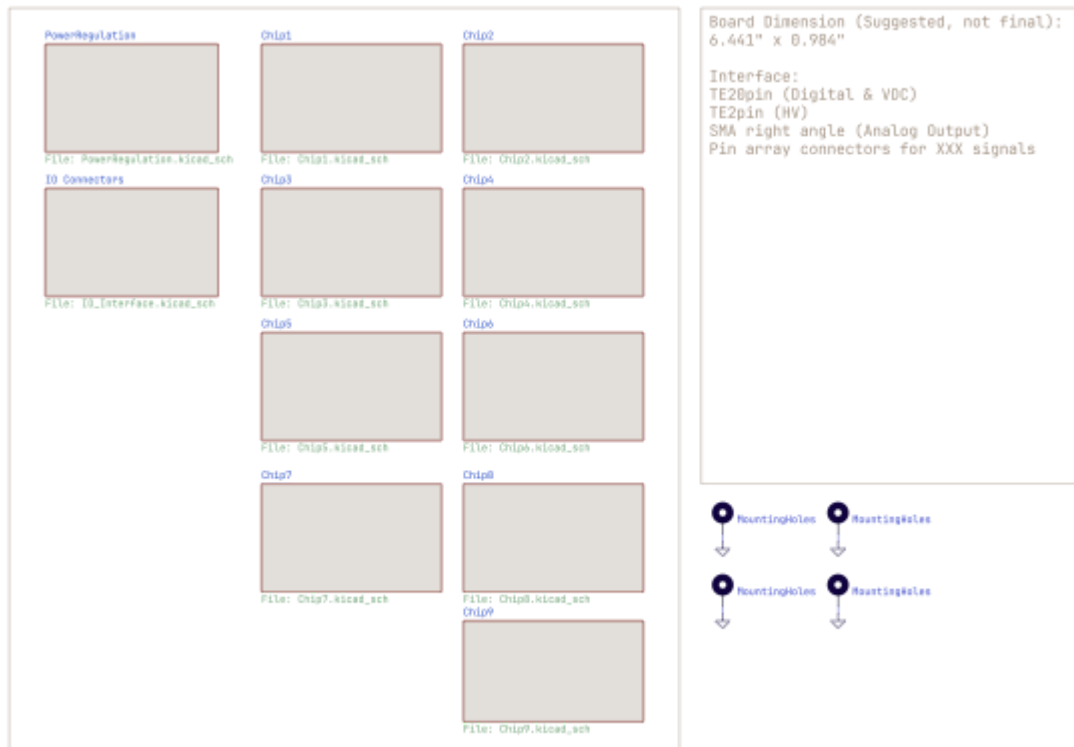
224



AstroPix Module Interfaces

Module PCB Schematic

225

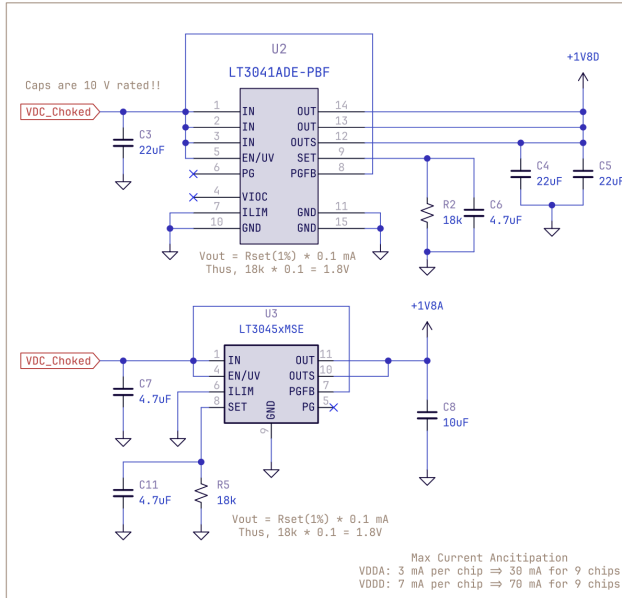


AstroPix Module Interfaces

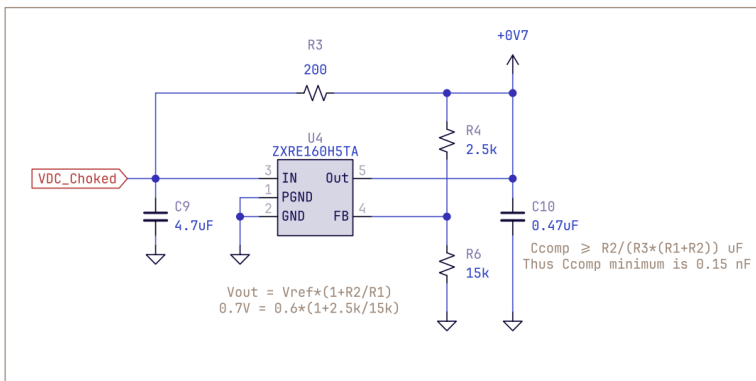
226

Voltage regulators for VDDD and VDDA

- LT3041ADE and LT3045xMSE



Voltage Regulator for Vminuspix 0.7V - will be removed in next iteration



Pin Outs

AstroPix Module Interfaces

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Usage	V3	V-final
Power	HVin	HVin
	GND	GND
	VDCIN	VDCIN
SPI	MISO0	MISO0
	MISO1	MISO1
	CSN	CSN
	CLK	CLK
	MOSI	MOSI
Sample Clk	SAMPLE_CLK_P	SAMPLE_CLK_P
	SAMPLE_CLK_N	SAMPLE_CLK_N
Shift Register	SR_Ck1	
	SR_Ck2	
	SR_LD	
	SR_SIN	
	SR_RB	
	SR_OUT	
Other	DIGINJ	
	INTERRUPT	
	TIMESTAMP_CLK	TIMESTAMP_CLK
	Hold	
	RES_N	

AstroPix Power Consumption:

AstroPix v3	1.87cm x	3.66 cm2			
--------------------	----------	----------	--	--	--

AstroPix Module Interfaces

228

	1.95cm					
	Per Chip					
Supply	Voltage (V)	Current (mA)	Power (mW)	Power (mW/cm ²)	Power per Module (mW)	Power per Stave (mW)
VDDA Analog	1.8	1.47	2.65	0.72	23.85	286.2
VSSA Analog	1.2	1.33	1.6	0.44	14.4	172.8
VDDD Digital	1.8	6.88	12.24	3.34	110.16	1321.92
		Total	16.49	4.51	148.41	1780.92
AstroPix v final	2cm x 2cm	4 cm ²				
(expected)	Per Chip					
Supply	Voltage (V)	Current (mA)	Power (mW)	Power (mW/cm ²)	Power per Module (mW)	Power per Stave (mW)
VDDA Analog	1.8	2.4	4.32	1.08	38.88	466.56
VSSA Analog	1.2	0	0	0	0	0
VDDD Digital	1.8	1.67	3	0.75	27	324
		Total	7.32	<1.83	65.88	790.56

6	Electrical Interfaces	229
6.1	Electric Block Diagram of Module	230
6.2	Flex PCB	231
6.3	Power Regulation	232
6.4	PCB Module Test Board v1 Design	233
6.5	AstroPix Power Consumption	234

235 **Part III**

236 **End-Of-Sector Board (EOSB)**

237 **Interfaces**

238 **7 EOSB**

Part IV	239
AstroPix Wafer Quality Control	240
8 AstroPix Wafers	241

242 **Part V**

243 **Appendices**

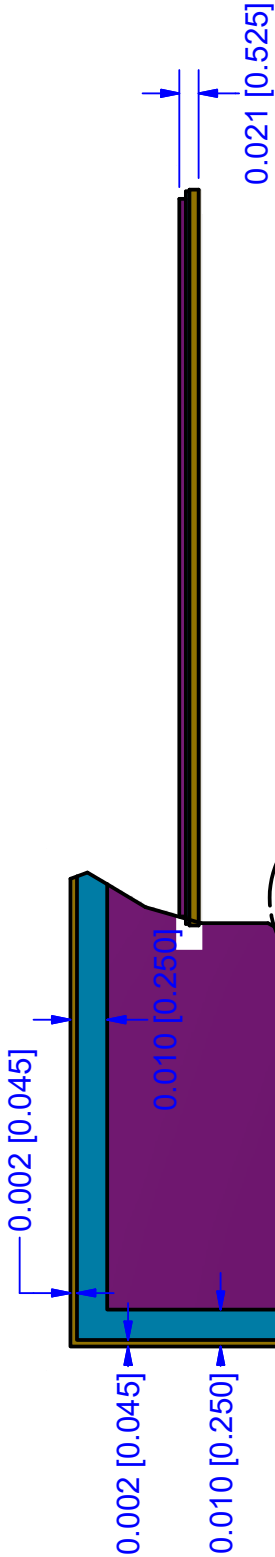
244 **A Global Design Interfaces**

245 **A.1 Starts with subsection**

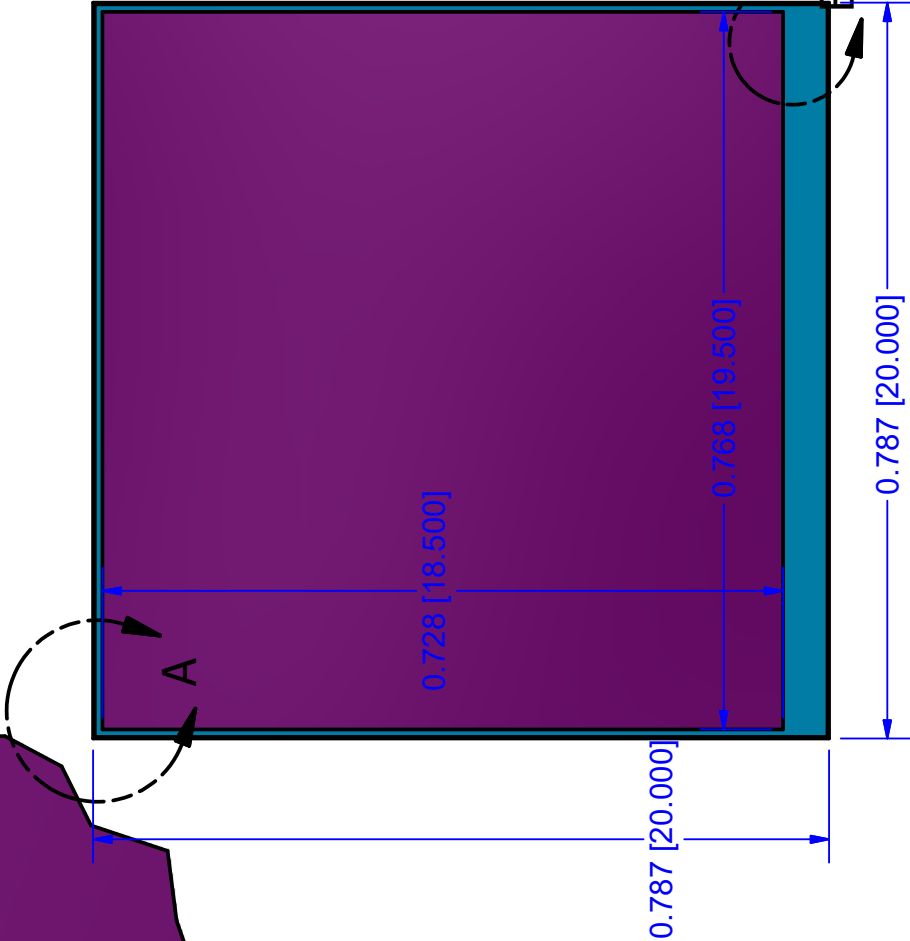
246 **B AstroPix Module Interfaces**

247 **B.1 AstroPix Module Design CAD Drawings**

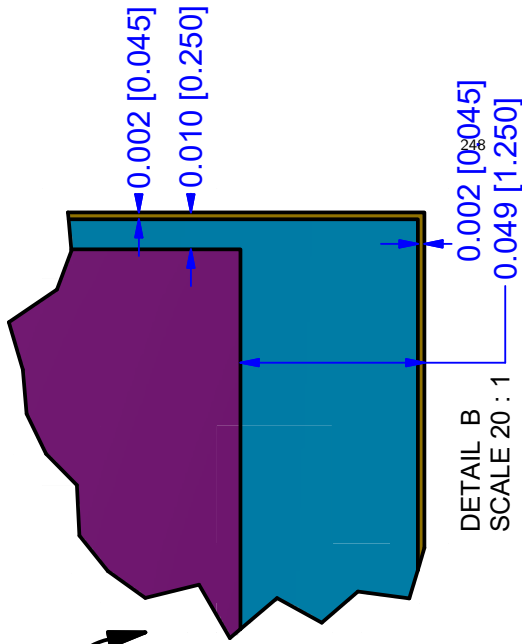
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DETAIL A
SCALE 20 : 1



VIEW2
SCALE 5 : 1

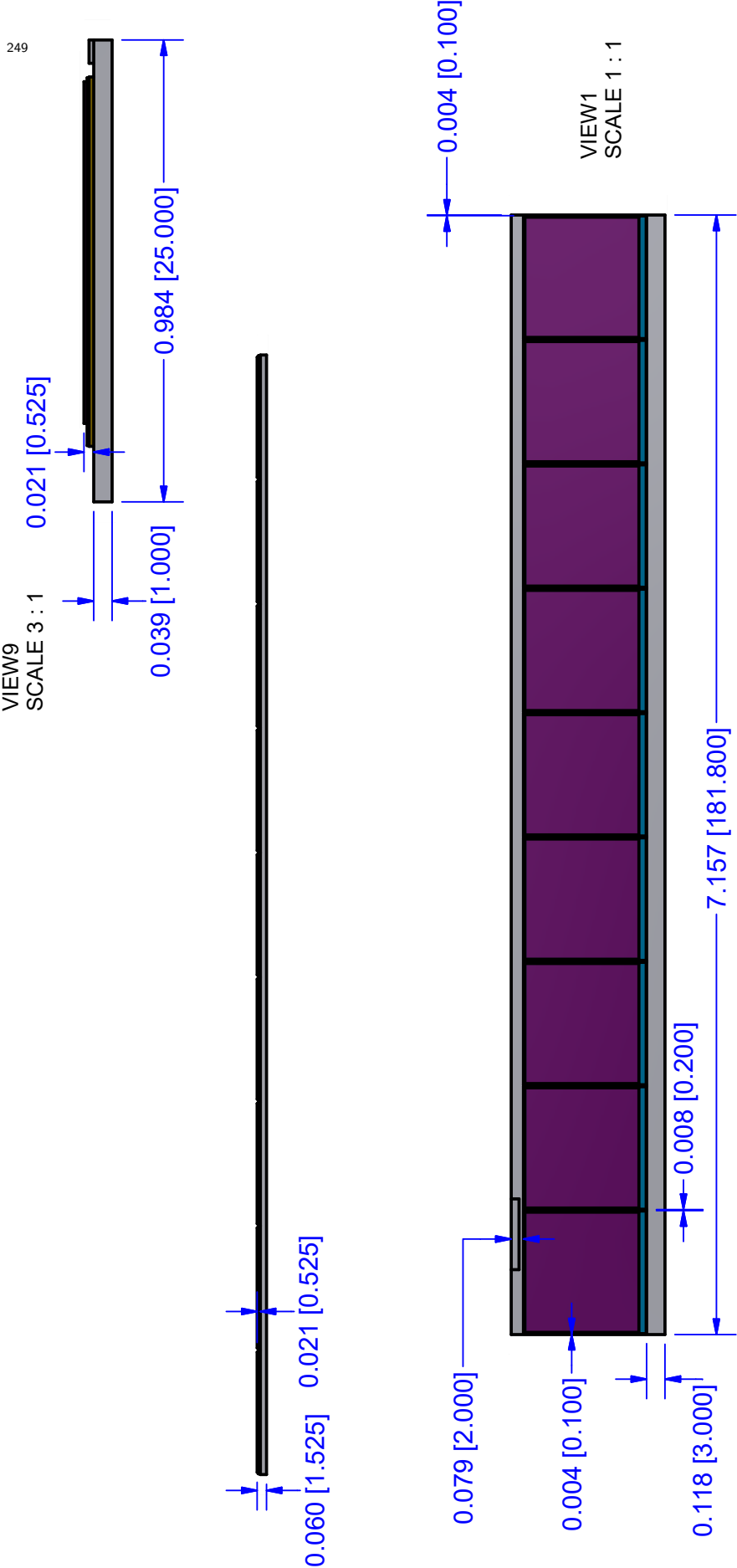


DETAIL B
SCALE 20 : 1

ASTROPIX CHIP 2 x 2 cm

INCHES [mm]

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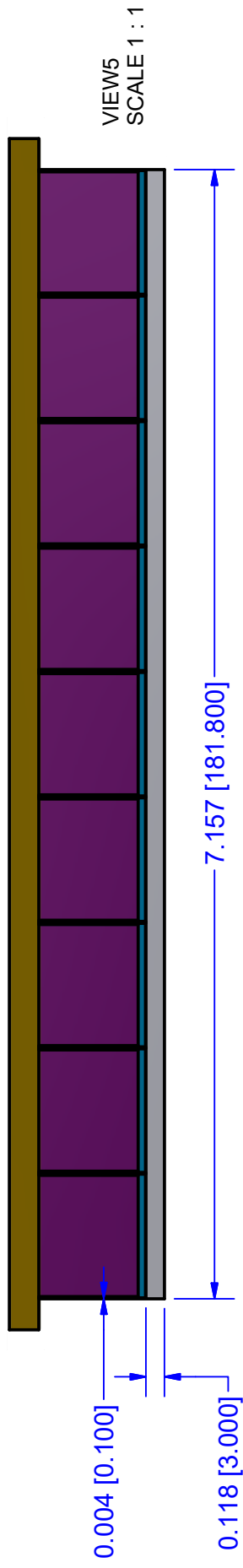
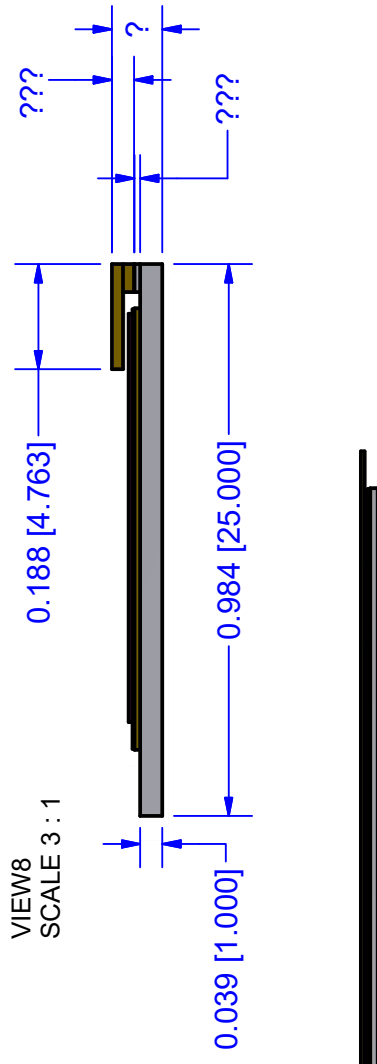


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ASTROPIX 2 x 2 cm W/O BUS TAPE

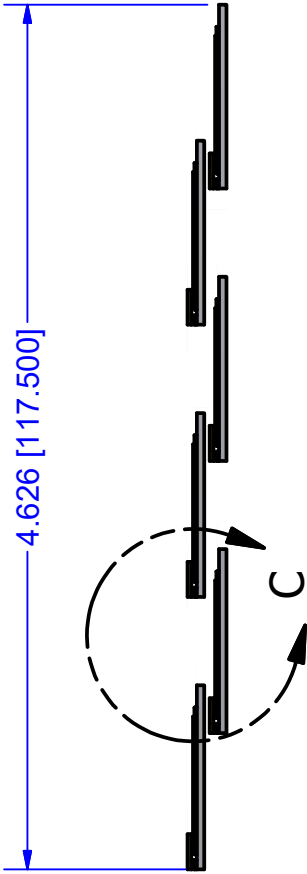
INCHES [mm]

APRIL 23 2024

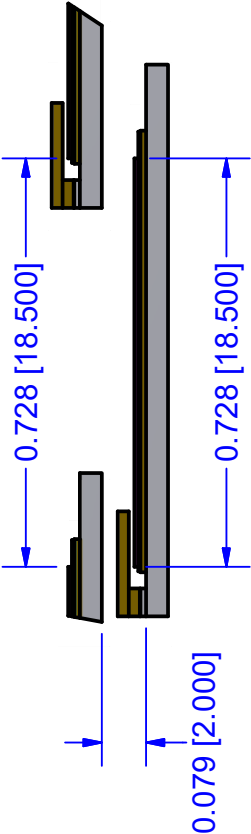


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ASTROPIX 2 x 2cm W/ BUS TAPE



SIX MODULES WIDE

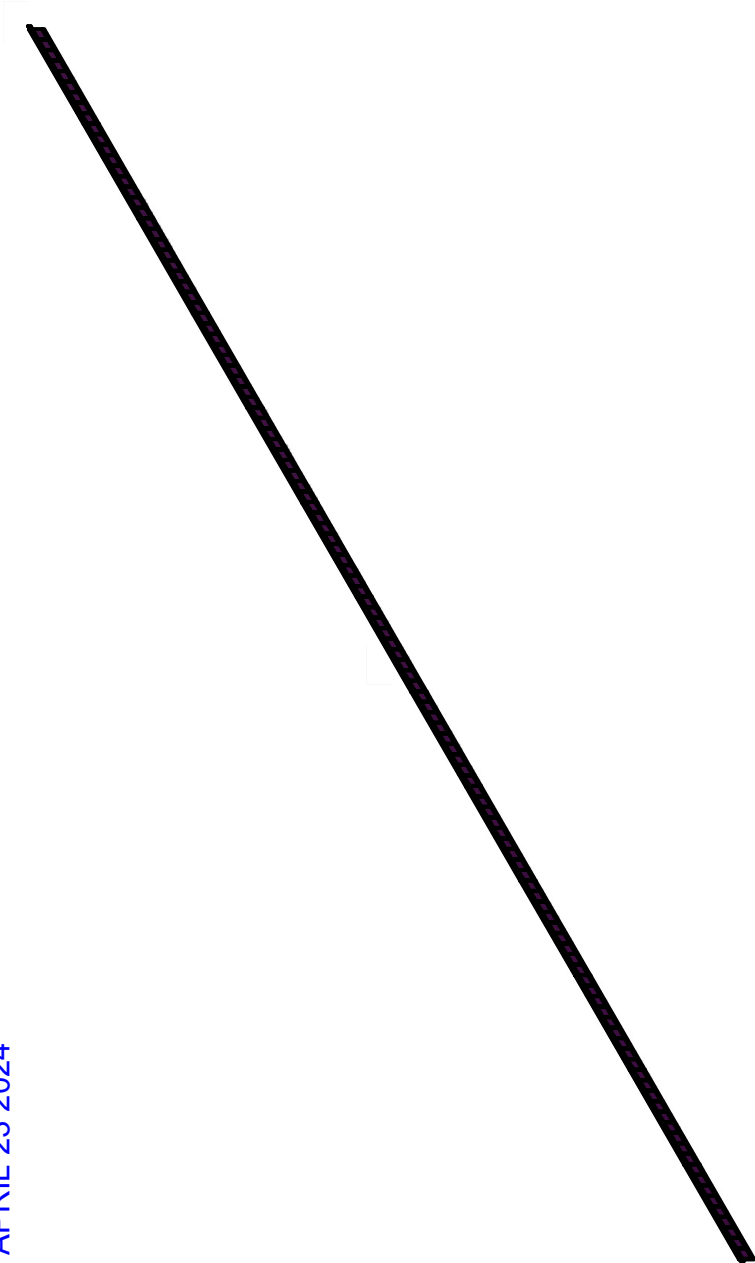


DETAIL C
SCALE 3 : 1

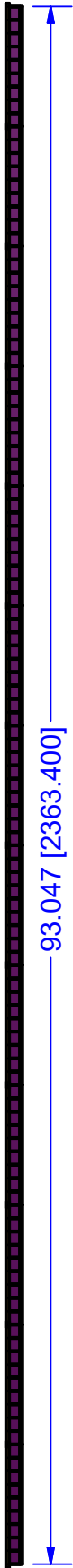


SEVEN MODULES WIDE

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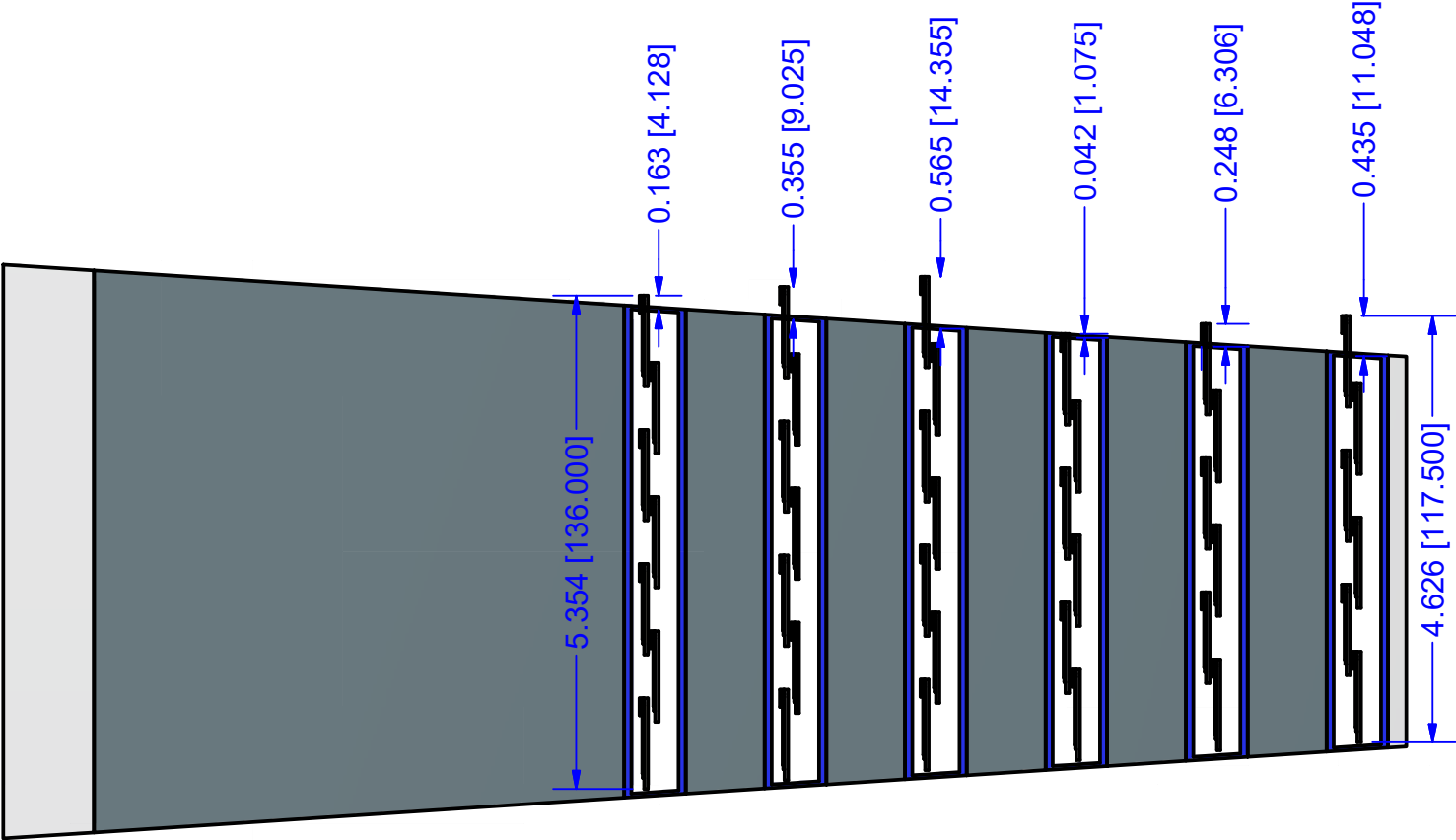
VIEW11
SCALE 1 / 10



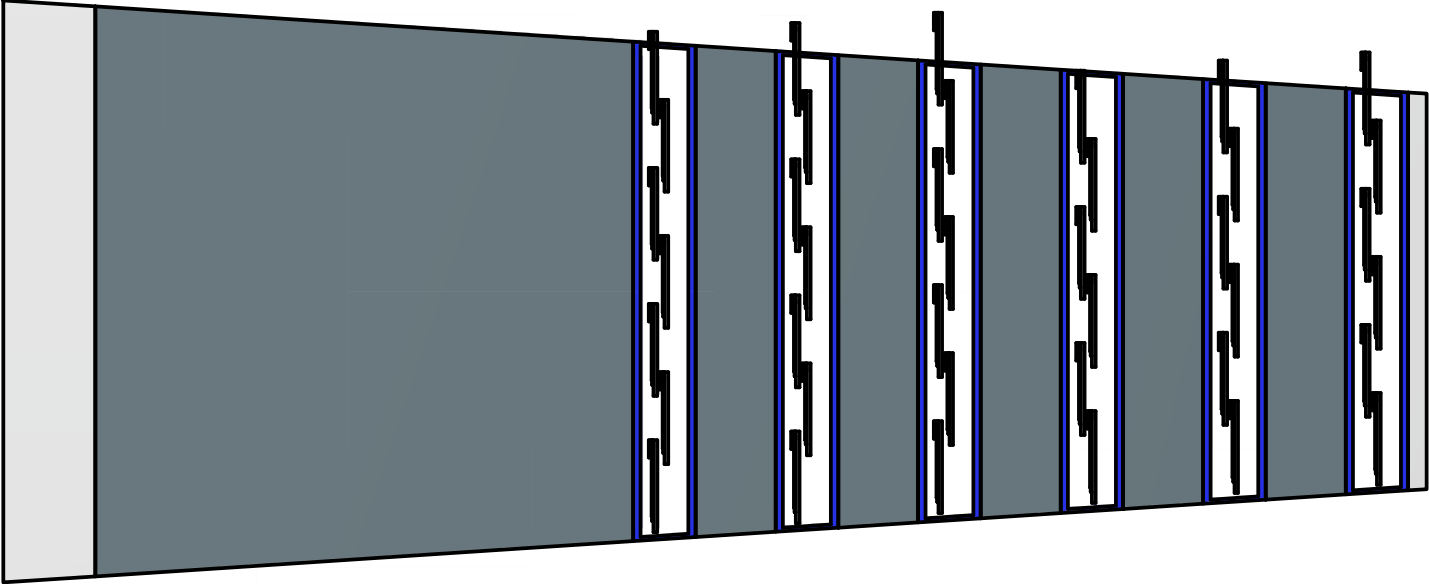
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ASTROPIX 2 x 2cm STAVE -13 MODULES

13 MODULES ARRAY
INCHES [mm]



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255 **C End-Of-Sector Board (EOSB) Interfaces**

256 **C.1 Starts with subsection**

257 **D AstroPix Wafer Quality Control**

258 **D.1 Starts with subsection**