ASIC Development at Nevis Laboratories/Columbia University

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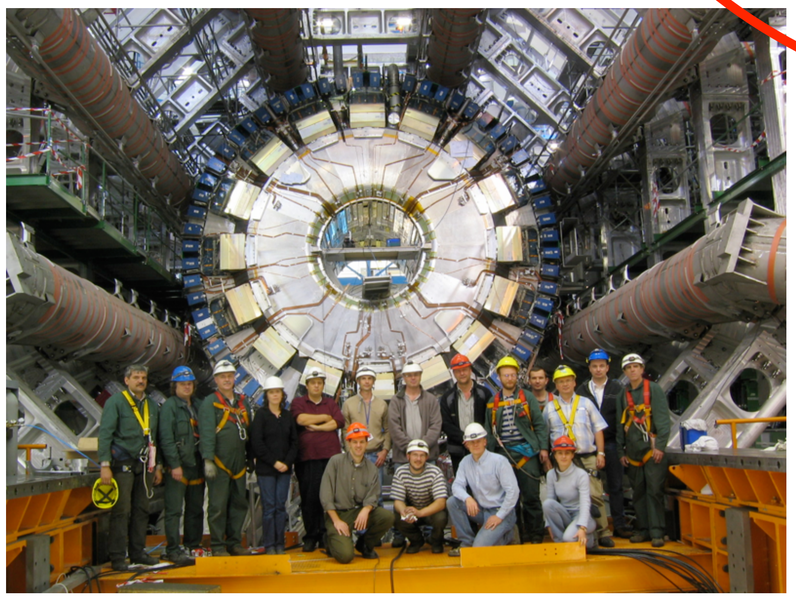
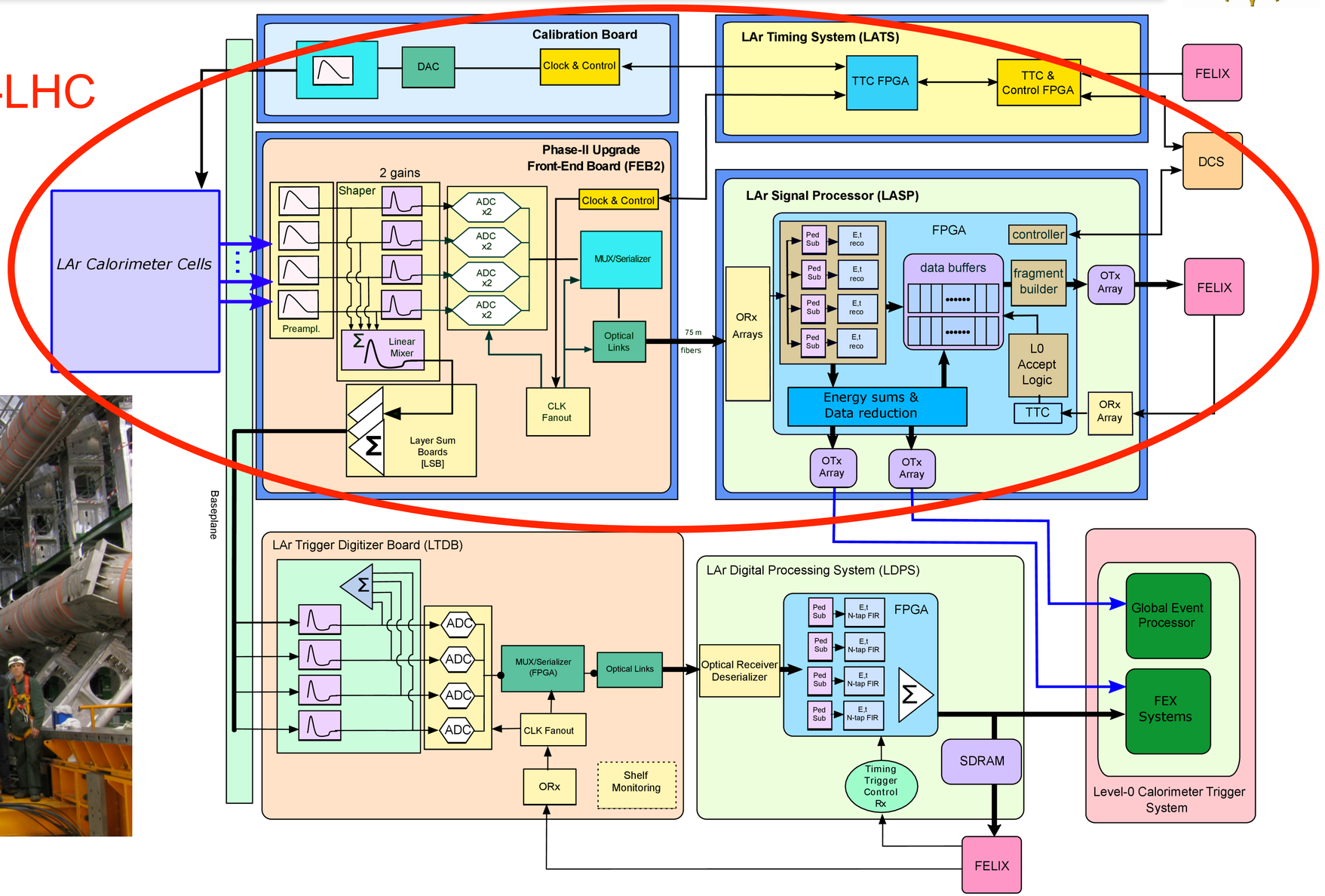
HEPIC Workshop
Brookhaven National Laboratory, April 30-May 2, 2024

Current Context

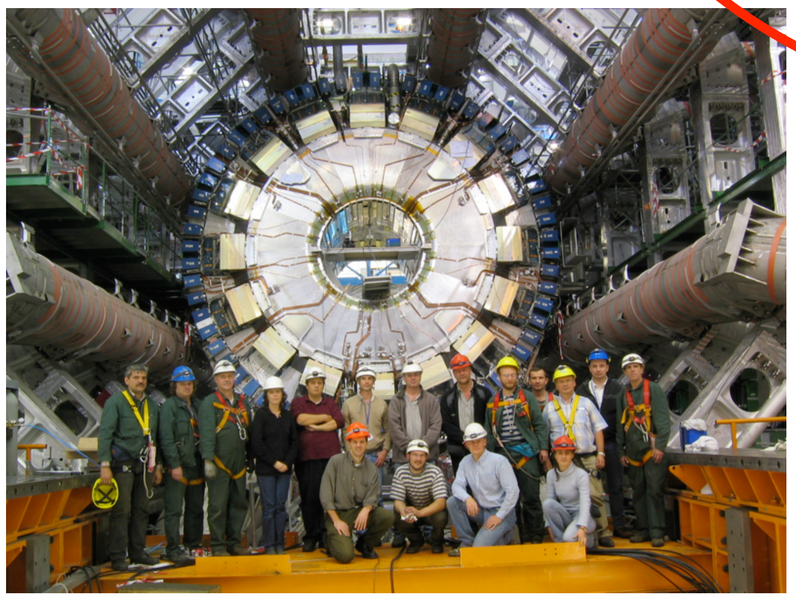
HL-LHC

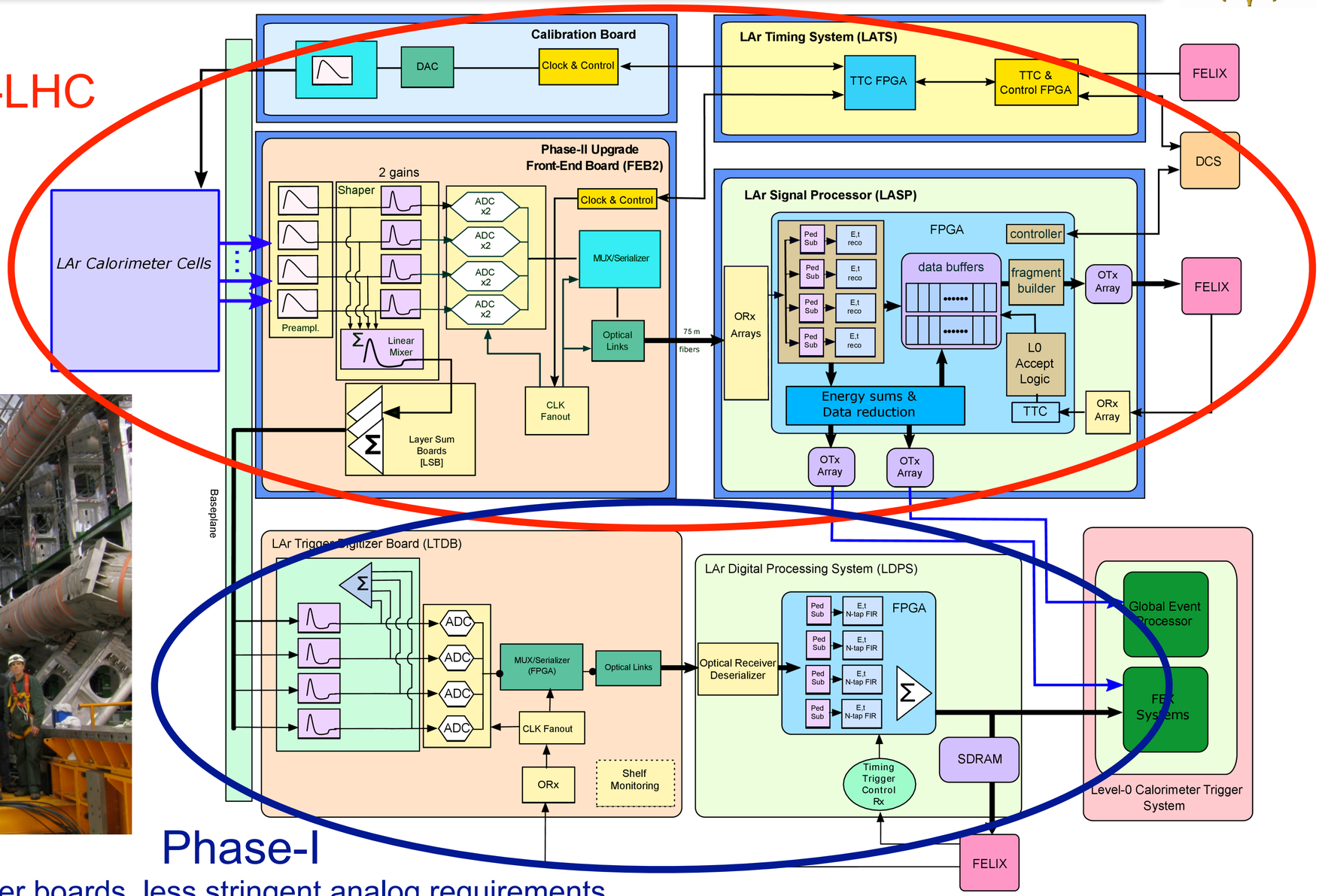




Current Context

HL-LHC



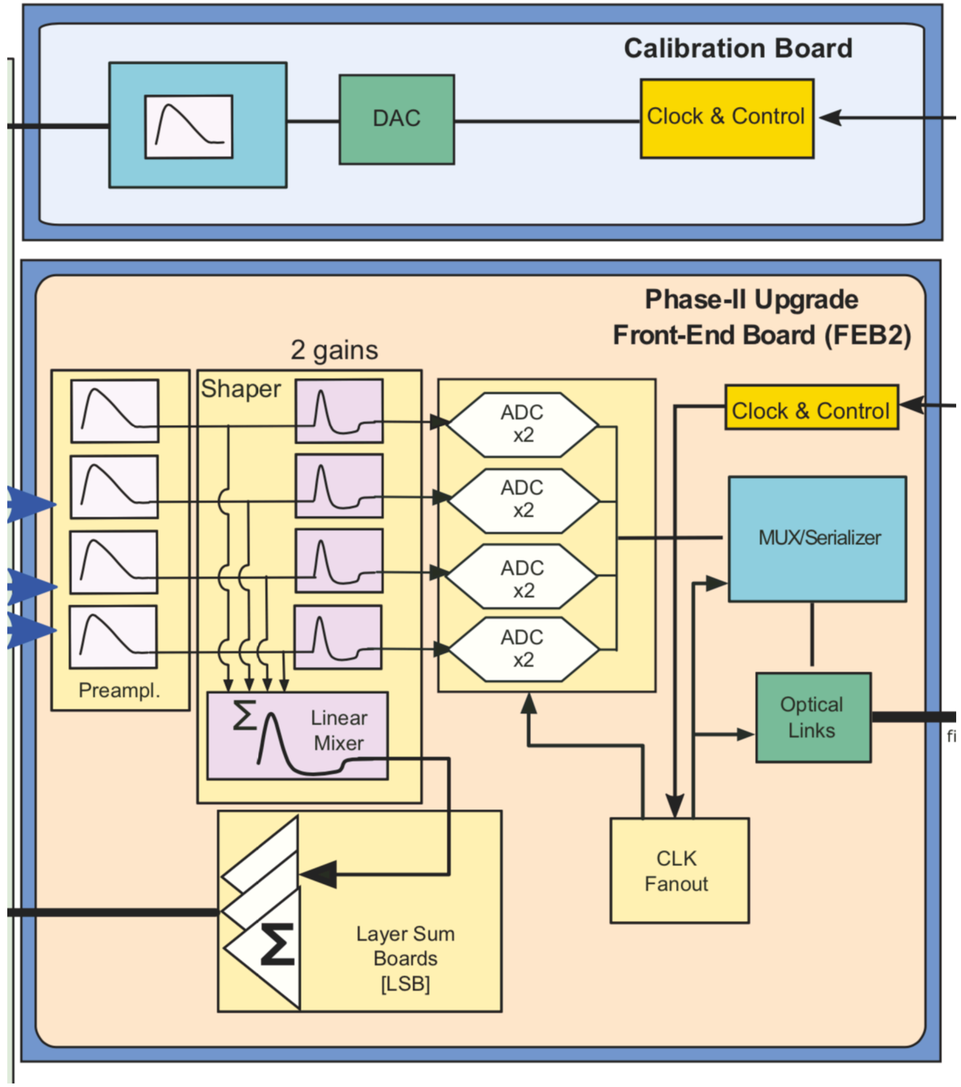


Phase-I

~10x fewer boards, less stringent analog requirements

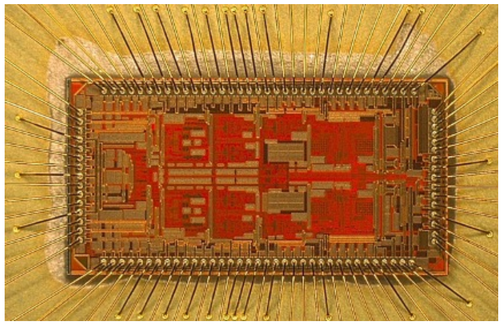
Key Readout Requirements/Components

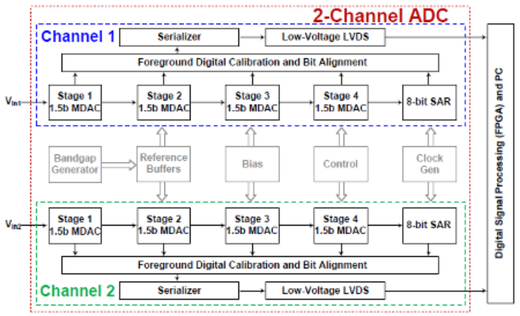
- Precision readout:
  - Need linearity ~0.1% up to 300 GeV (for precision physics, e.g. Higgs and W mass), electronics noise < MIP (for calibration), minimal saturation for large signals ⟹ 16-bit dynamic range with 11-bit precision
    - Implemented in 2 overlapping 14-bit gains
  - Nevis Labs responsible for ADC (with UT Austin) and front-end board
    - Builds on Phase-I experience
      - Improved trigger readout path (both granularity and precision)
      - Nevis developed 12-bit ADC with 10-bit precision
    - And original construction
      - Nevis developed 5 ASICs (including analog pipeline) and front-end board

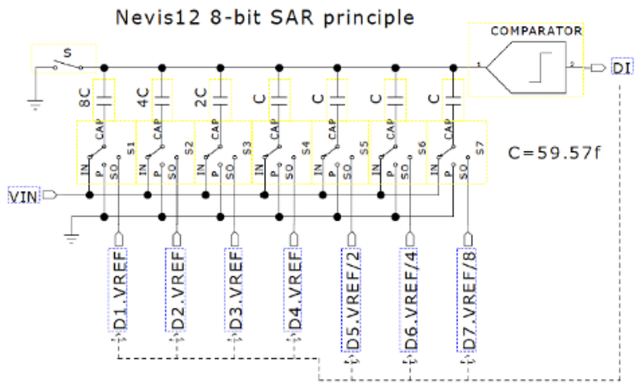


ATLAS LHC Phase-I Upgrade ADC

- Target: Quad, 40 MSPS, 12-bit dynamic range, 10-bit precision (ENOB) ADC
- Development effort started in 2008 (IBM/GF CMOS8RF, 130 nm)
  - Quickly realized would benefit from more expertise: developed close collaboration with Columbia Low Voltage Analog Designs group in Electrical Engineering (led by Peter Kinget)
    - Had multiple PhD students from the group participate in the design, interesting for them as they don't normally make "full chips" but rather targeted test structures
  - Stepwise development with ~yearly test chip
    - 2009: S&H circuit based on OTA at core of MDACs: understand technology, software, simulation
    - 2010: dual chip, 4 MDAC pipeline stages for most significant bits, radiation tests
    - 2012: dual, 4 pipeline stages + 8-bit SAR, digital error correction, reference voltage, output serializers, … just about all "plumbing" blocks



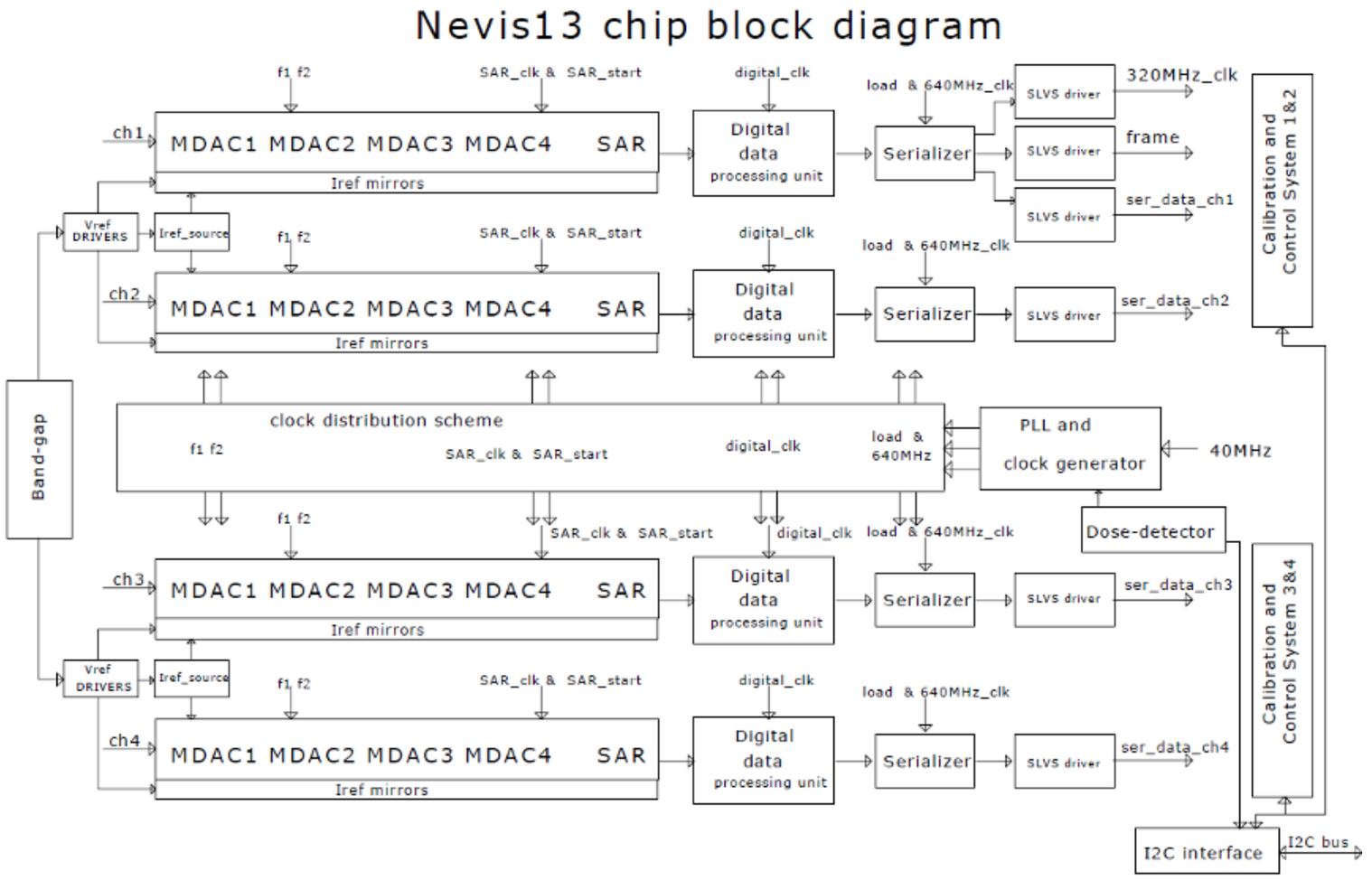




  - 2013: quad, 2012 chip + PLL, I2C, various "smaller" improvements

ATLAS LHC Phase-I Upgrade ADC

- Layout
  - 3.6mm x 3.6 mm
  - 120 die pins
  - 48 GND down-bonds
  - 72-pin QFN
- Blocks adapted from CERN:
  - Bandgap
  - PLL
  - I2C interface
- Power
  - 43 mW/channel
- Latency
  - 112.5 ns (last bit out)

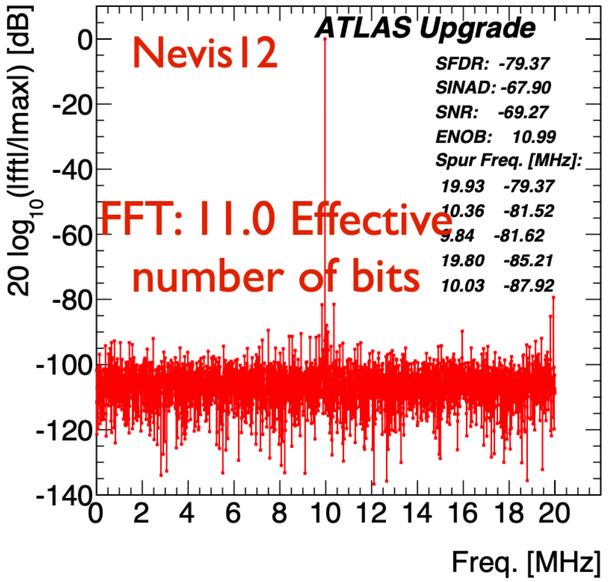


ATLAS LHC Phase-I Upgrade ADC

- Performance:
  - To ensure no missing codes, target MDAC gain slightly below 2
    - Consequence: dynamic range reduced to ~11.8 bits rather than 12
  - Technology (CMOS 8RF) should be 8-bit precise, so SAR does not need calibration
    - But calibration needed for MDACs! (Each MDAC is 1.5 bits to resolve 1 bit)
  - Comfortable radiation tolerance margin

Nucl.Instrum.Meth.A 855 (2017) 38-46
e-Print:1706.01535 [physics.ins-det]

At 10 MHz input at full scale:



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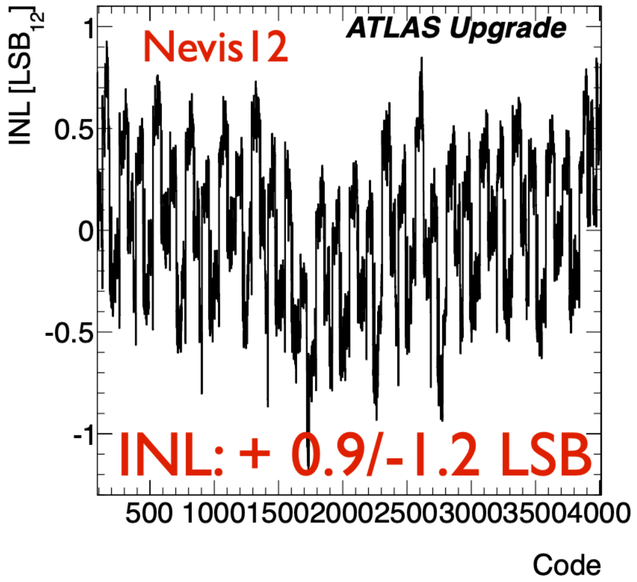
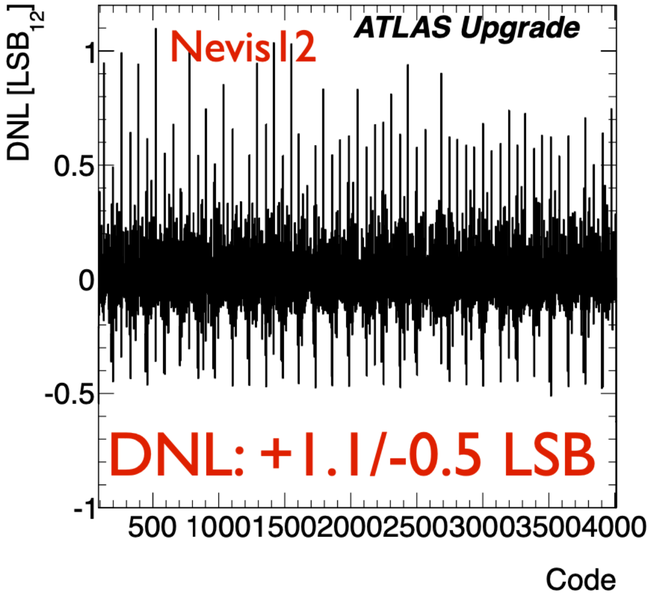
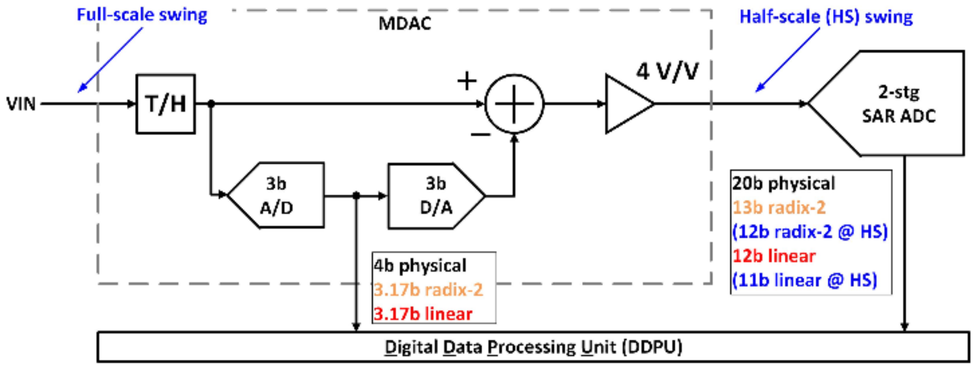


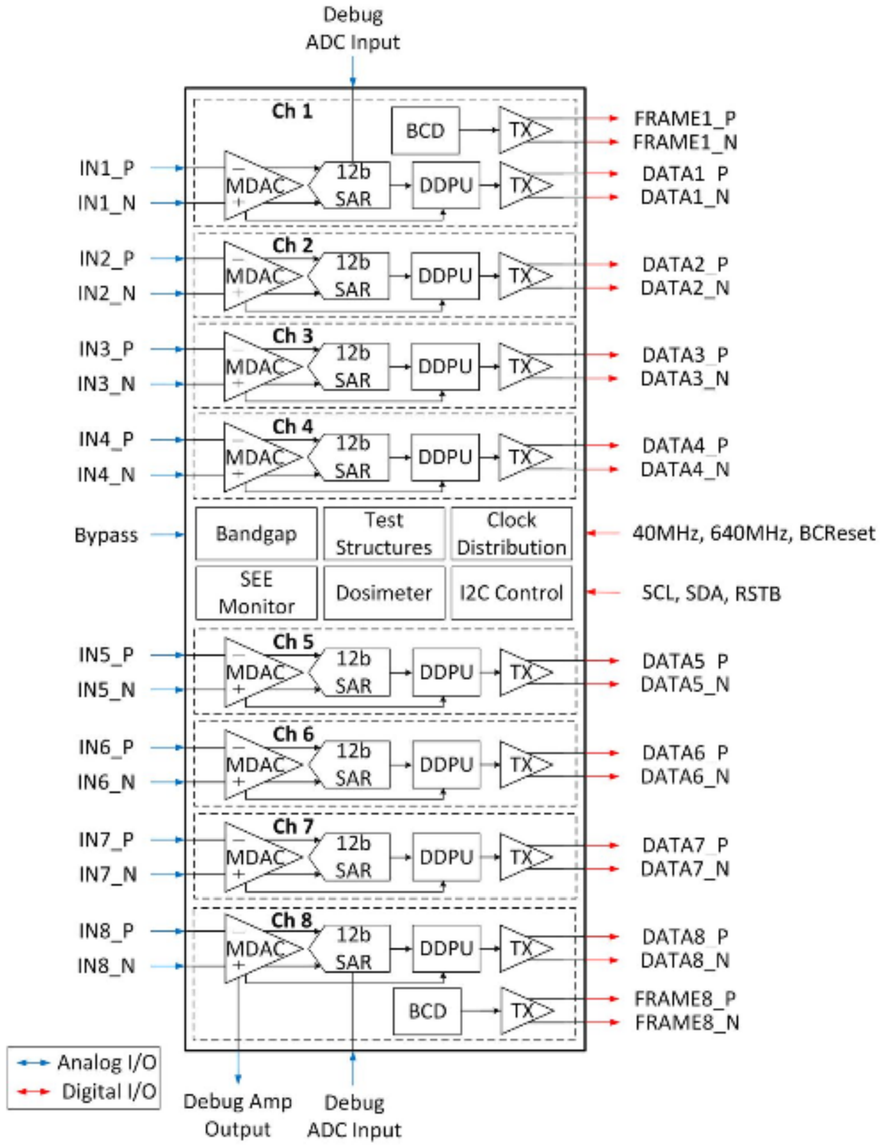
At 10 MHz input at full scale:



ATLAS LHC Phase-II Upgrade ADC

- For Phase-II, target is octal, 40 MSPS, 14-bit dynamic range with 11-bit precision
  - Enlarged the group: Columbia Nevis Labs + EE (Peter Kinget group) + UT Austin physics + UT Austin EE
    - ~yearly test chip cycle starting in 2017, final version in 2021
  - Now TSMC 65 nm CMOS (faster technology, use 1.2V only)
    - 3-bit MDAC + 12-bit SAR architecture (SAR needs calibration)

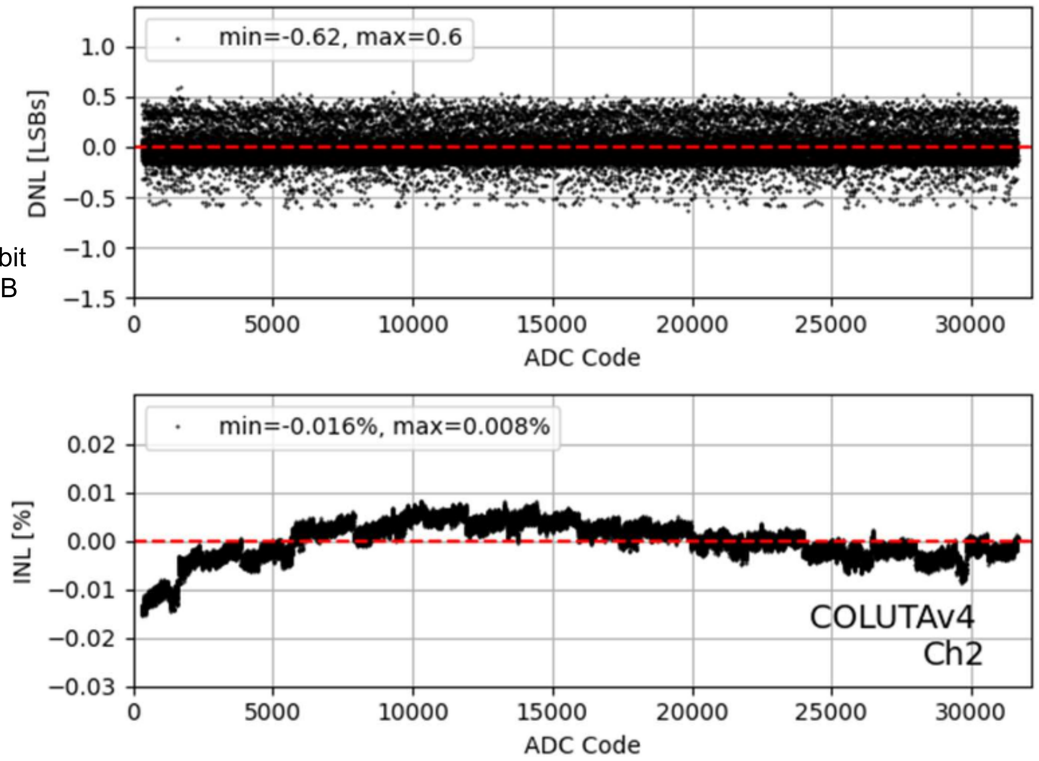


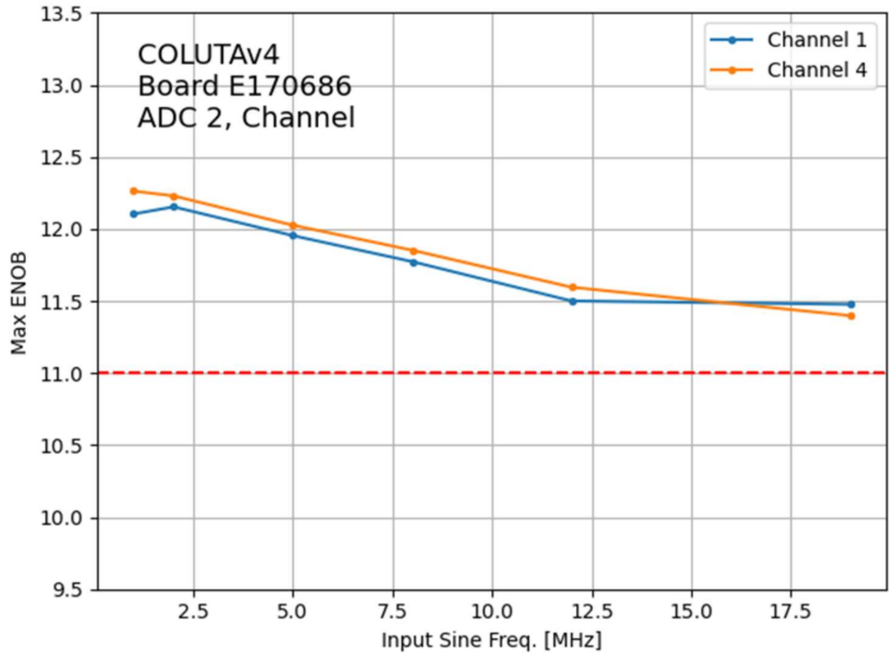


ATLAS LHC Phase-II Upgrade ADC

- Performance
  - Exceeds specs: almost 15-bit ADC, close to 12-bit ENOB@8 MHz (LAr pulse equivalent)
  - Comfortably radiation tolerant
  - 143 mW/channel

15-bit LSB





What's Next?

- At Lab level priorities are
  - Short/medium term:
    - ATLAS LAr front-end:
      - Phase-II ADC in production, QC is shared between UT Austin and CEA/Saclay
      - Front-end board: finalize design, run production & QC (~1 year)
    - AI on FPGAs: DUNE and smaller experiments, also exploring a somewhat related venture with engineering school
  - Longer term:
    - GRAMS: Pixellated LArTPC for gamma ray/antimatter astronomy (balloon/space-borne)
      - Exploring cold FE ASIC in collaboration with Columbia EE and Computer Science departments
    - Getting involved in "FCC" R&D, also likely applicable to other colliders
      - Current (or commercial) ADC likely fine for testbeams etc.
      - Once specs are better defined, will explore options

Extra

Radiation Tolerance

Table 1: Radiation tolerance requirements for the LAr front-end electronics for operation at the HL-LHC for a total luminosity of 4000 fb^{-1}, including safety factors given in brackets. This table supersedes Table 3.1 from the LAr Phase-II Electronics Upgrade TDR and is based on the most recent Geant4 simulations.

	TID [Gy]	**NIEL [n_{eq}/cm^2]**	**SEE [$h_{>20\,MeV}/cm^2$]**
FEC (barrel)	1400 (1.5)	4.1×10^{13} (2)	1.0×10^{13} (3)
FEC (endcap)	210 (1.5)	6.0×10^{12} (2)	1.2×10^{12} (3)
LVPS between TileCal fingers (barrel)	430 (1.5)	1.1×10^{13} (2)	2.8×10^{12} (3)
HEC and FEC LVPS (endcap)	81 (1.5)	2.0×10^{12} (2)	4.1×10^{11} (3)
LVPS new position (barrel)	18 (1.5)	5.1×10^{11} (2)	1.1×10^{11} (3)
LVPS new position (endcap)	33 (1.5)	5.2×10^{11} (2)	8.6×10^{10} (3)

(April 2021)