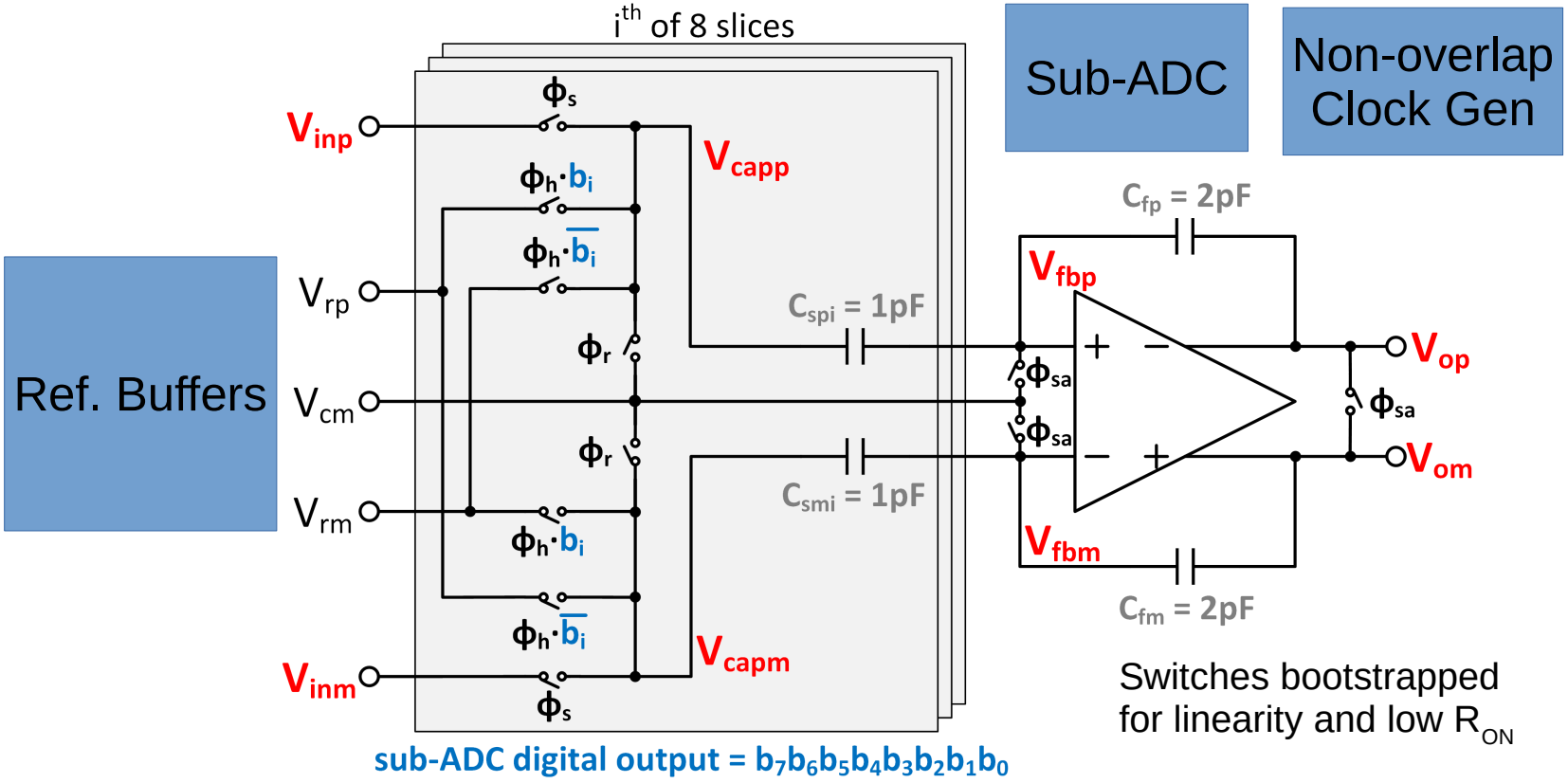
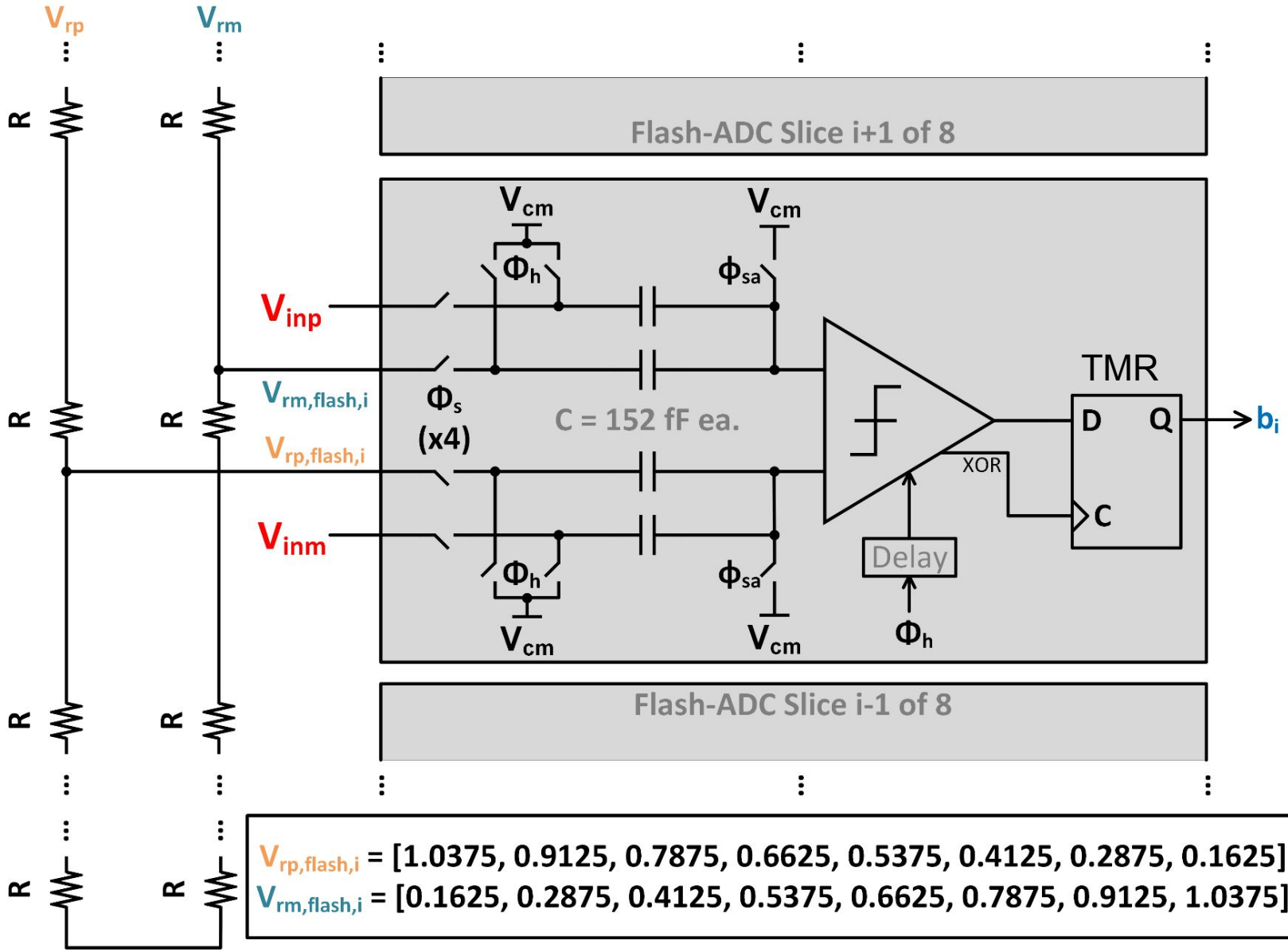
MDAC Implementation

- MDAC maps (1/8)*FS at the input → (1/2)*FS at the back-end ADC
- Input S/H cap = 4 pF diff. = 32 μV_{rms} kT/C noise. Compare against $V_{LSB} = 2\ V_{pp,diff} / 2^{15} = 61\ \mu V_{pp,diff}$
- Residue gain of 2^2 = 4 V/V (instead of 2^3) provides 1-b of inter-stage redundancy



Input S/H capacitors are sized for noise considerations to meet ≥ 14 bit dynamic range specification. Thermometer encoding guarantees monotonicity.

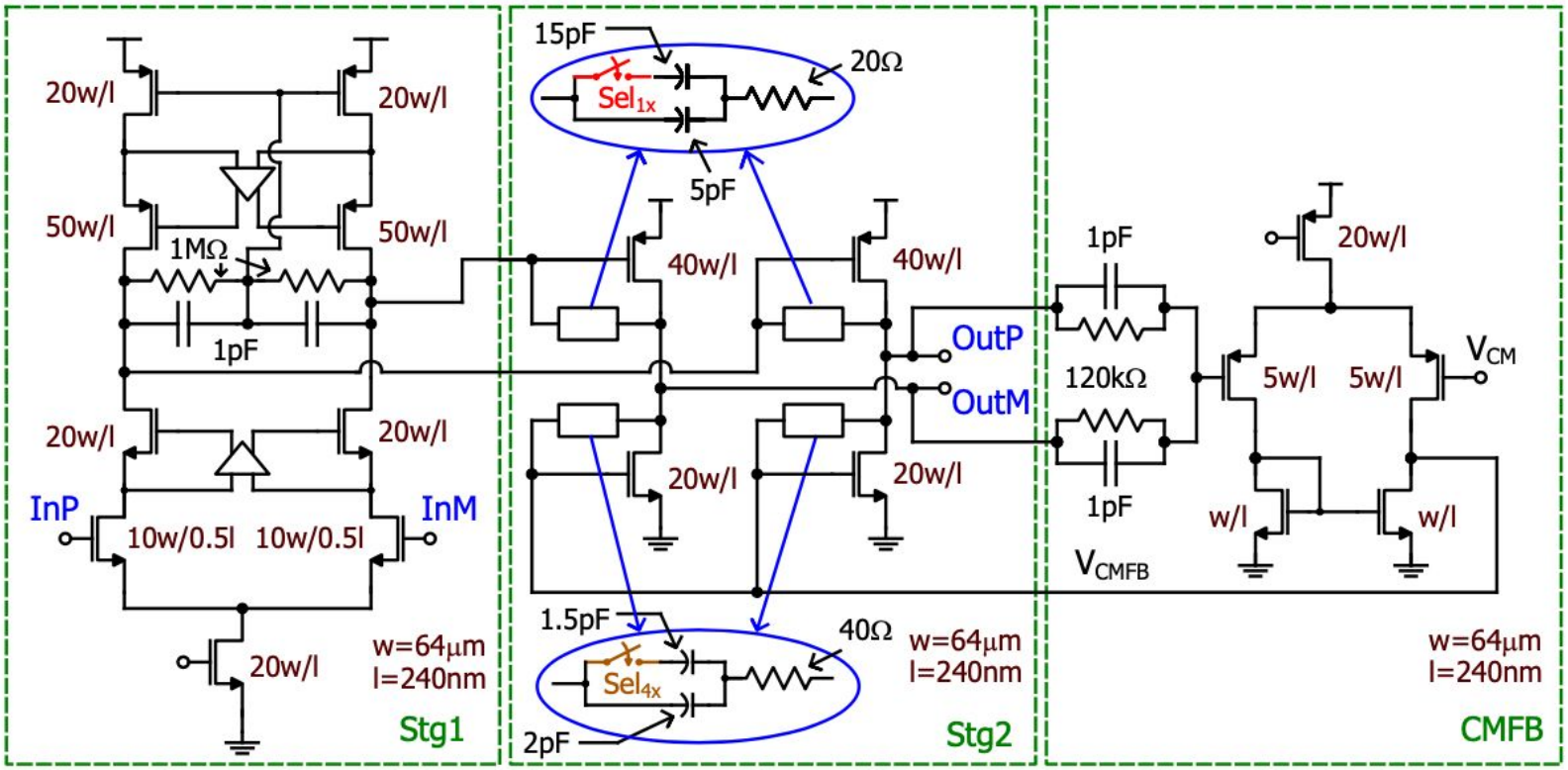
MDAC: Sub-ADC



$V_{rp,flash,i}$ = [1.0375, 0.9125, 0.7875, 0.6625, 0.5375, 0.4125, 0.2875, 0.1625] V

$V_{rm,flash,i}$ = [0.1625, 0.2875, 0.4125, 0.5375, 0.6625, 0.7875, 0.9125, 1.0375] V

MDAC: Residue OTA

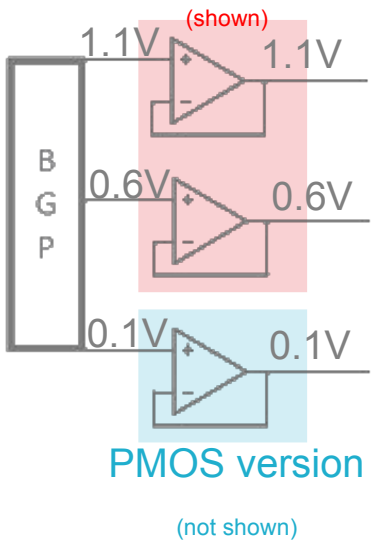


Two-Stage Gain-Boosted Telescopic Miller-Compensated OTA	
Gain (open-loop)	90 dB
Bandwidth (unity-gain)	300 MHz
Power	24mW

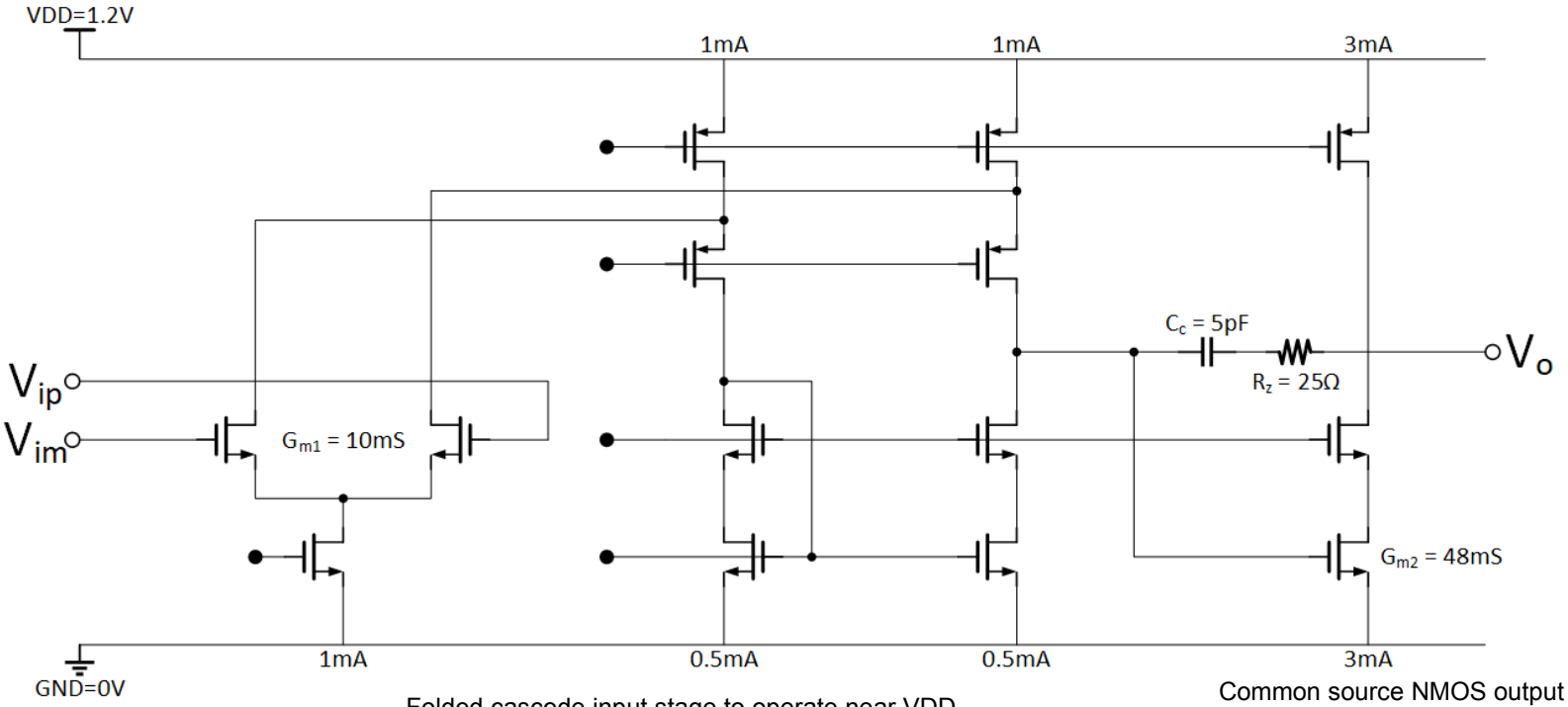
OTA for Residue Amplifier

- Operational Transconductance Amplifier (1.2V)
  - Gain boosted two-stage Miller-compensated topology
  - Using mostly LVT devices → smaller V_{GS}
  - Large output swing, centered around $V_{DD}/2$
  - Input Common-mode at $V_{DD}/2$
- Open-loop DC gain > 90dB
  - Guarantees no amplifier errors when in 4x configuration with ¼ feedback factor → loop gain still 86dB
  - L = 2 or 4 x L_{min} → larger DC Gain
  - Gain-boosting in first stage
- Differential Mode BW
  - Sel1x=0 for MDAC → UGB >= 300MHz
- CMFB
  - Local CMFB first stage → controls current second stage
  - 50dB CMFB amplifier for second stage, compensated with 3.5pF (sel4x=1)

MDAC: Reference Buffers



Bias circuits not shown



Folded cascode input stage to operate near VDD

Common source NMOS output stage to operate near VDD

Two-Stage Folded Cascode Miller-Compensated OTA in Unity-Gain Negative Feedback	
Power (per buffer)	7.8 mW
Gain (open-loop)	40 dB
Bandwidth (unity-gain)	170 MHz
Time to settle to 14-bit precision (for 8pF load)	9.7 ns