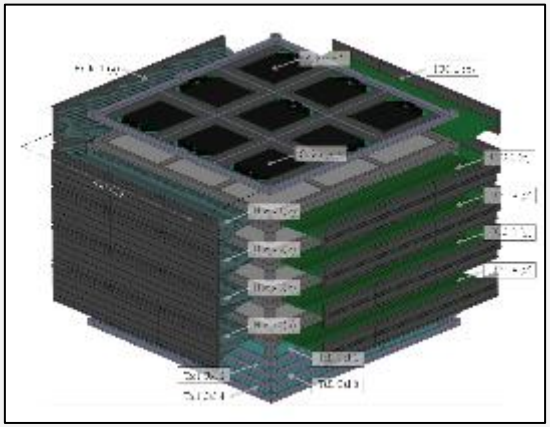
Overview of Group Activities
- University of Hawaii -

April 30, 2024

Boris Murmann, Matt Andrew, Makiko Kuwahara, Aera Jung, Richard Peschke, Gang Liu, (Gary Varner)

Outline/Overview

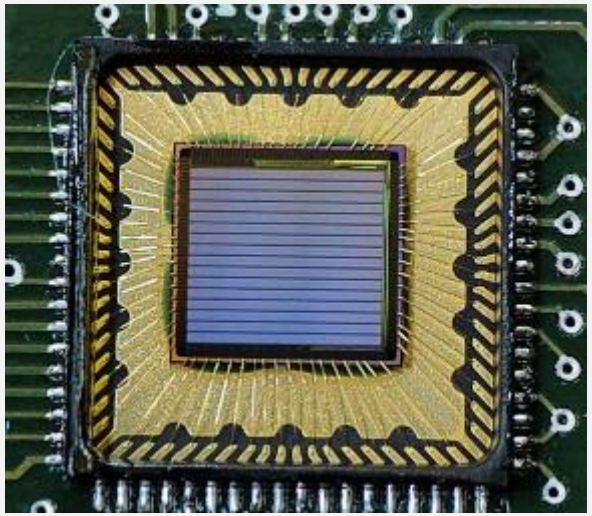
- ADCs for ADAPT (Antarctic Demonstrator for the Advanced Particle-astrophysics Telescope), led by WashU
  - Scintillating fiber-tracker, imaging (CsI) calorimeter, silicon strip detector for gamma- and cosmic-rays
  - ALPHA ASIC, designed by G. Varner et al.
  - HDSoC, designed by Nalu Scientific



- New Open-Source IC Design Course
  - https://github.com/bmurmann/EE628/
  - Students design delta-sigma modulators in IHP130

- ALPHA (Advanced Low Power Hybrid Acquisition) overview

Technology	TSMC 180 nm (MS RF G)
Area	38.7mm^2 (6mm x 6.4mm)
Power Supply	1.8V (ALPHA) / 2.5V (CT5TEA trigger ASIC)
Package	QFN 72-pin package



- Requirements
  - moderately high dynamic range
  - low noise
  - low power consumption (~10 mW)
  - high channel count (16)
  - high sample rate (100+ MSPS)
- V1 taped out in 2021
- V2 taped out in 2023

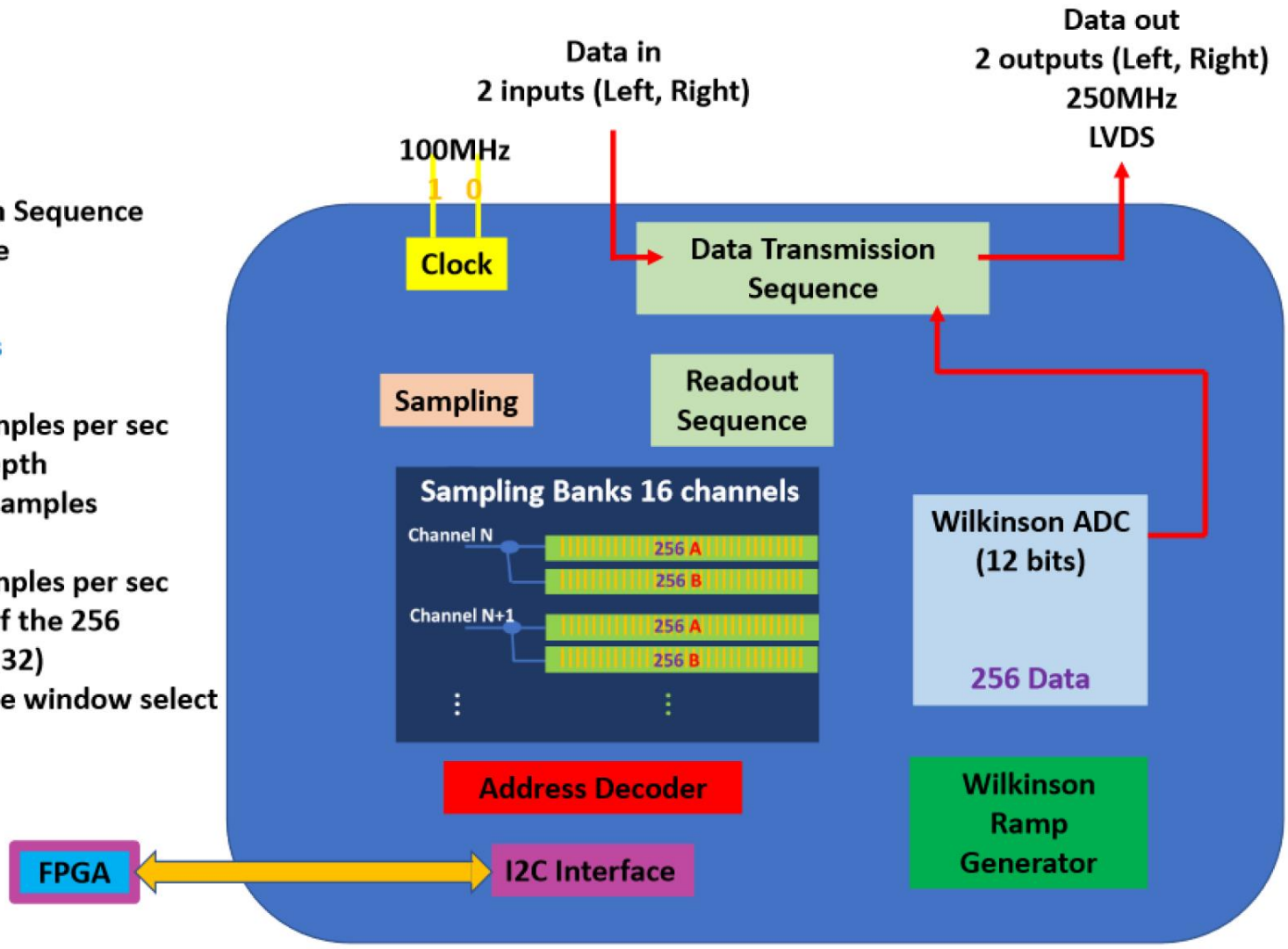
01 Alpha Block Diagram

New features

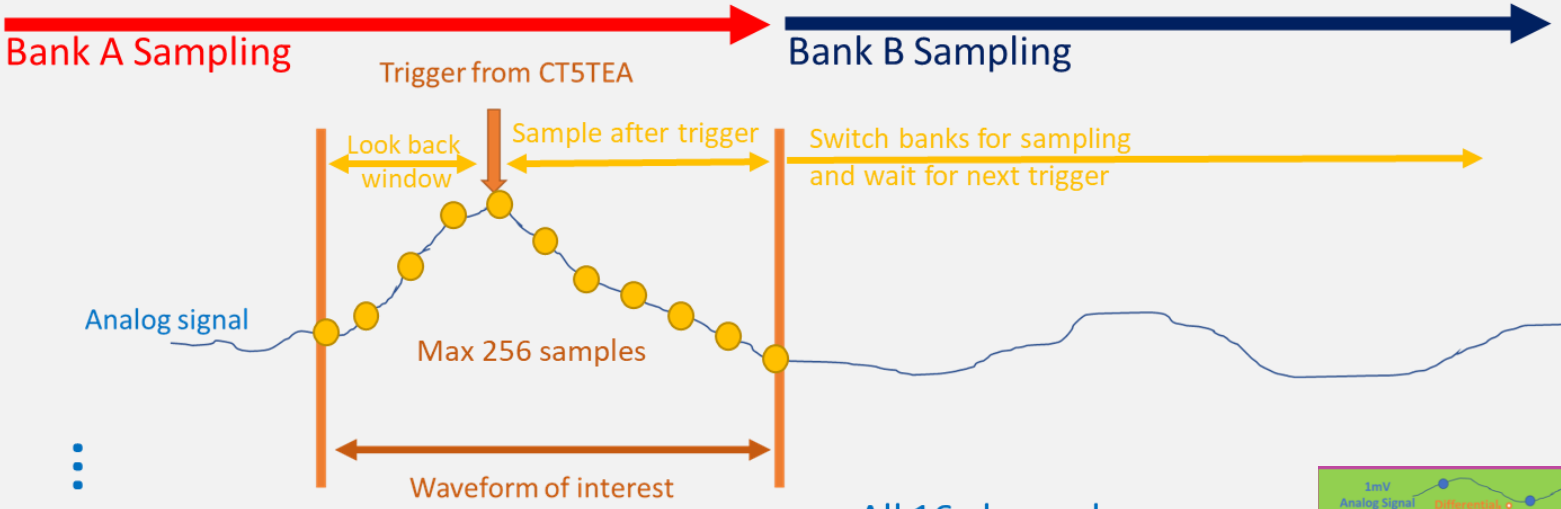
1. Data Transmission Sequence
2. Readout sequence

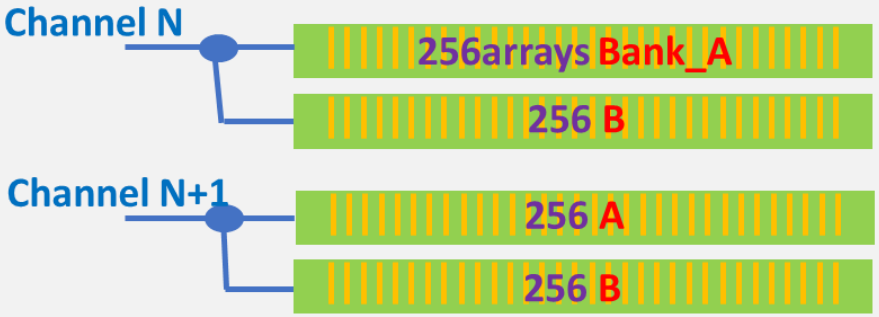
Two operating modes

1. Calorimeter
   - 100 mega samples per sec
   - 2 microsec depth
   - Approx. 200 samples
2. Tracker
   - 250 mega samples per sec
   - Use portion of the 256 samples (e.g. 32)
   - Programmable window select



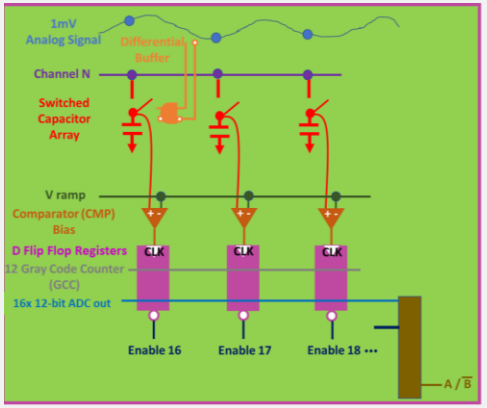
01 Alpha Sampling Scheme





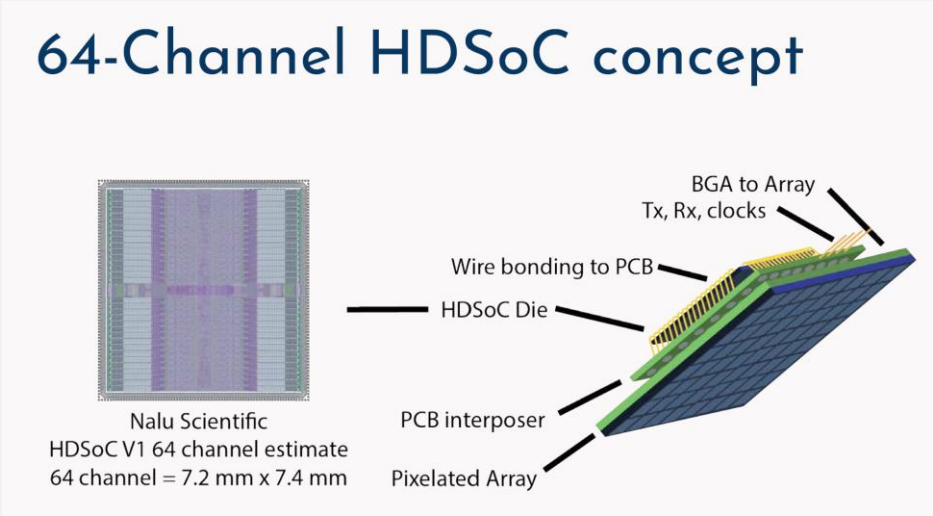
All 16 channels either bank A or B always active sampling

After trigger and wait interval, samples go to ADC



- Test of ALPHA V2 ongoing
  - Chip is alive, but still resolving various issues

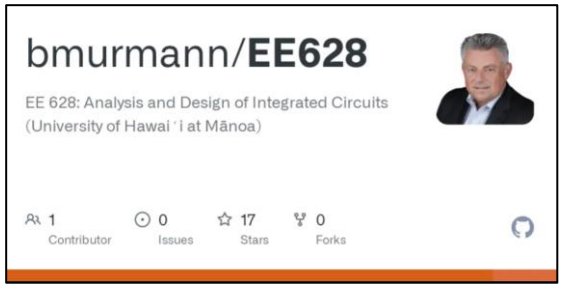
- Considering Nalu's HDSoC as an alternative



- Potential development of ALPHA V3 in the future
  - With focus on ultra-low power

EE 628 (University of Hawai‘i at Mānoa)

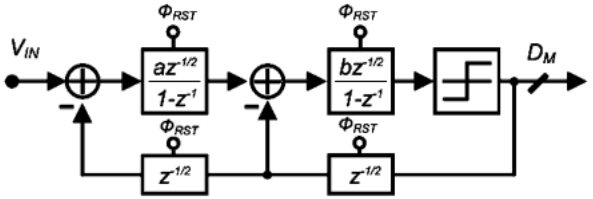
- Project course for students interested in mixed-signal chip design using open-source tools
- Students work in project teams toward a chip that can (potentially) be taped out (IHP 130nm)
- Experienced teams can create their own design
- Less experienced teams follow a “template” circuit designed by the instructor in “real time”
- Students gain exposure to
  - Circuit concept development
  - Circuit analysis, design and simulation
  - Layout and verification (DRC, LVS, PEX)
- **Teaming of students with complementary skill sets and “follow the instructor” model make this course accessible with minimal prerequisites**

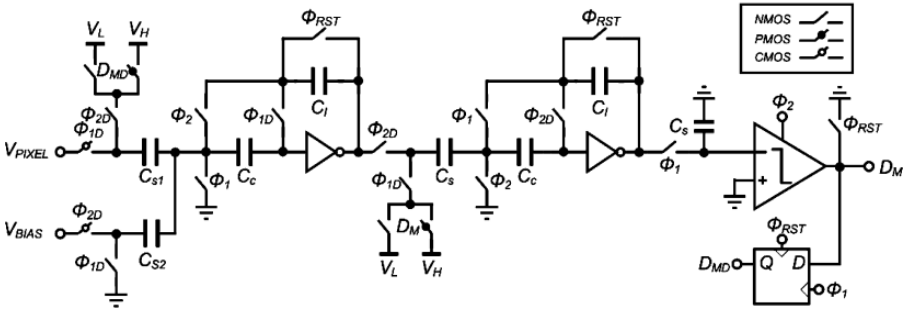


All files and course materials openly available on GitHub

“Template Project” – Incremental ΔΣ ADC (“Voltmeter Chip”)

[Chae, JSSC 1/2011]





High-level model → Design and layout of complete transistor-level circuit