RDC 4 – CPAD R&D Collaboration in ASICs & Electronics

Status update and next steps

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Principal ideas behind the RDCs

Detector R&D in many different technology areas is essential to realize many of the future planned experimental efforts spanning all of the frontiers in High Energy / Nuclear Physics

Much of the efforts needed require **collaboration** and **coordination** in order to realize the technologies required

- **Collaboration**: The required expertise/resources/new ideas often live within multiple people, institutions, labs and only by bringing these pieces together can we hope to realize the technological challenges
- **Coordination**: We live in a resource limited funding environment and so we need efforts to be coherent, minimize duplication, and to build off of progress happening elsewhere (both in other technologies and in other places)

Snowmass IF Recommendations

IF-1 Advance performance limits of existing technologies and develop new techniques and materials nurture enabling technologies for new physics, and scale new sensors and readout electronics to large, integrated systems using co-design methods.

IF-2 Develop and maintain the critical and diverse technical workforce, and enable careers for technicians, engineers and scientists across disciplines working in HEP instrumentation, at laboratories and universities.

IF-3 Double the US Detector R&D budget over the next five years, and modify existing funding models to enable R&D consortia along critical key technologies for the planned long term science projects, sustaining the support for such collaborations for the needed duration and scale.

IF-4 Expand and sustain support for blue-sky R&D, small-scale R&D, and seed funding. Establish a separate agency review process for such pathfinder R&D, independently from other research reviews.

IF-5 Develop and maintain critical facilities, centers and capabilities for the sharing of common knowledge and tools, as well as develop and maintain close connections with international technology roadmaps, other disciplines and industry.

CPAD RDCs

RDC	Topic	Coordinators
1	Noble Element Detectors	Jonathan Asaadi, Carmen Carmona
2	Photodetectors	Shiva Abbaszadeh, Flavio Cavanna
3	Solid State Tracking	Sally Seidel, Tony Affolder
4	Readout and ASICs	Angelo Dragone, Mitch Newcomer
5	Trigger and DAQ	Jinlong Zhang, (TBN)
6	Gaseous Detectors	Prakhar Garg, Sven Vahsen
7	Low-Background Detectors (incl. CCDs)	Noah Kurinsky, Guillermo Fernandez-Moroni
8	Quantum and superconducting Detectors	Aritoki Suzuki, Rakshya Khatiwada
9	Calorimetry	Marina Artuso, Minfang Yeh
10	Detector Mechanics	Andy Jung, Eric Anderssen
11	Fast Timing	Gabriele Giacomini, Matt Wetstein

ASICs and Electronics RDC4 roles

- **Foster collaborations** for generic “long term” R&D in alignment with PRDs related to ASIC and Electronics
- **Taking input from synergistic activities** (e.g., HEPIC) and creating opportunities for implementations
- **Ensuring coordination and collaboration** between US groups and other International groups
- **Support the organization of work packages** following input from this community
- **Promote RDC4** work packages and **help advocate for funding**
- **Foster a cross-institution framework for training** new generations of designers with hands-on components in HEP-funded facilities

Key scopes

Remove Legal Barriers:

- Enable sharing of design blocks
  - Common ground for foundry NDAs (Eg. TSMC, ARM)
- Establish clear and consistent guidelines on design blocks sharing among partners
  - Acknowledgment of credits
  - Understanding of critical needs related to multi-purpose institutions

Create more opportunities for collaboration and increase communication:

- Organize yearly workshops
- Catalog of designs / Data management
- Promote Cross-institution MPWs
- Lists information on groups and projects
- Maintains a Twiki and FAQs repository
- Provide Education and Training (course material to share)
- Advertise Jobs / Fellowship opportunities
- Lists ideas for student projects

by increasing communication and lowering or removing barriers for collaboration any costs incurred by the organization will be offset by its clear benefits

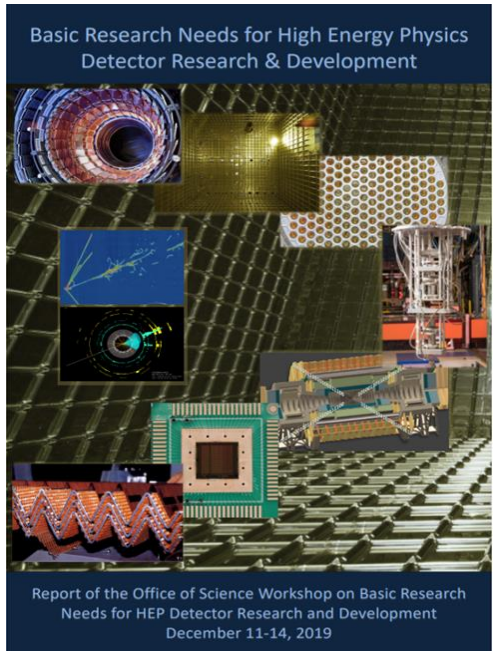
RDC 4 Coordination

Areas of overlap with other RDCs / DRDs / existing collaborations

- **HEPIC:** Community-organized workgroup providing input from the community on HEP IC design needs and challenges
  - RDC4 aims at implementing HEPIC recommendations within IF PRDs
- **ECFA DRD7** on Electronics and on-Detector Processing
  - RDC4 coordinators will engage with DRD7 coordinators to explore synergies, promote US community efforts, and foster collaboration
- **Other US collaborations** (US FCC, Linear Collider workgroup, Muon Collider Workgroup)
  - RDC4 coordinators will engage with other US collaborations to ensure RDC generic R&D efforts support collaborations in the of readout and ASICs
  - *Encourage RDC Blue Sky efforts to be passed on to project responsibilities.*
- **US Initiative on Microelectronics**
  - RDC4 coordinators will highlight potential opportunities to leverage the Microelectronics Initiative synergistically, supporting Microelectronics R&D and HEP core mission

RDC 4: R&D Priorities from the community

A cross-cutting Area with big challenges



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Snowmass

	BRN PRIORITY RESEARCH DIRECTION	
CALORIMETRY	**PRD 1:** Enhance calorimetry energy resolution for precision electroweak mass and missing-energy measurements	
	PRD 2: Advance calorimetry with spatial and timing resolution and radiation hardness to master high-rate environments	RDC9/RDC11/RDC4
	PRD 3: Develop ultrafast media to improve background rejection in calorimeters and particle identification detectors	
NOBLES	**PRD 4:** Enhance and combine existing modalities to increase signal-to-noise and reconstruction fidelity	RDC1/RDC7/RDC4
	PRD 5: Develop new modalities for signal detection	
	PRD 6: Improve the understanding of detector microphysics and characterization	
PHOTODETECTORS	**PRD 7:** Extend wavelength range and develop new single-photon counters to enhance photodetector sensitivity	
	PRD 8: Advance high-density spectroscopy and polarimetry to extract all photon properties	
	PRD 9: Adapt photosensors for extreme environments	
	PRD 10: Design new devices and architectures to enable picosecond timing and event separation	RDC2/RDC4
	PRD 11: Develop new optical coupling paradigms for enhanced or dynamic light collection	
QUANTUM	**PRD 12:** Advance quantum devices to meet and surpass the Standard Quantum Limit	
	PRD 13: Enable the use of quantum ensembles and sensor networks to fundamental physics	
	PRD 14: Advance state of the art in low-threshold quantum calorimeters	
	PRD 15: Advance enabling technologies for quantum sensing	RDC8/RDC4
ASIC	**PRD 16:** Develop process evaluation and modeling for ASICs in extreme environments	RDC 4
	PRD 17: Create building blocks for Systems-on-Chip for extreme environments	
SOLIDSTATE	**PRD 18:** Develop high spatial resolution pixel detectors with precise high per-pixel time resolution to resolve individual interactions in high-collision-density environments	RDC3/RDC11/RDC4
	PRD 19: Adapt new materials and fabrication/integration techniques for particle tracking	
	PRD 20: Realize scalable, irreducible-mass trackers	
TDAQ	**PRD 21:** Achieve on-detector, real-time, continuous data processing and transmission to reach exascale	RDC5/RDC4
	PRD 22: Develop technologies for autonomous detector systems	
	PRD 23: Develop timing distribution with picosecond synchronization	
X-CUT	**PRD 24:** Manipulate detector media to enhance physics reach	
	PRD 25: Advance material purification and assay methods to increase sensitivity	
	PRD 26: Addressing challenges in scaling technologies	

RDC 4 R&D Priorities Translation

- Topic Area #1: **Circuits and Architectures for 4D Tracking and Calorimetry**
  - Picosecond Timing Circuits
  - Efficient methods for increased granularity
  - Monolithic Readouts
  - Models and Techniques for extreme radiation
- Topic Area #2: **Big Data Management**
  - Energy efficient architectures and circuits
  - On-Chip Computing (e.g., eFPGA)
  - On-Chip AI/ML
  - Fast Interconnections and I/Os
  - Advanced Integration (3D, Photonics, Wireless)
- Topic Area #3: **Cryogenic and Deep Cryogenics**
  - 4K Circuits and Architectures for QIS
  - Circuits and Architectures for Noble Liquid Detectors
  - Cryogenic Models and Libraries
- Topic Area #4: **Methodologies, Tools, and Workforce Development**
  - Design for Verification methodologies
  - CAD Tools and Foundries shared joint access
  - Common IC blocks, Shared libraries and access model
  - Domain knowledge transfer and training

CPAD Received Abstract (via CPAD – RDC4 call)

- Received a total of 57 abstracts
  - 27 RDC4 specific
  - 13 shard with RDC3 and RDC11
  - 4 shared with RDC5
  - 5 shared with RDC1
  - 2 shared with RDC10
  - 3 with RDC2
  - 2 shared with RDC8

Id	Title	Speakers (affiliation)	Submitted for tracks
45	Testing of CRYO ASIC for the nEXO Experiment	Zepeng Li (UCSD)	RDC1: Noble Element Detectors; RDC4: Readout and ASICs
72	Q-Pix: ASIC Development and First Prototypes for Pixelated Charge Readout	Kevin Keefe (University of Texas at Arlington)	RDC1: Noble Element Detectors; RDC4: Readout and ASICs
99	LightPix: Scalable digital readout for cryogenic SiPM applications	Stephen Greenberg (University of California, Berkeley and Lawrence Berkeley National Lab)	RDC1: Noble Element Detectors; RDC4: Readout and ASICs
124	GAMPix: A Novel Charge Readout Architecture for Enhanced Spatial and Energy Resolution in TPCs	Bahrudin Trbalic (SLAC)	RDC1: Noble Element Detectors; RDC4: Readout and ASICs
126	The LArPix Pixelated Charge Readout System for Liquid Argon TPCs	Kevin Wood (Lawrence Berkeley National Laboratory)	RDC1: Noble Element Detectors; RDC4: Readout and ASICs
112	System tests for prototypes of the ATLAS ITK pixel detector	Zhi Zheng (SLAC)	RDC10: Detector Mechanics; RDC4: Readout and ASICs
157	A 1:100 Scale Pathfinder for the The OSCURA Experiment	CLAUDIO CHAVEZ (Fermilab)	RDC10: Detector Mechanics; RDC4: Readout and ASICs
18	Design of a 40 GS/sec 10 mw/Channel Waveform Sampling ASIC in 65 nm CMOS	Jinseo Park (University of Chicago)	RDC11: Fast Timing; RDC4: Readout and ASICs
24	Design, Testing, and Applications of the Fermilab CFD Readout ASIC	Si Xie (Fermi National Accelerator Laboratory)	RDC11: Fast Timing; RDC4: Readout and ASICs
150	From ETROC to VTROC (Vertically integrated Timing ReadOut)	Tiehui Ted Liu (Fermilab)	RDC11: Fast Timing; RDC4: Readout and ASICs
29	The beam test of the lead tungstate calorimeter prototype with SiPM readout at Jefferson Lab	Vladimir Berdnikov (Jefferson Lab)	RDC2: Photodetectors; RDC9: Calorimetry; RDC4: Readout and ASICs
28	Use of CVD Diamond Sensors in Extreme Environments and Applications	Mohammad Nizam (University of California Santa Cruz)	RDC3: Solid State Tracking; RDC11: Fast Timing; RDC4: Readout and ASICs
38	3D Integrated Testing Solutions	Artur Apresyan	RDC3: Solid State Tracking; RDC11: Fast Timing; RDC4: Readout and ASICs
63	SiGe integrated chip readout for fast timing	Zachary Galloway (Anadyne Inc.); Gabriel Saffier-Ewing (Anadyne Inc.)	RDC3: Solid State Tracking; RDC11: Fast Timing; RDC4: Readout and ASICs
111	Pebbles: paving the way toward 4D Pixel detectors in 28nm CMOS	Timon Heim (Lawrence Berkeley National Lab (LBNL))	RDC3: Solid State Tracking; RDC11: Fast Timing; RDC4: Readout and ASICs
191	Design Updates for HPSoC: A very high Channel Density Waveform Digitizer with sub-10ps resolution	Jennifer Ott (UCSC)	RDC3: Solid State Tracking; RDC11: Fast Timing; RDC4: Readout and ASICs
89	Design of the NAPA Prototypes Towards Large Area Sensors for Future e+e- Colliders	Alexandre Habib (SLAC)	RDC3: Solid State Tracking; RDC4: Readout and ASICs
93	Front-end neural network filtering implemented in a silicon pixel detector	Jennet Dickinson (Fermilab)	RDC3: Solid State Tracking; RDC4: Readout and ASICs
106	Integrated CMOS sensor r&d for future colliders	Nicola Bachetta (Fermilab)	RDC3: Solid State Tracking; RDC4: Readout and ASICs
116	MAPS R&D for tracking and calorimetry at future e+e- colliders	Caterina Vernieri (SLAC)	RDC3: Solid State Tracking; RDC4: Readout and ASICs
129	ATLAS ITk Pixel Module Electrical Quality Control	Emily Thompson (Lawrence Berkeley National Lab)	RDC3: Solid State Tracking; RDC4: Readout and ASICs
31	Exploration of Resource-efficient Implementations of ML Models Targeting eFPGAs	Jyothisraj Johnson (Lawrence Berkeley National Laboratory (LBNL))	RDC4: Readout and ASICs
51	Towards 4D tracking: 28nm sub-10ps TDC ASIC design and characterization setup	Larry Ruckman (SLAC)	RDC4: Readout and ASICs
53	Developments of Reconfigurable Digital Logic in the ASIC using 130nm and 28nm CMOS	Larry Ruckman (SLAC)	RDC4: Readout and ASICs
77	CRYO ASIC: A System-on-Chip (SoC) for Charge Readout in the nEXO Experiment	Aldo Pena Perez (SLAC)	RDC4: Readout and ASICs
87	CMS High Granularity Calorimeter ECON-D ASIC overview and radiation testing results	Grace Cummings (Fermi National Accelerator Laboratory)	RDC4: Readout and ASICs
88	Two-stage Cryogenic Charge Amplifier for Semiconductor Dark Matter Detectors	Arran Phipps (Cal State East Bay)	RDC4: Readout and ASICs
96	3D Heterogeneous Integration Multi-Project Wafer	Farah Fahim (Fermilab)	RDC4: Readout and ASICs
104	Testing and characterization of the RD53 ATLAS pixel production readout ASIC (ITkPixV2) for HL-LHC	Maria Mironova (Lawrence Berkeley National Lab)	RDC4: Readout and ASICs
110	RFSoC-based Readout and Characterization Platform Development at SLAC	Chao Liu (SLAC)	RDC4: Readout and ASICs
127	CryoCMOS modelling and PDK development for GF 22 FDX	Olivia Seidel (Fermilab)	RDC4: Readout and ASICs
130	Front-end Application Specific Integrated Circuits (ASICs) in 65 nm CMOS for Charge and Light Readout	Prashansa Mukim (Brookhaven National Laboratory)	RDC4: Readout and ASICs
135	An input buffer for PSEC5 – a waveform sampling ASIC – in 65nm CMOS Technology with a 5GHz analog bandwidth	Richmond Yeung (University of Chicago)	RDC4: Readout and ASICs
137	Readout IC for future Phase III high luminosity upgrade of the large Hadron collider	Benjamin Parpillon	RDC4: Readout and ASICs
158	Emerging approaches for a flexible and energy-efficient readout	Prafull Purohit (Brookhaven National Laboratory)	RDC4: Readout and ASICs
182	Warm Electronics for Time Division Multiplexed (TDM) SQUID readout of CMB-S4	Benjamin Reese (SLAC)	RDC4: Readout and ASICs
36	hls4ml: deploying deep learning on FPGAs for L1 trigger and Data Acquisition	Mia Liu	RDC5: Trigger and DAQ; RDC4: Readout and ASICs
81	Rapid Firmware/Software Development with SLAC's Open-Source Tools: SURF, RUCKUS, and ROGUE	Ryan Herbst (SLAC)	RDC5: Trigger and DAQ; RDC4: Readout and ASICs
92	Empowering AI Implementation: The Versatile SLAC Neural Network Library (SNL) for FPGA, eFPGA , ASIC	Abhilasha Dave (SLAC)	RDC5: Trigger and DAQ; RDC4: Readout and ASICs
184	Future detector readout	Alexander Paramonov (Argonne National Laboratory)	RDC5: Trigger and DAQ; RDC4: Readout and ASICs
10	Towards the Muon Collider Detectors	Sergo Jindariani (Fermilab)	RDC6: Gaseous Detectors; RDC11: Fast Timing; RDC4: Readout and ASICs; RDC3: Solid State Trackir
49	Ultra-low Background Flexible Cables	Isaac Arnquist (PNNL)	RDC7: Low-Background Detectors; RDC2: Photodetectors; RDC4: Readout and ASICs
143	Skipper CCD-in-CMOS active pixel sensor: status and first characterization results	Benjamin Parpillon (Fermilab)	RDC7: Low-Background Detectors; RDC2: Photodetectors; RDC4: Readout and ASICs
144	Scalable SNSPD cryogenic readout	Davide Braga (Fermilab)	RDC8: Quantum and Superconducting Sensors; RDC11: Fast Timing; RDC4: Readout and ASICs; RDC3
178	Advanced time-division transition-edge sensor readout development for CMB-S4	Shawn Henderson (SLAC)	RDC8: Quantum and Superconducting Sensors; RDC4: Readout and ASICs
1	DC-DC conversion using new materials and architectures	UPenn Physics, and UPenn SEAS (School of Engineering and Applied Science)	
2	AC-LGAD Readout using SiGe BiCMOS technology	UC Santa Cruz, Anadyne INC	
3	Waveform readout of fast semiconductor timing detectors	UC Santa Cruz, Nalu Scientific	
4	Readout circuits on 28nm for 4D tracking at future colliders	SLAC	
5	3D Integrated Sensing Solutions project	SLAC, FNAL, LLNL	
6	Large-area MAPS with ~ns timing	SLAC, CERN, Uoregon	
7	Cryogenic CMOS	SLAC	
8	eFPGA and Reconfigurable Digital Logic	SLAC	
9	AI/ML for Future Readout	SLAC	
10	Beyond Von-Neumann CMOS accelerators	SLAC, UCSB	
11	SLAC Neural Network Library SNL	SLAC	
12	RFSoC-based Readout and Characterization Platform Development at SLAC	SLAC	

Where we are now

- At CPAD we solicited ideas for collaborations around specific projects
  - 11 responses come in the form of one-page ideas (SLAC -5, ANL -3, Penn -2, UCSC -1)
  - Series of meetings to allow additional ideas to bubble up

- Clear areas where collaborations can form have been identified (so far…)
  - 4D Tracking front-ends and fast timing ASICs (SLAC, LBNL, FNAL, UCSC ….)
  - MAPS architectures (SLAC, FNAL….)
  - Cryogenic readouts (LBNL, FNAL, SLAC….)
  - eFPGAs (SLAC, LBNL, FNAL….)

Next steps

- Encourage collaboration group formation
  - Collaboration proposals
    - Work plan
    - Organization
- Work with the RDC coordination to identify and prioritize funding opportunities to fund elements of the collaboration work plans
  - RDC Community Meeting – May 3rd 12pm CT
- Engage to ensure connections between the RDC 4 collaboration groups and other collaborations (e.g., DRD7, US FCC …)

DRD 7 Initial Focus areas

- Data density and power efficiency (WG 7.1)
- Intelligence on the detector (WG 7.2)
- 4D and 5D techniques (WG 7.3)
- Extreme environments (WG 7.4)
- Backend systems and commercial-off-the-shelf components (WG 7.5)
- Complex imaging ASICs and technologies (WG 7.6)

The collaboration currently comprises 64 contributing institutes in 15 countries, and we are developing an agreed work plan for an initial three-year R&D phase. The collaborating institutes intend to contribute to 16 projects with an aggregated yearly effort of over 100 FTEs. The collaboration will remain open to new participants and projects and is intended to continue and evolve in the long term.

Stay connected

- Dedicated RDC Email List
  - cpad_rdc4@fnal.gov
  - To subscribe:
    - Send an e-mail message to listserv@fnal.gov
    - Leave the subject line blank
    - Type “SUBSCRIBE cpad_rdc4 FIRSTNAME LASTNAME” (without the quotation marks) in the body of the e-mail message
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Backup