Monolithic Stitched Sensor

HEP-IC 2024

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Outline

- Monolithic Stitched Sensor (ER1 Submission)
  - Introduction
  - ER1: MOSS and **MOST** (timing prototype)
  - **MOST:** Architecture and Design
  - Design Challenges

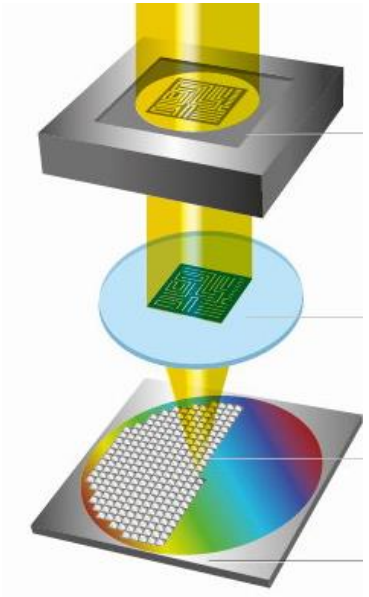
- Next generation (ER2 Submission)
  - MOSAIX (Alice/ITS3 upgrade)
  - **Readout Link**

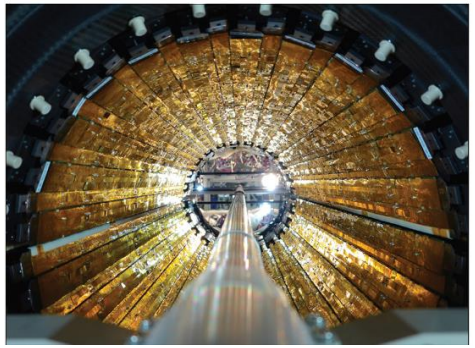
Introduction

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - Typical sizes of few cm^2
  - modules are tiled with chips connected to a flexible printed circuit board

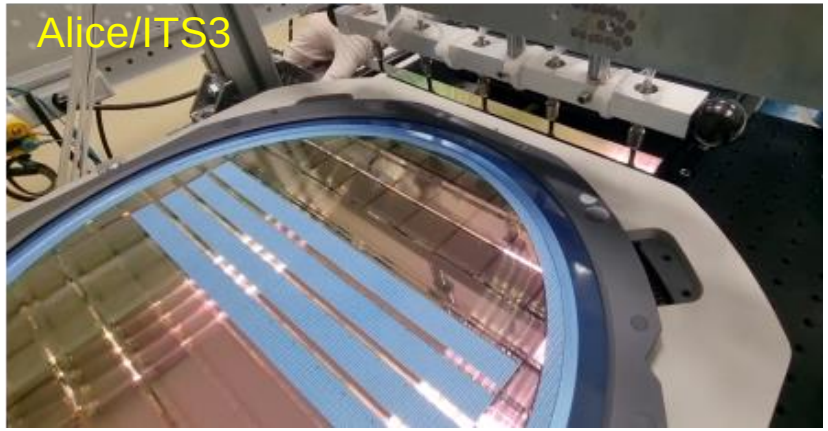
- Wafer-scale sensors: stitching
  - New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
  - wafer-size chip

Principle of photolithography





Alice/ITS2

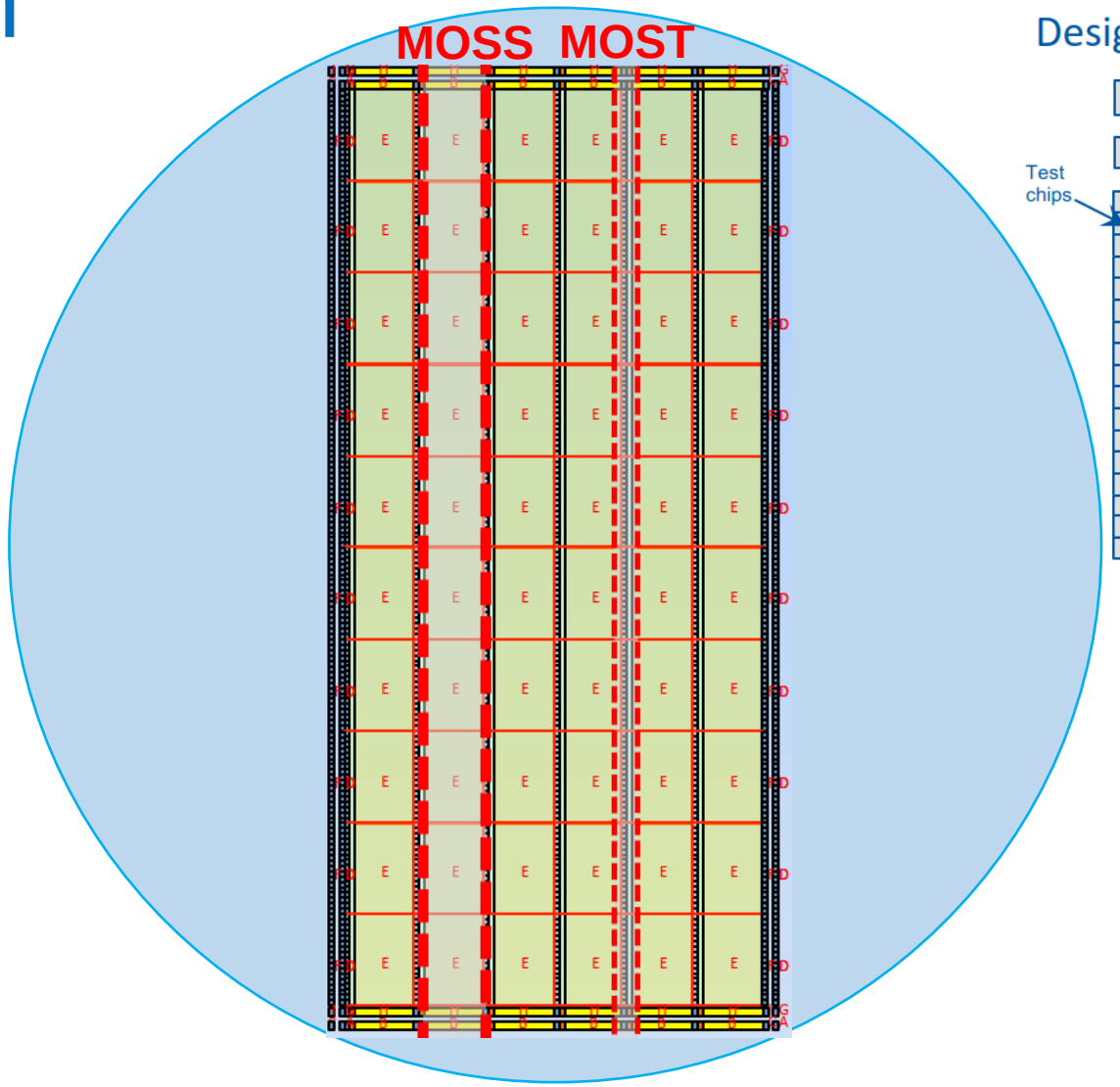


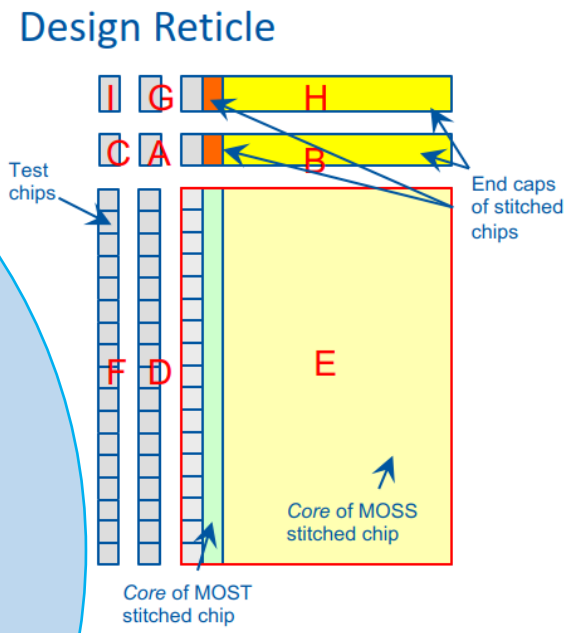
Motivation: Reduction of the material budget

Challenges: Power supply, cooling, and design/yield

ER1 Submission

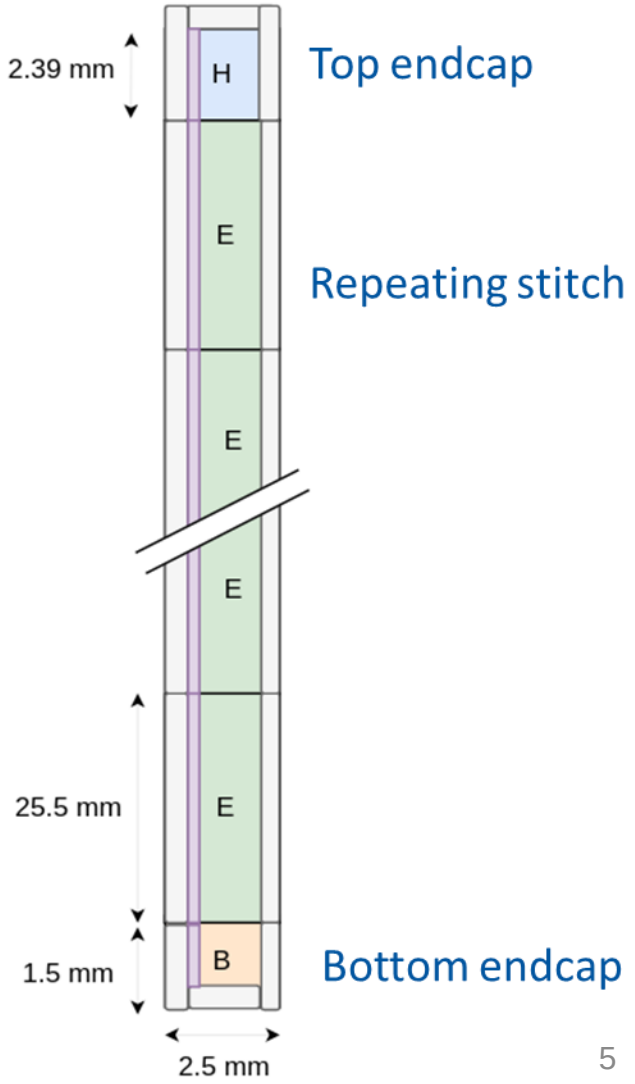
- Learn and prove stitching
- Two large stitched sensor chips (MOSS, MOST)
- Different approaches for resilience to manufacturing faults
- Small test chips (Pixel Prototypes)





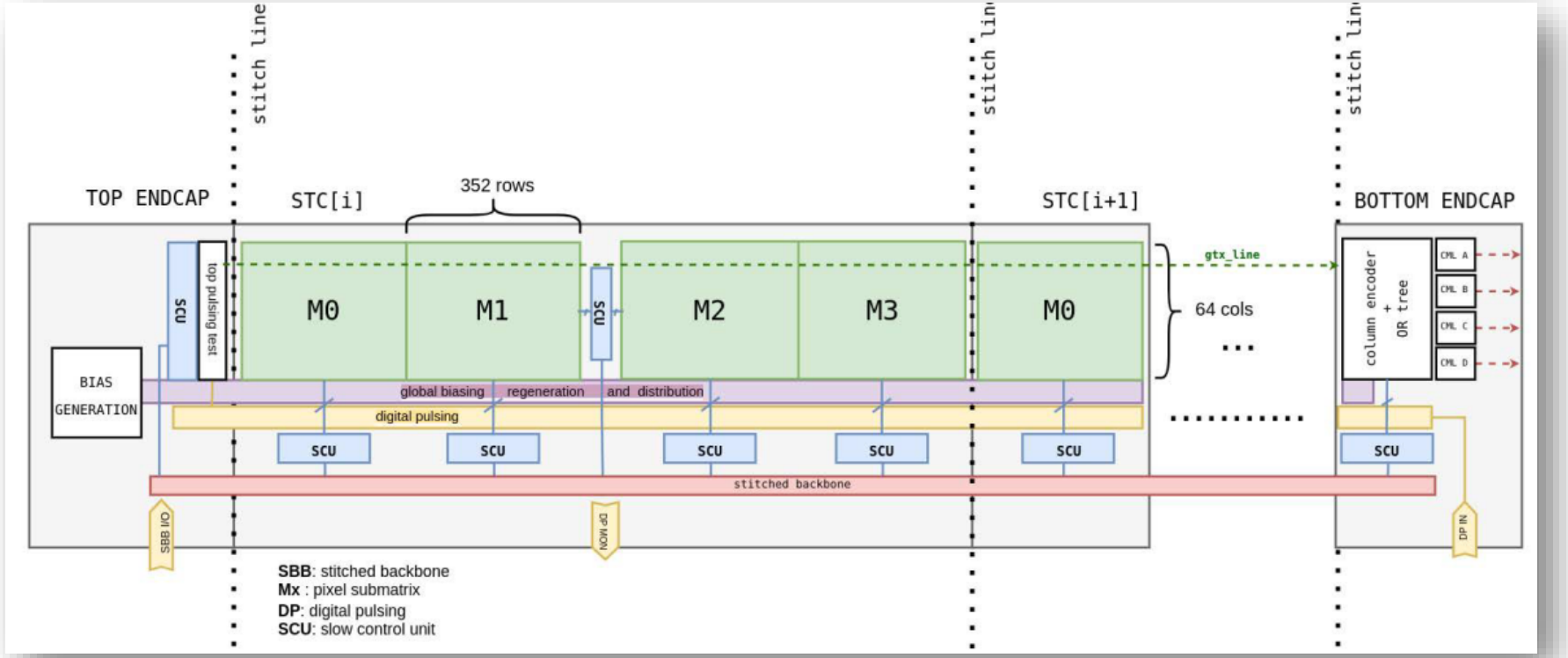
Monolithic Stitched Timing Prototype (**MOST**)

- Aim of the **MOST** submission:
  - Investigate power and signals on wafer scale chip
  - Higher granularity in power gating in case of a defect of
    - analog (rows of 4 pixels)
    - digital (half columns)
  - Explore low power **asynchronous** serial readout solutions
  - Immediate transfer of hit data to the periphery (no strobing).
  - Explore long line (several cm range) transmissions **timing** and power performance



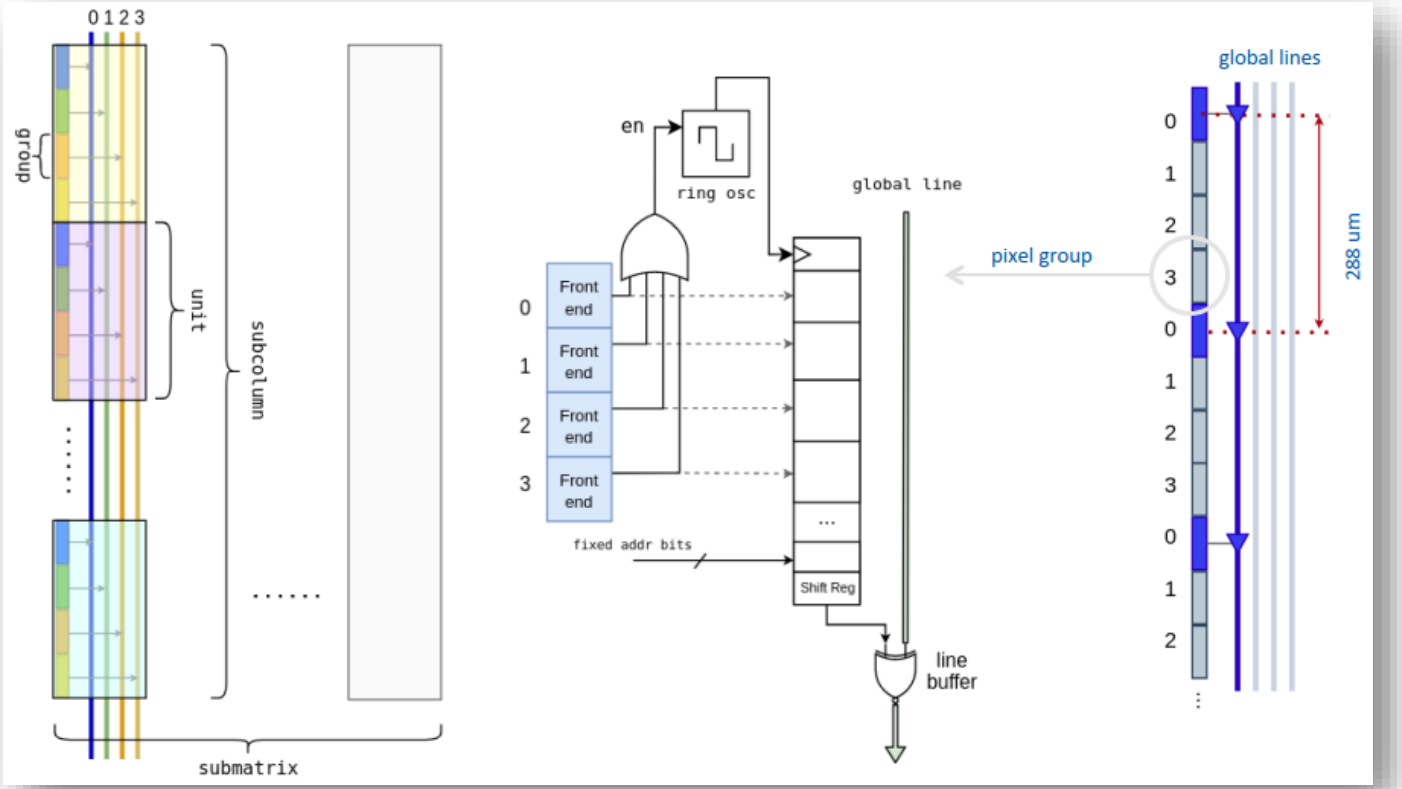
Monolithic Stitched Timing Prototype (**MOST**)

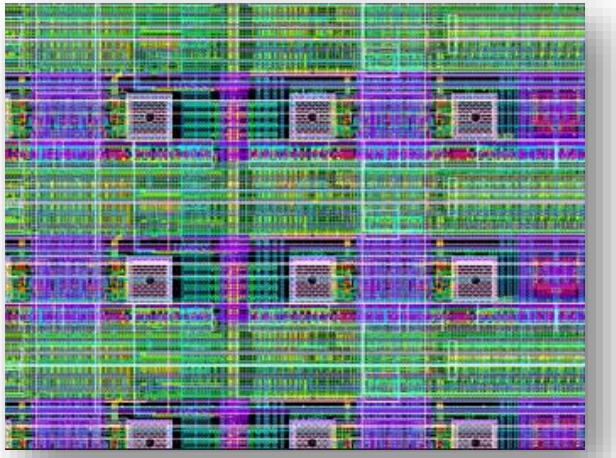
❑**MOST** High-Level Architecture



Monolithic Stitched Timing Prototype (**MOST**)

- Matrix in more details

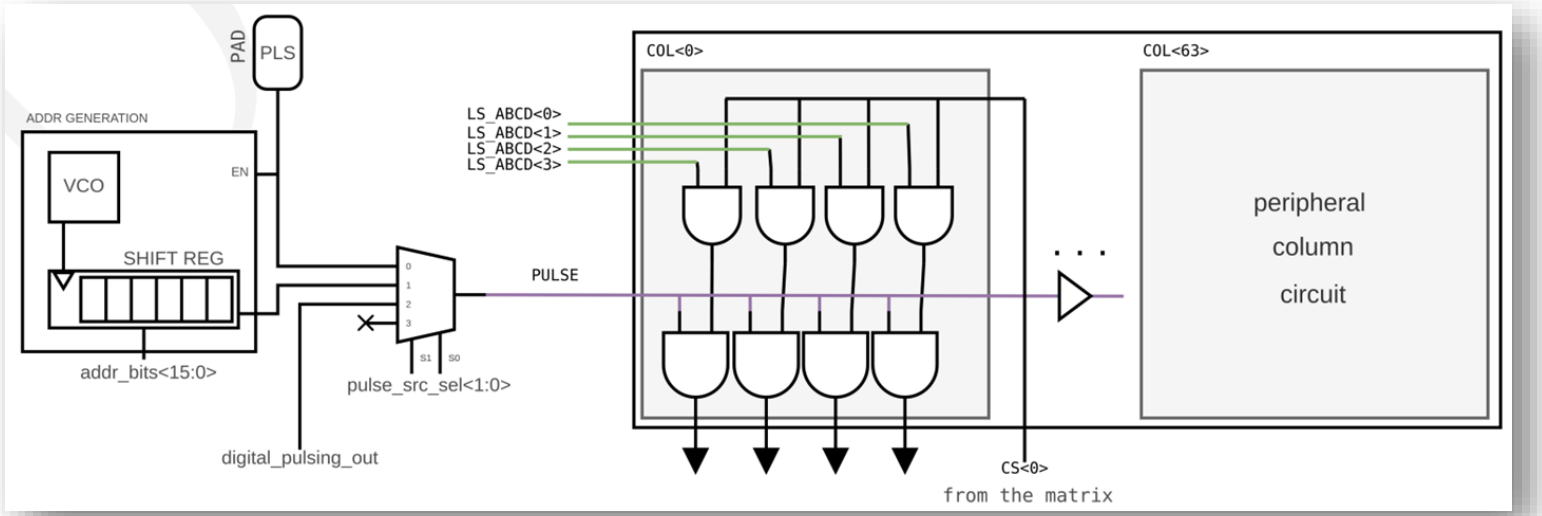


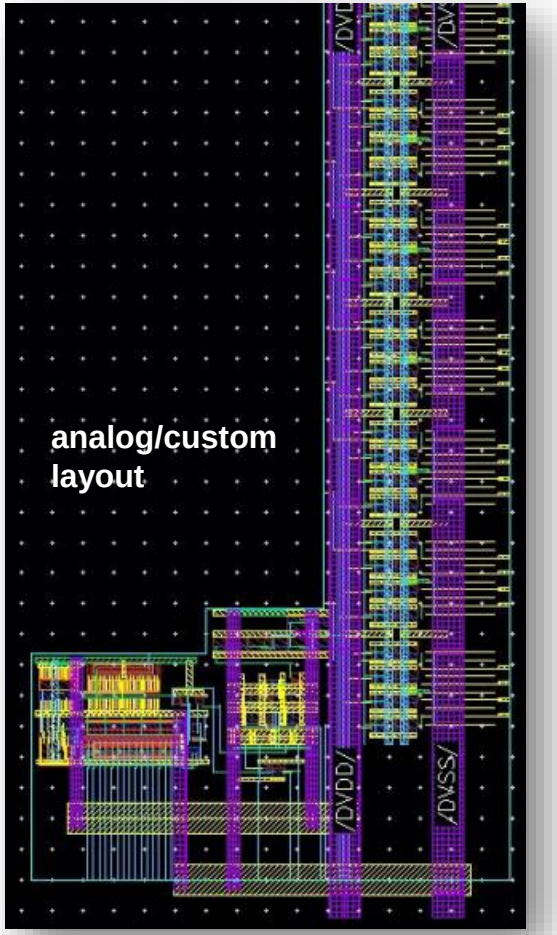


Matrix (zoom) layout

Monolithic Stitched Timing Prototype (**MOST**)

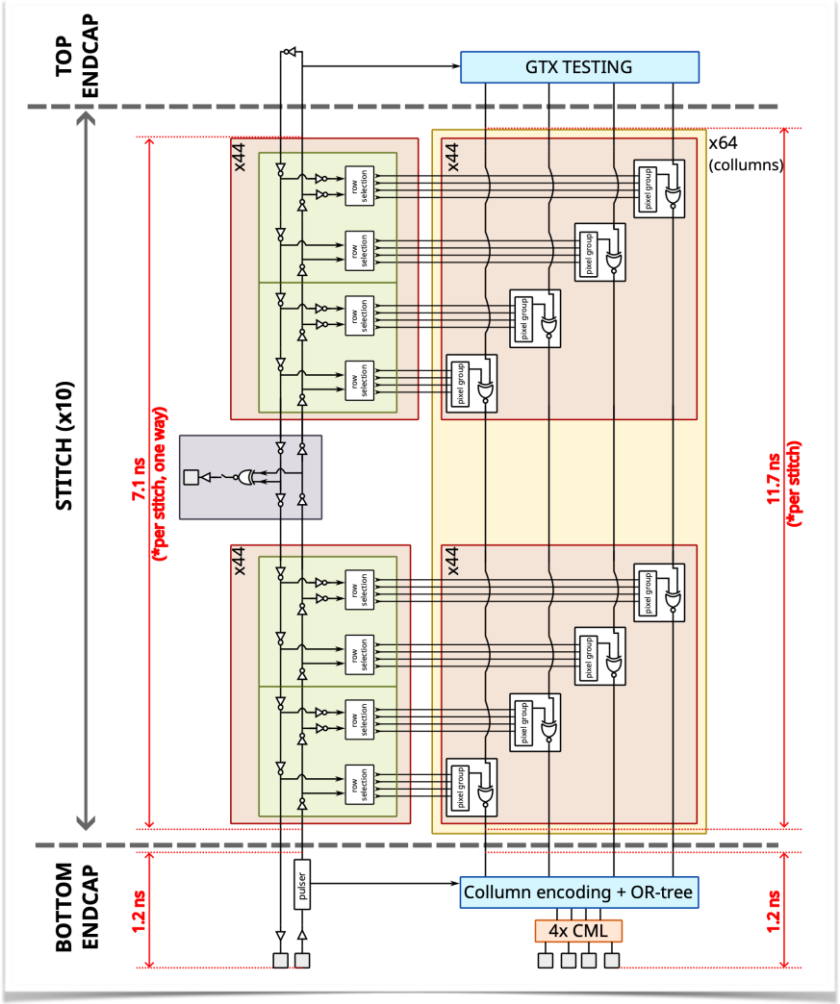
- TOP Periphery
  - Column Address Generator / Pulsing (test the 25 cm lines)





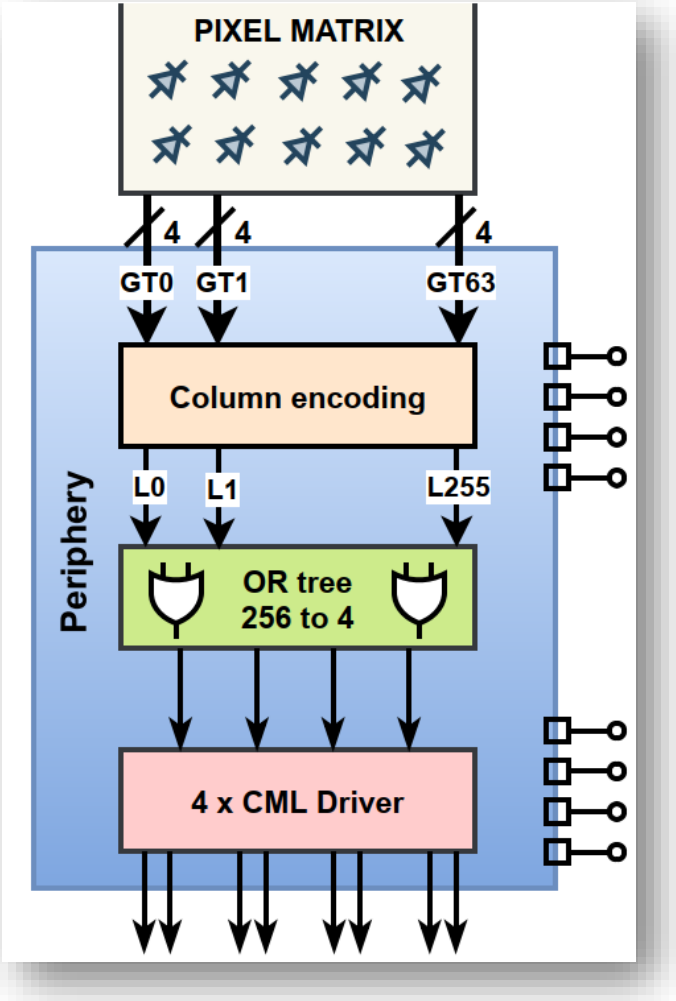
Monolithic Stitched Timing Prototype (**MOST**)

- Digital pulsing & readout
  - A test pulse can be fed at the bottom and travels across the full chip to the top and then back
  - Fired pixels send their address to the bottom
    - Bitstream of 1Gbps (programable)
    - There are 256 of these lines on MOST (4 per column)
  - Buffered several times along chip



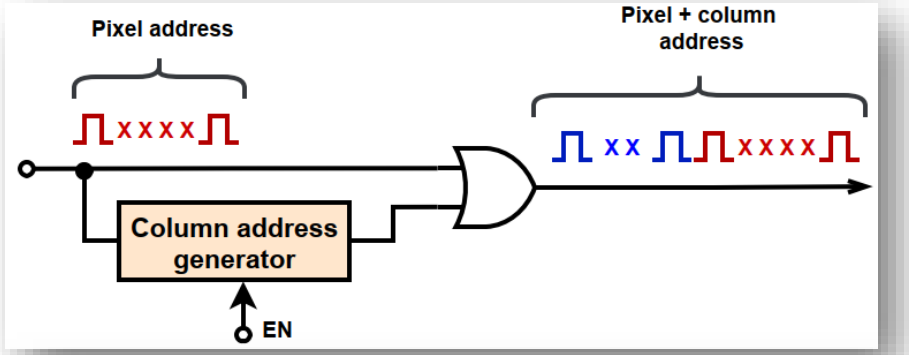
Monolithic Stitched Timing Prototype (**MOST**)

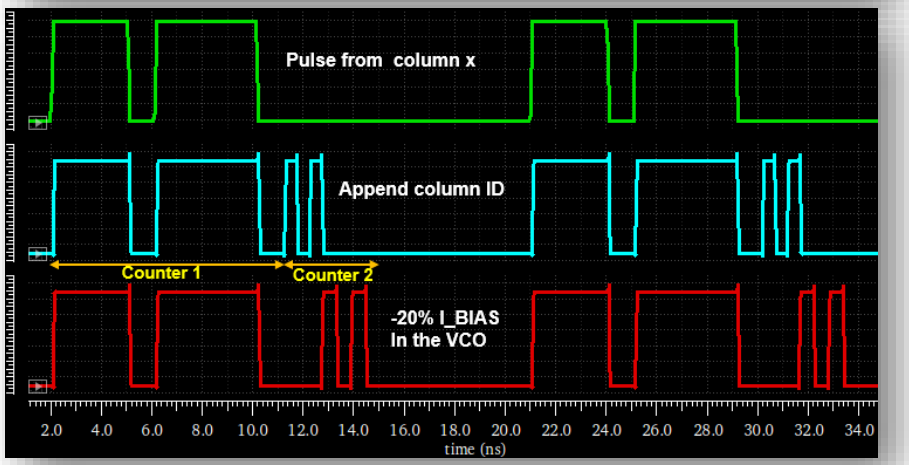
- Bottom Periphery
  - Peripheral circuits for encoding and merging the global columns:
    - Append column ID to the serial address
    - 64 x 4 = 256 lines to be merged into 4 output channels
    - Digital Pulsing Selector
  - Off-chip transmission:
    - 4 x CML Drivers

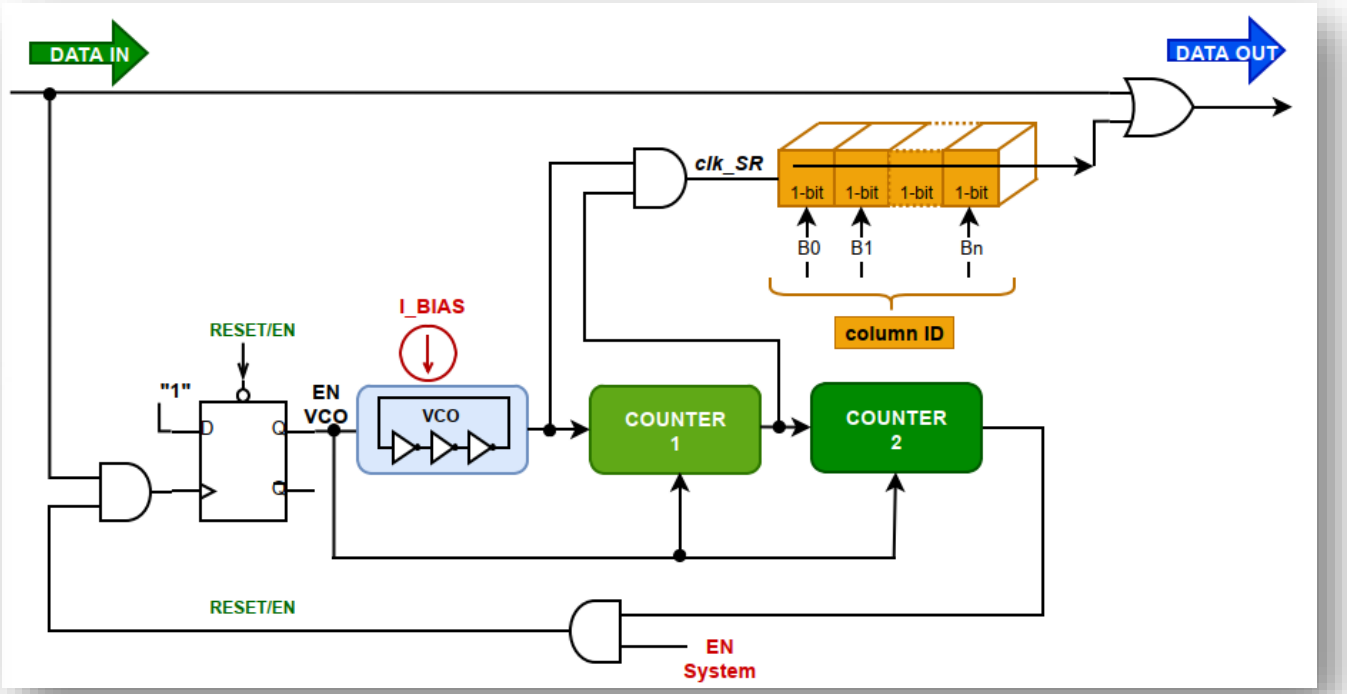


Monolithic Stitched Timing Prototype (**MOST**)

❑Bottom Periphery: Column Encoding Circuitry (256 units)

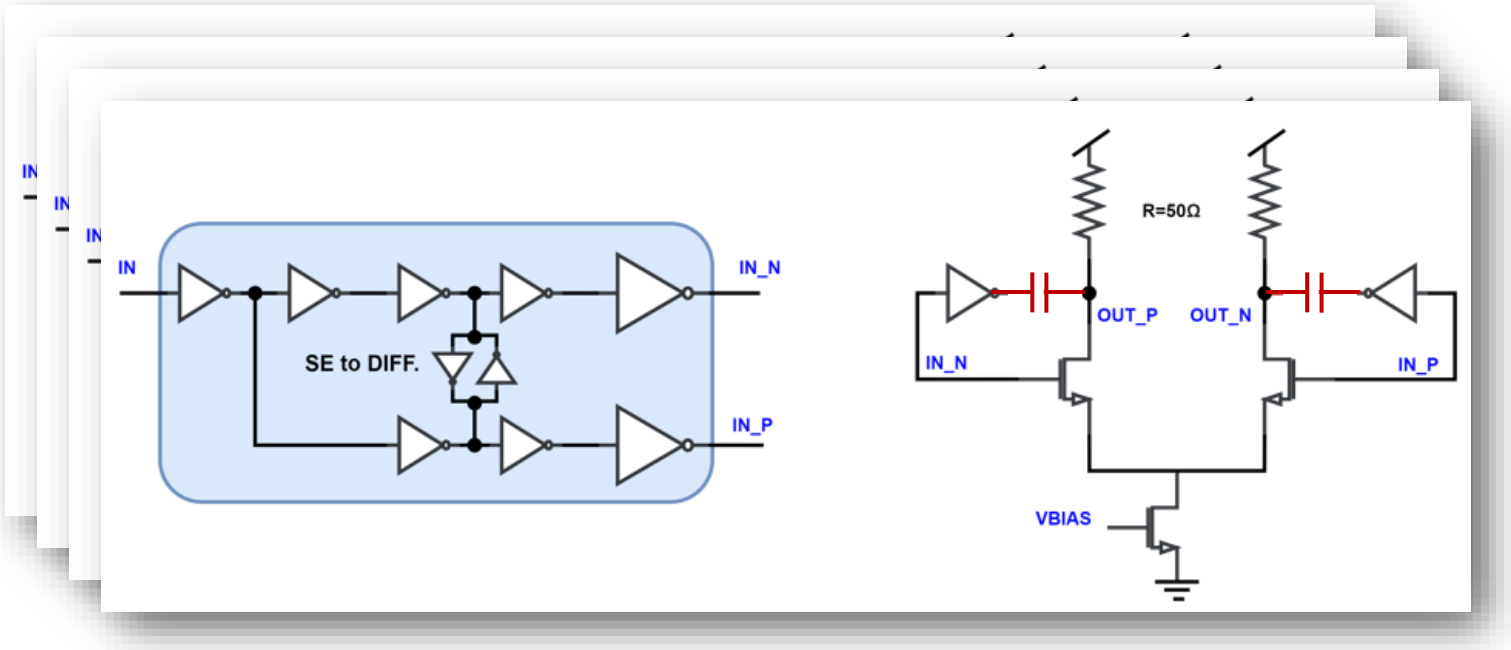






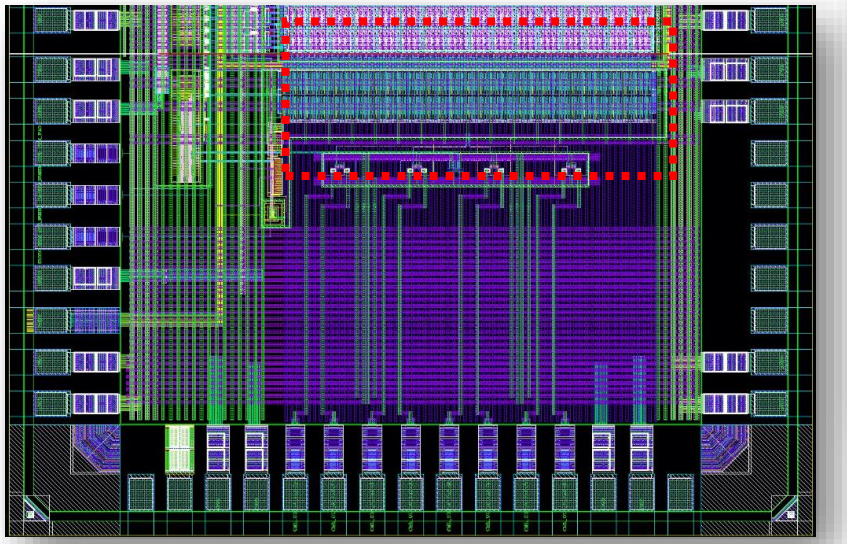
Monolithic Stitched Timing Prototype (**MOST**)

- Bottom Periphery: Off-Chip Transmission
  - 4 x CML Drivers (with adjustable BIAS)
    - Single-ended-to-differential converter
    - Capacitive pre-emphasis
    - BW up to 2GHz

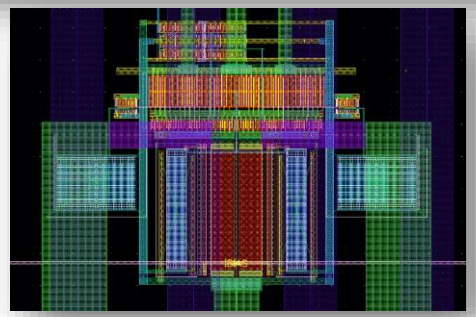


Monolithic Stitched Timing Prototype (**MOST**)

- Bottom Periphery
  - Analog/Custom Layout

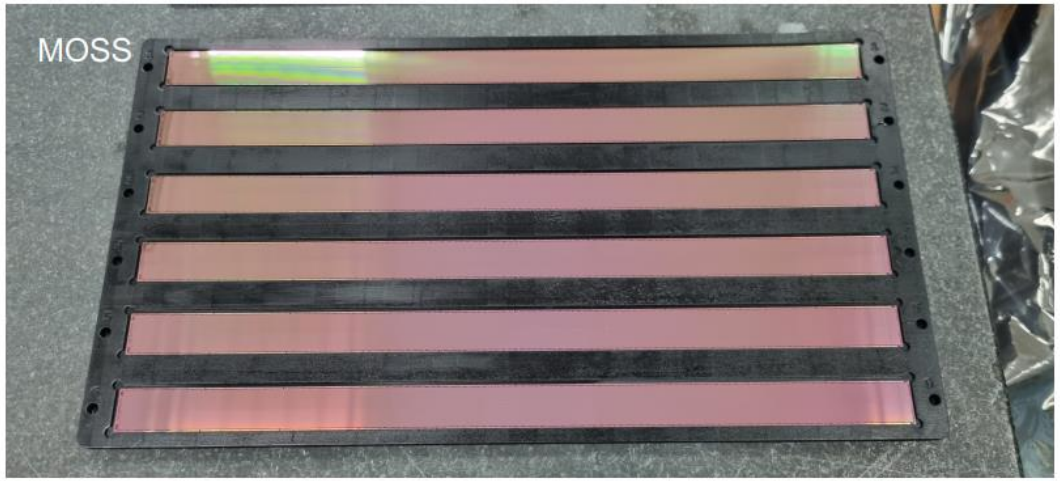


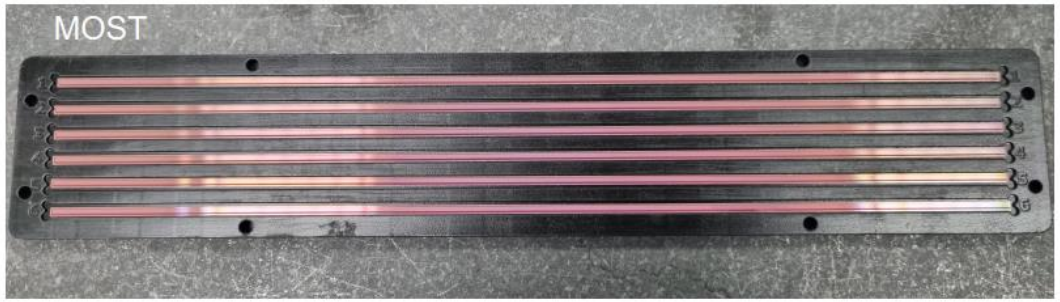
1.35 x 0.55 mm

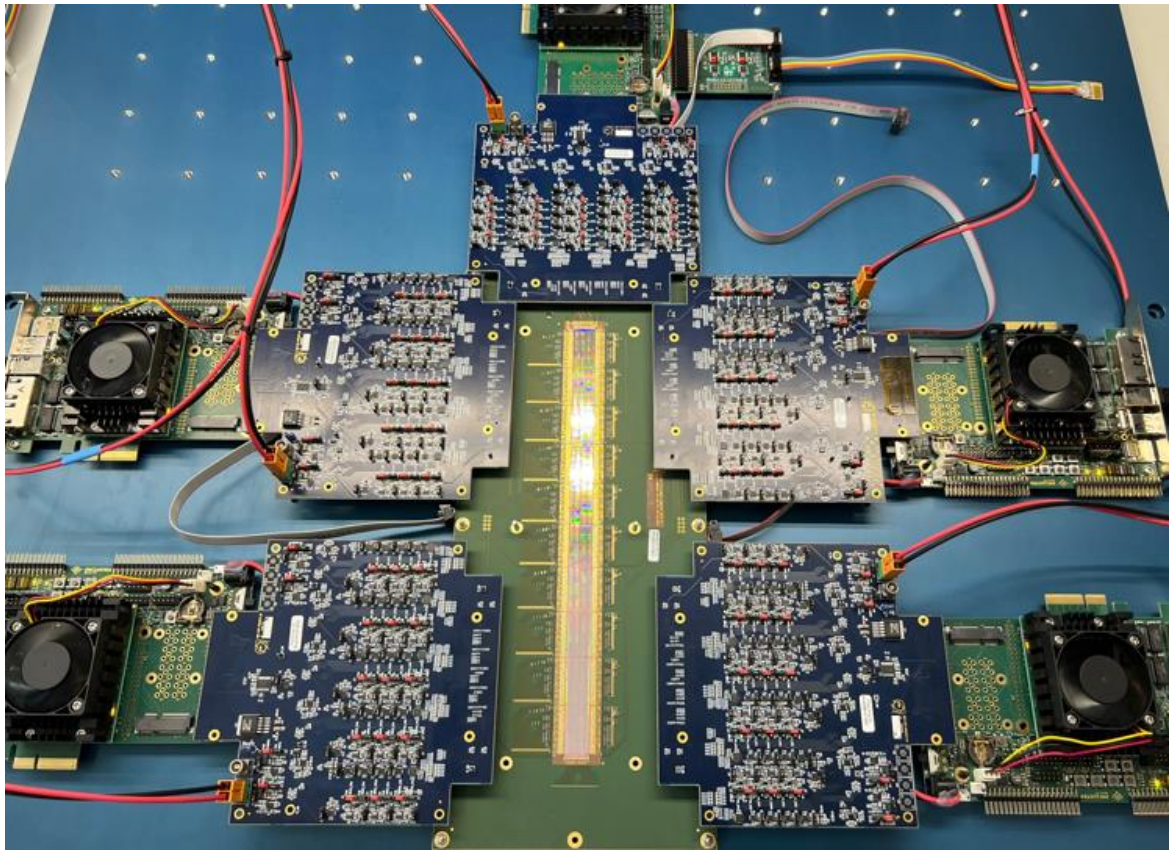


CML Driver layout

ER1 Dicing and Test System

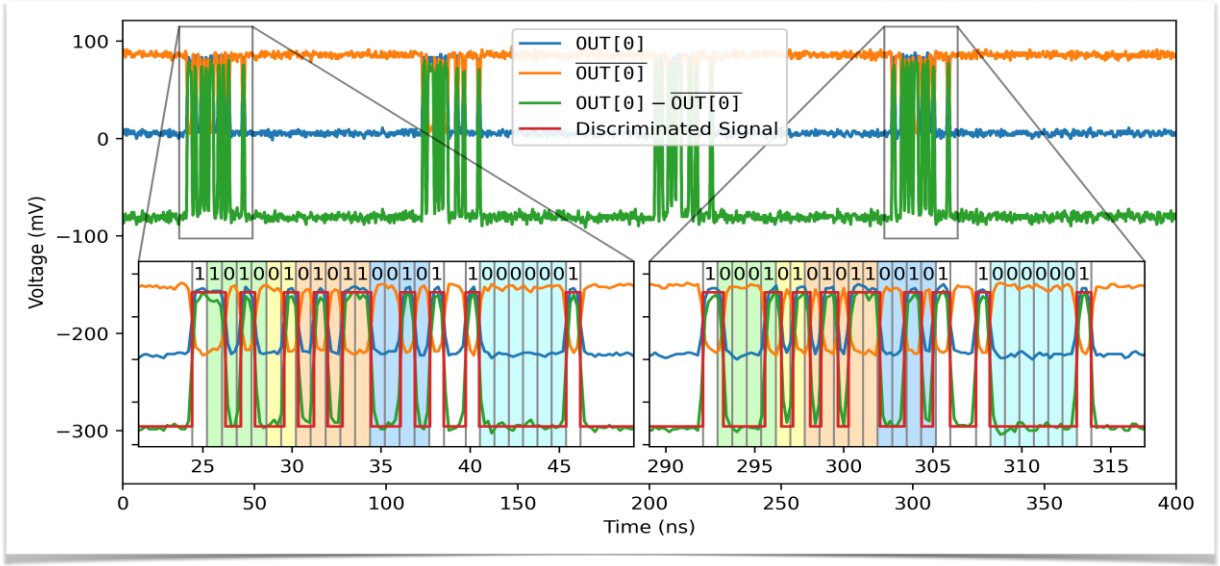


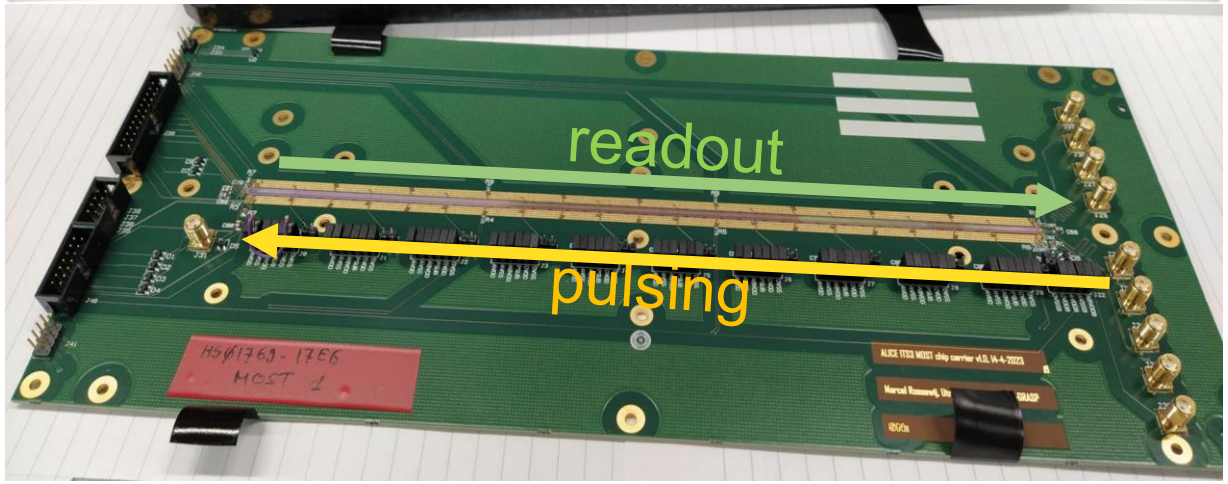




Measurement Results (MOST)

- Pulsing & Readout
  - All 256 readout lines work across the full length of the chip/across all stitches
  - Decoding of pixel addresses work nicely
  - Chip is functional, including front ends, sometimes pixel address is only transmitted partially
  - Detailed tests ongoing, also on behavior of pixels adjacent to powered down pixels



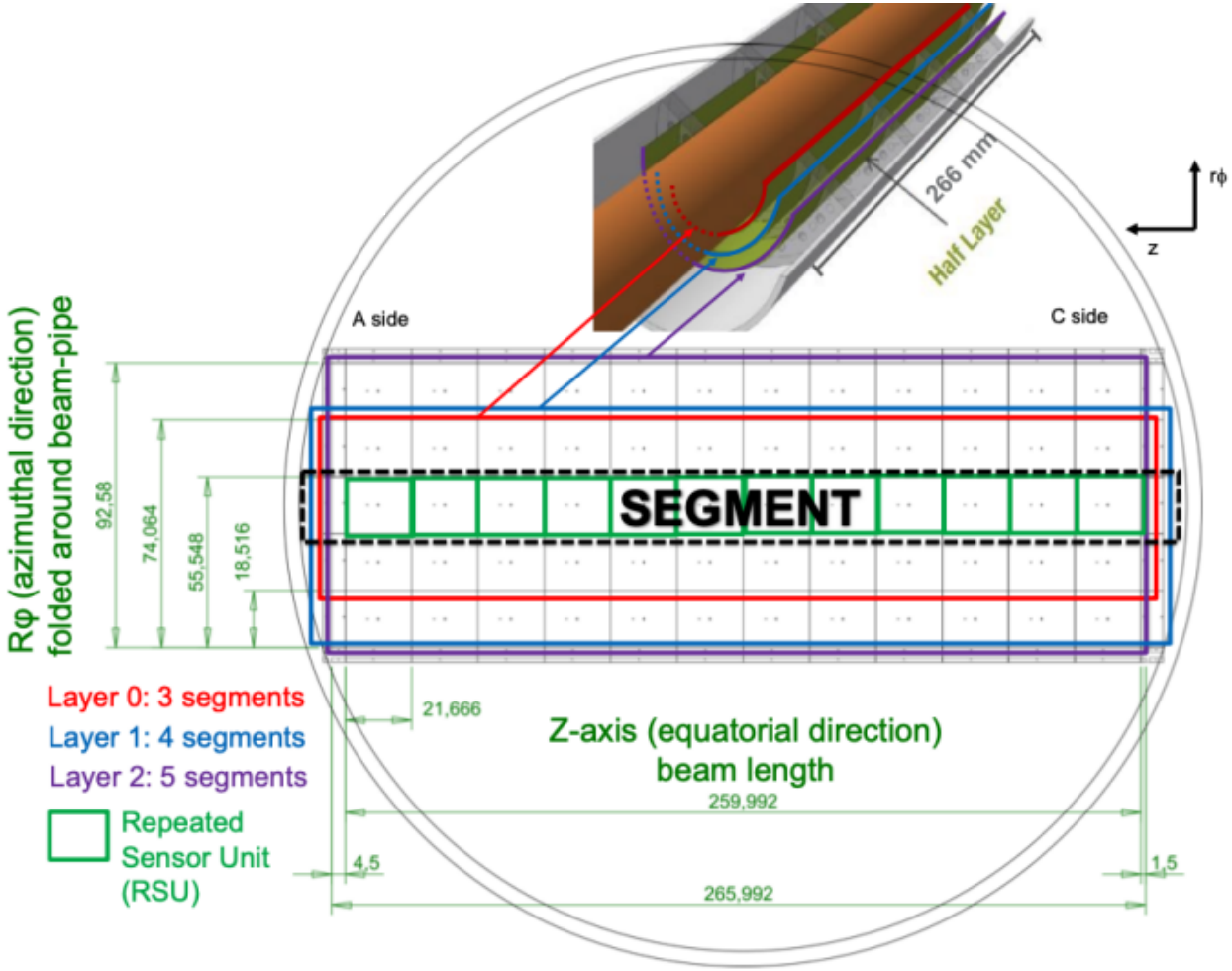


Monolithic Stitched Timing Prototype (**MOST**)

- Wafer-scale MAPS offer a unique possibility to build ultra-light, highly granular detectors
- Design Challenges
  - Metal spacing and width for **yield** (DFM)
  - Minimum channel length and space between devices for **yield**
  - Readout due to a large area of pixels/information
  - **Power** supply routing to minimize voltage drops
    - Power supply regulation?
  - BIAS generation and distribution (voltage *vs* current)

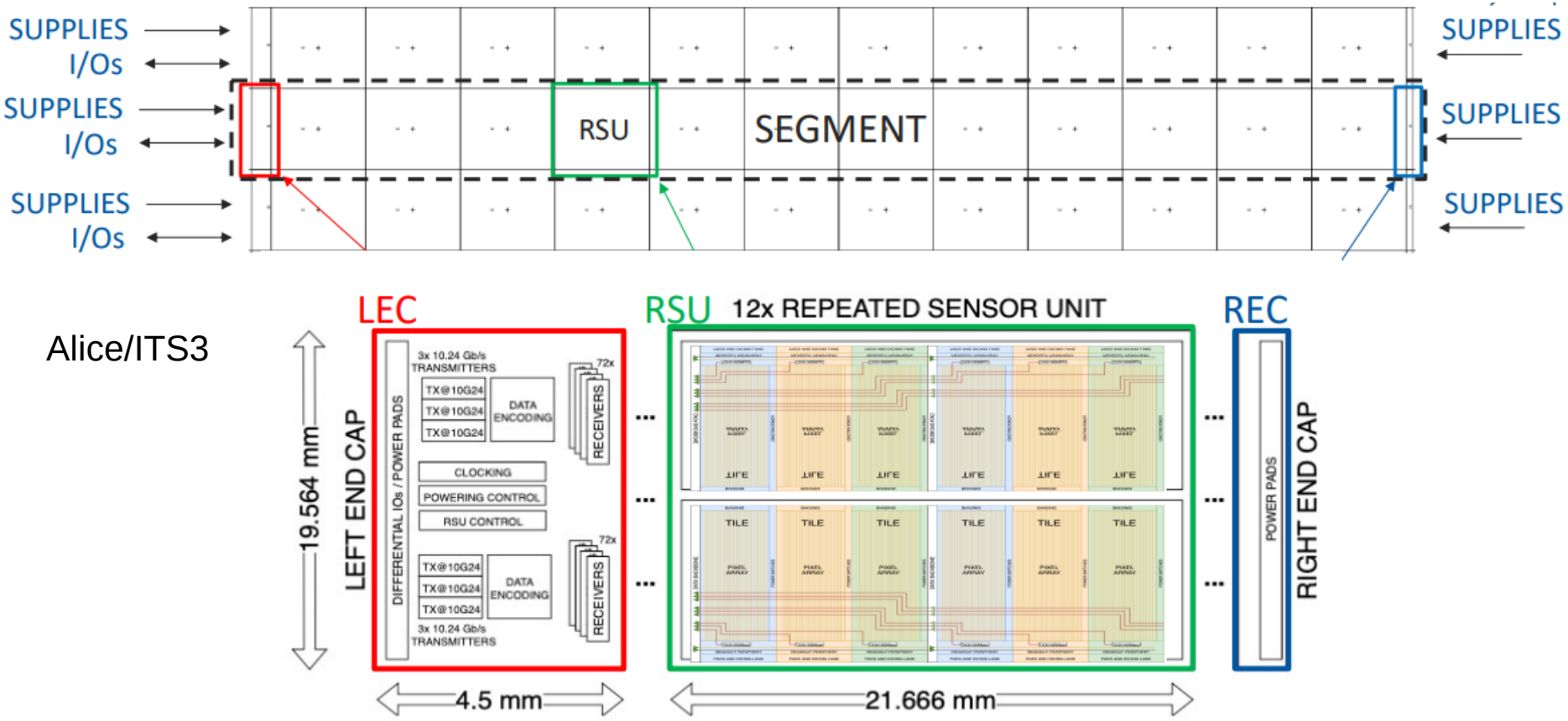
MOSAIX (ER2) - Sensor Dimensions

- Wafer scale sensor design using the stitching technique
- Process: TPSCo 65 nm CMOS Imaging Sensors(customized)



Alice/ITS3

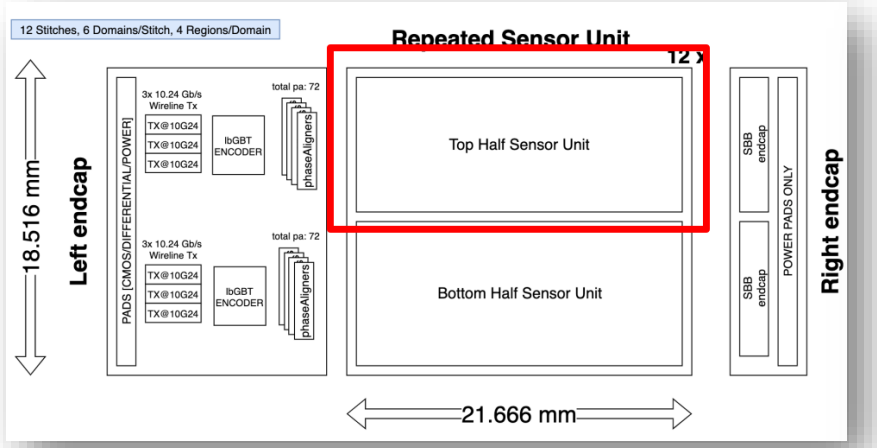
MOSAIX (ER2) - Top Integration Diagram

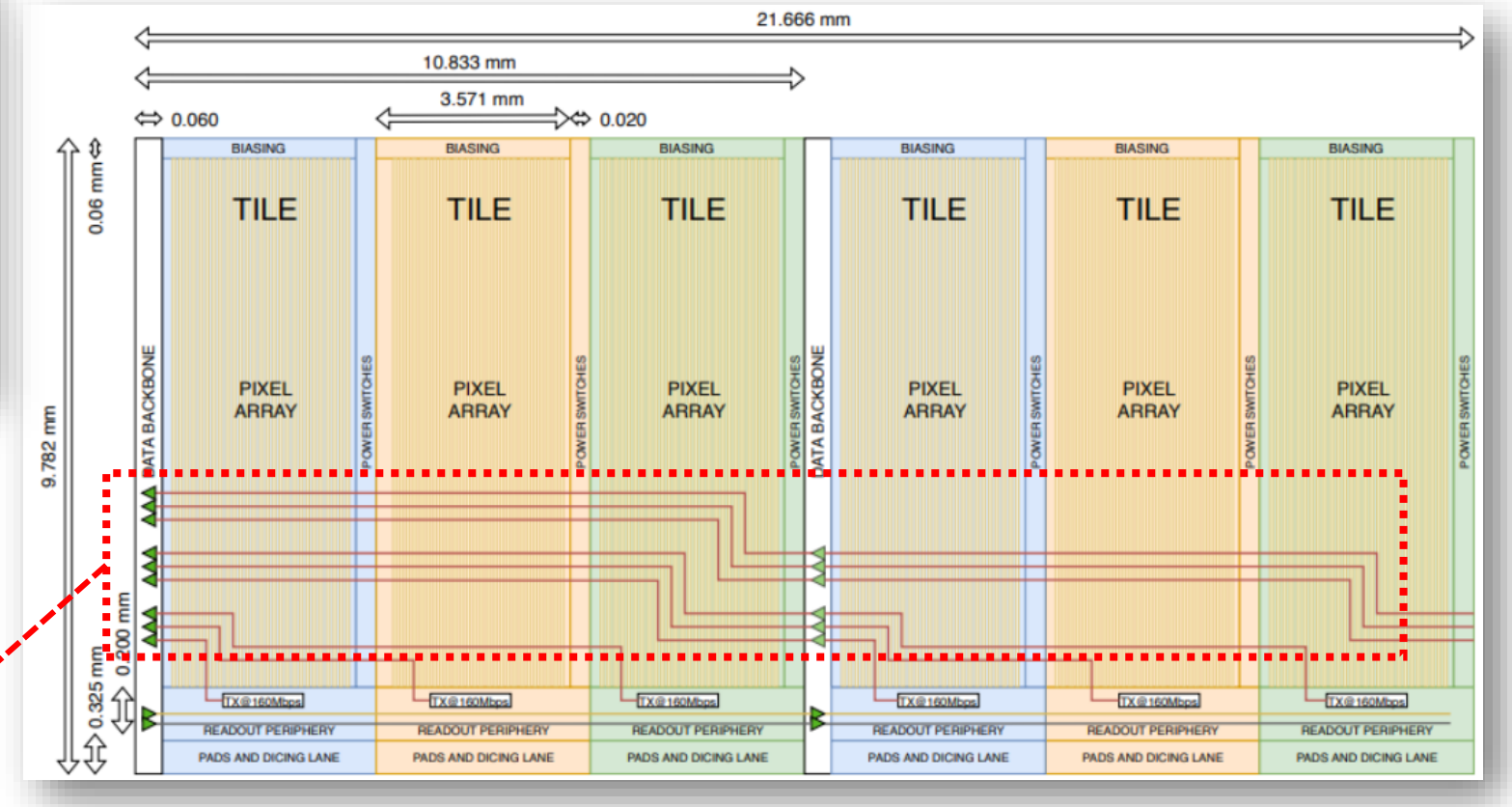


Alice/ITS3

Figure 3.34: Block diagram of the sensor segment.

ER2 Stitched Sensor (MOSAIX)



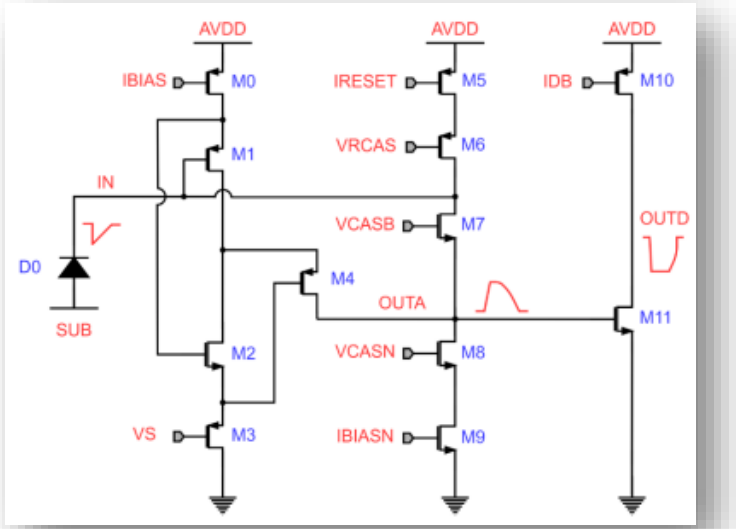


- **Fill factor ~93%**
- Depending on ER2 results, optional removal of test pads for final design would provide **~95.5%**

  - Redout Link @ 160Mb/s

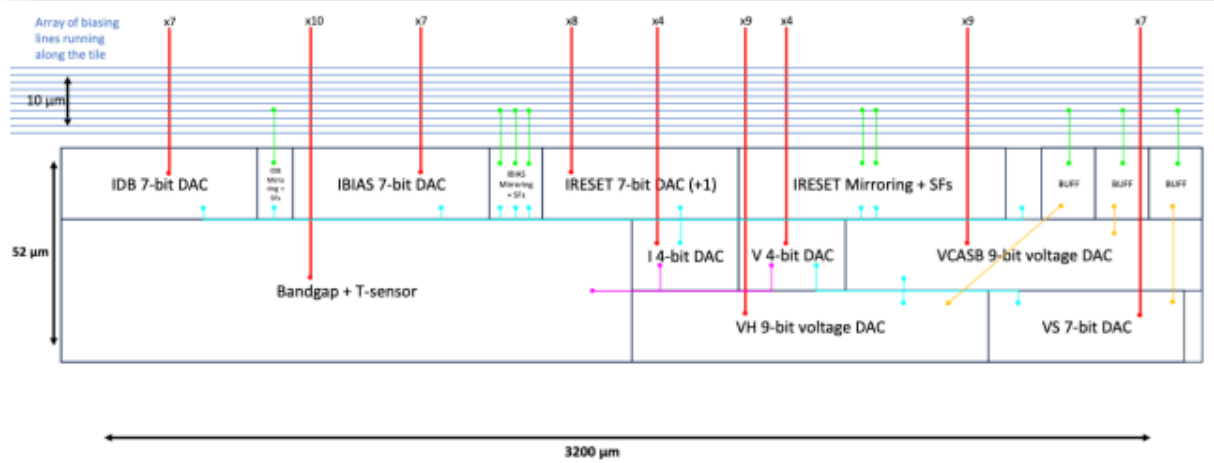
Front-End and Biasing

- **Evolution path**
  - DPTS -> MOSS -> MOSAIX
    - ✓ Improving transistor sizing and new layout



Alice/ITS3

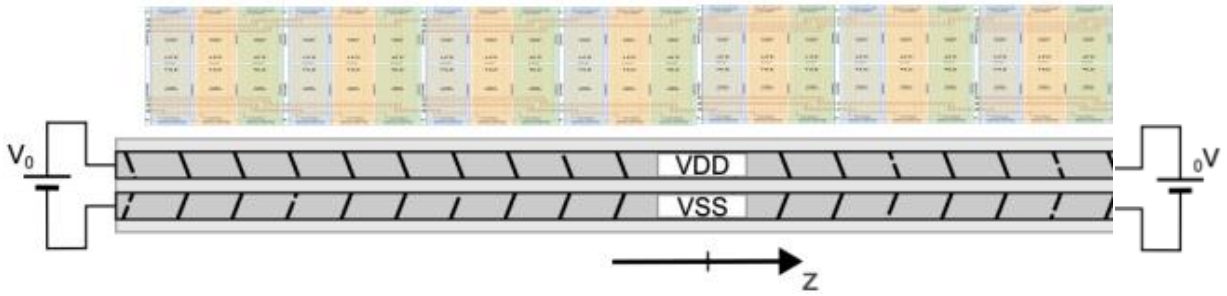
Unit Biasing (per Tile)



Specification	Value	Comment
Current consumption	< 30 nA	IBIAS + discriminator standby current
Dynamic energy (@ 600 e)	≤ 10 pJ	No hard spec. as negligible wrt total power
Nominal threshold	$\approx 150\ e$	¼ of MIP
Equivalent Noise Charge	$< 18\ e$	
Threshold mismatch	$< 18\ e$	
Gain (@ threshold)	$> 400\ \mu V/e$	Simulated avoiding discriminator kick-back
Phase margin	$> 45°$	
Time of Arrival	$< 1\ \mu s$	
Time over Threshold (@ 600 e)	$\ll 1$ ms	For lost hit probability $< 1\,\%$
Threshold sensitivity vs supply drop	$< 2\ e/mV$	Supply drop on AVDD and AVSS
Detection efficiency	$> 99\,\%$	

Table 3.5: Analog front-end characteristics.

Power Domains, Currents and IR Drops



Supply purpose	Nets	Voltage [V]	Current [mA]	Pads on LEC	Pads on REC
Services	SDVDD-SDVSS	1.2 to 1.32	227	Yes	Yes
Global analog	GAVDD-GAVSS	1.2 to 1.32	540	Yes	Yes
Global digital	GDVDD-GDVSS	1.2 to 1.32	1369	Yes	Yes
Serializers	TXVDD-TXVSS	1.8	200	Yes	No
Substrate bias	PSUB	−1.2 to 0			

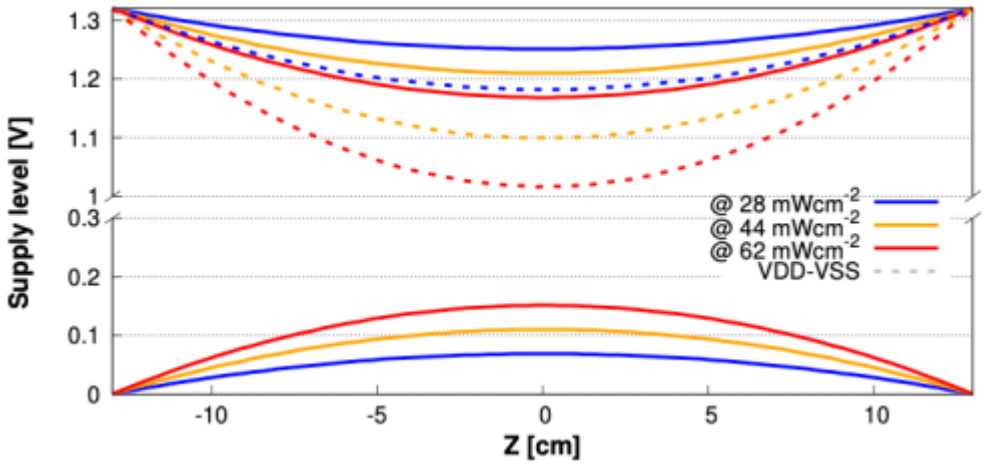
Alice/ITS3

❑On-chip LDOs?

- Increases complexity and power dissipation

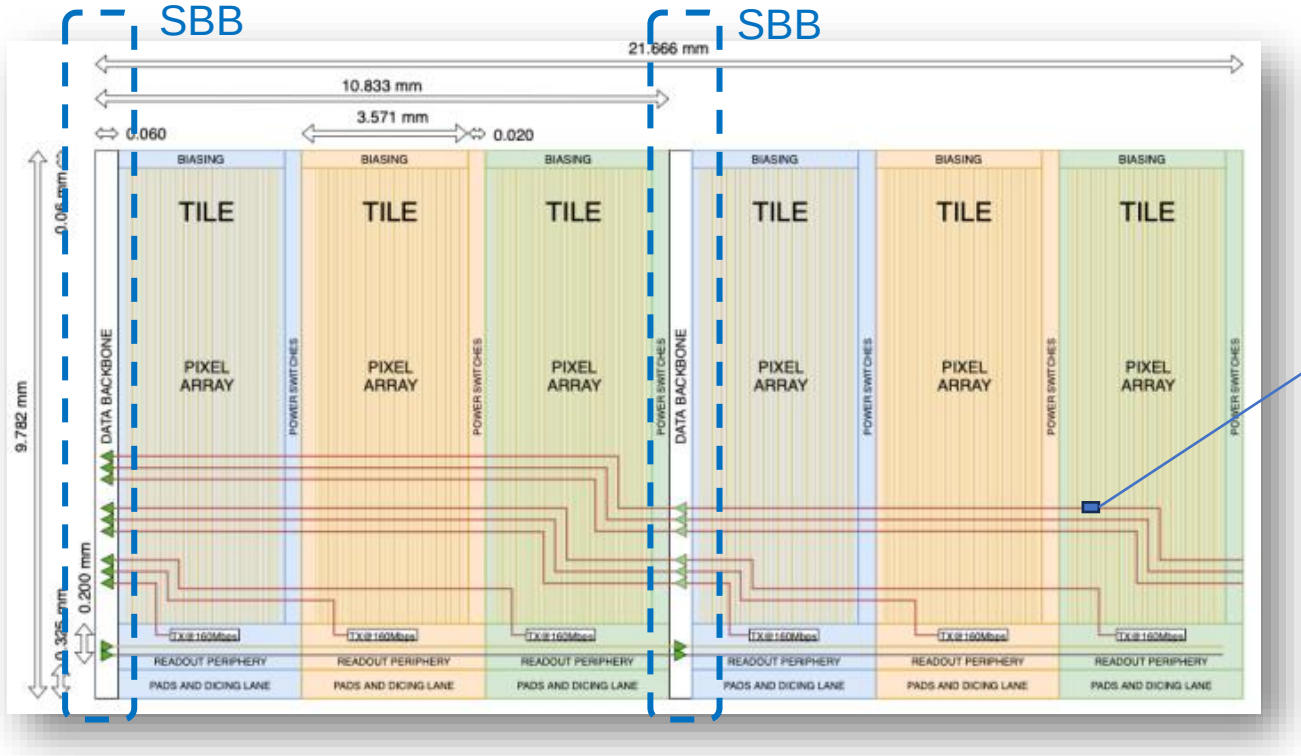
❑Estimates of IR drops

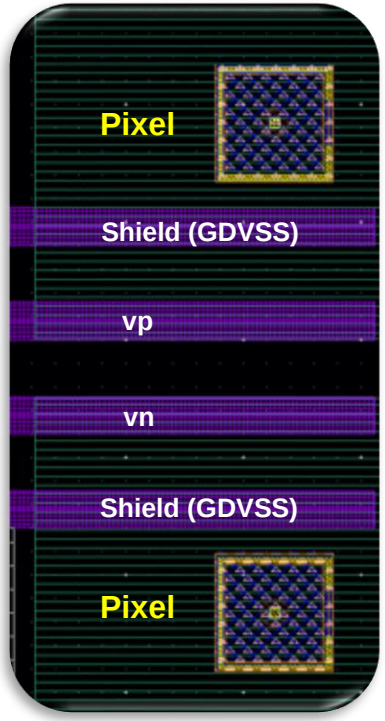
- Simple model, one global domain
- Assuming *new* metal stack (tick metal)



Data Readout / SBB

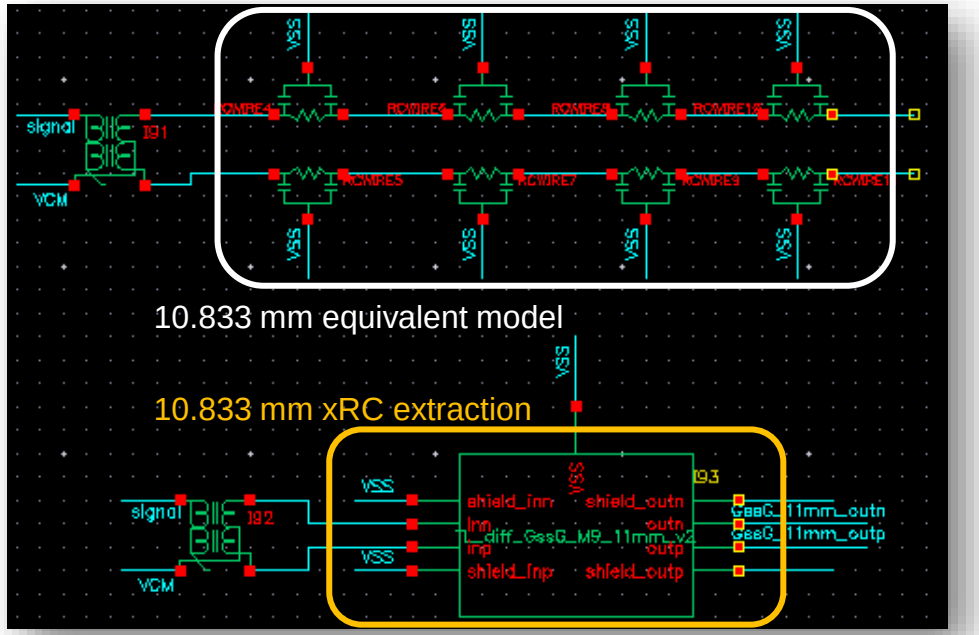
- Differential transmission scheme with low voltage swing
  - Power efficiency, immunity to supply noise, reduction of noise injection into sensing analog nodes

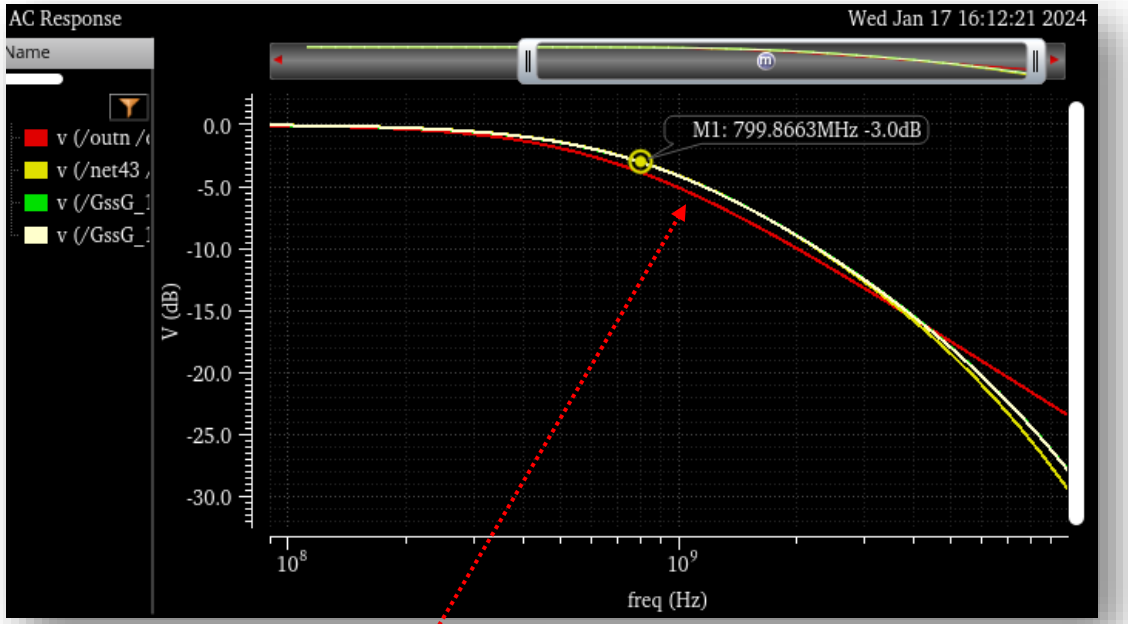


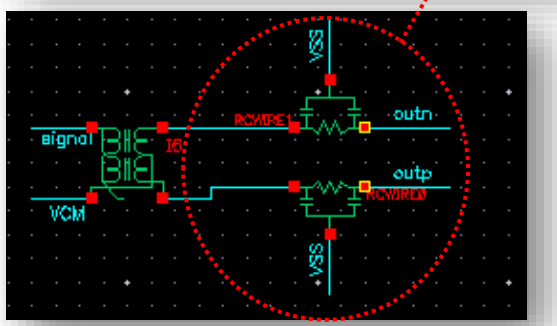


- Parasitic extraction (PEX)
  - R=16 Ohm/mm (22 Ohm worst)
  - C=0.24 pF/mm (0.3 pF worst)

Line Model and AC Analysis



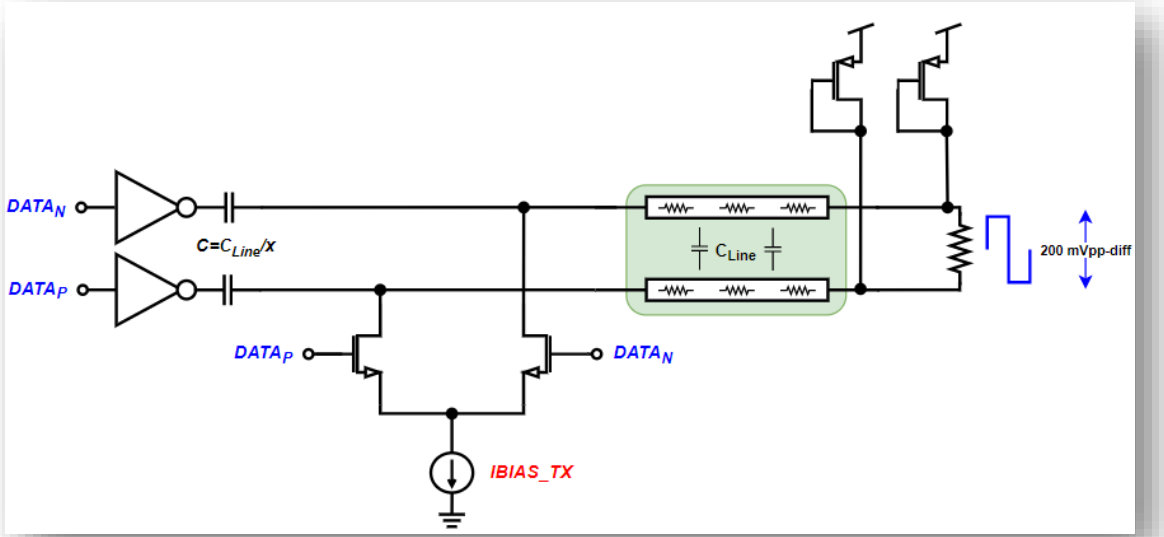


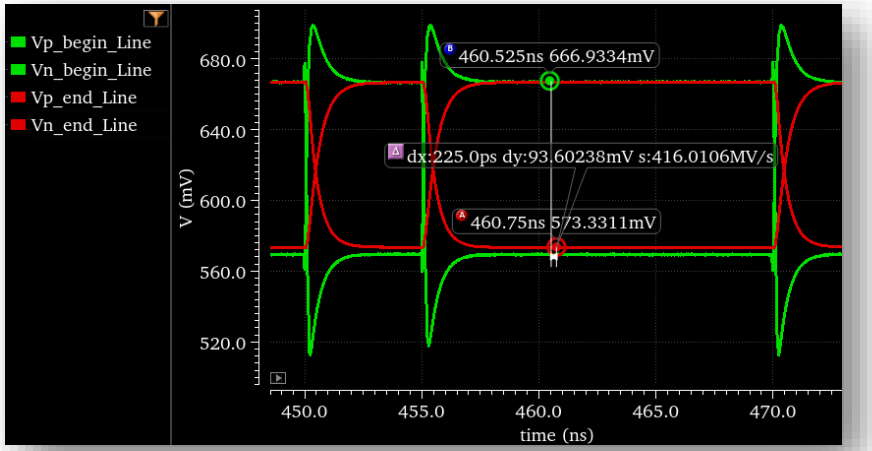


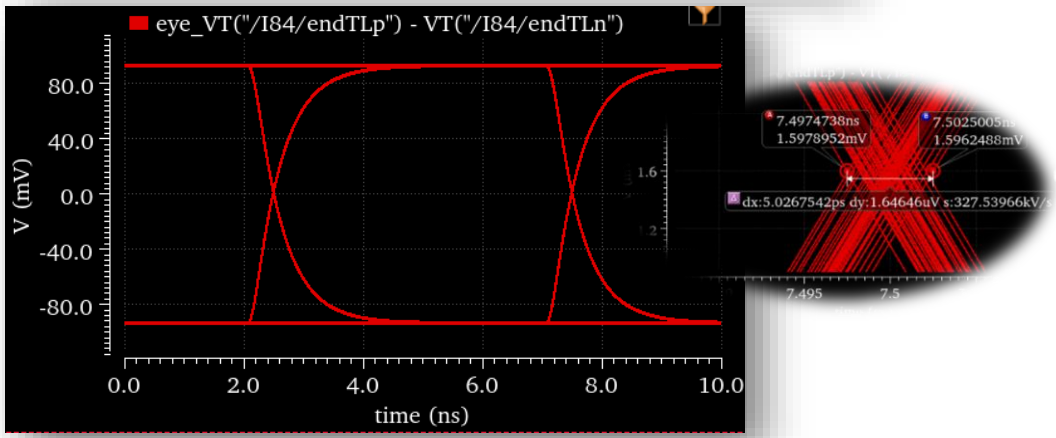
- 4 x RCWIRE model has the same response as the extraction
- For a TL length ≈ 10.833mm
  - BW-3dB ≈ 800MHz
- Single RCWIRE model has a slightly different AC response compared to the extraction

SBB - Transmitter Scheme

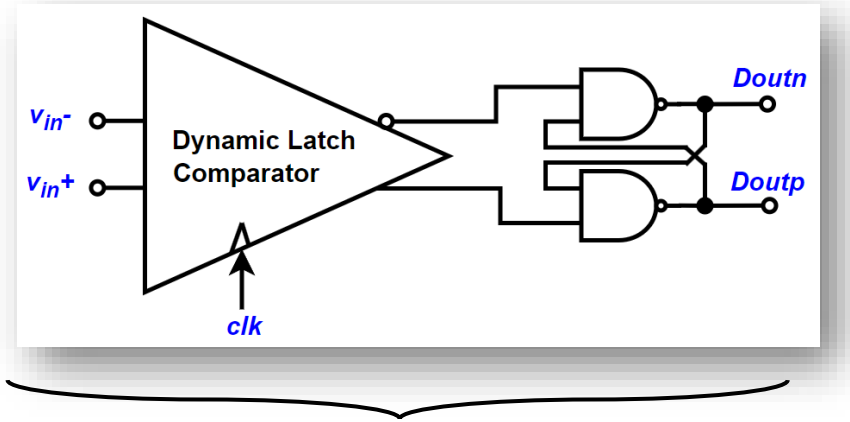
- Capacitive Transmitter with low swing signals for energy efficiency
  - Charging a fraction of the capacitance of the Line (ratio depends on a minimum required swing over the line)
  - Energy $\propto \boldsymbol{C} \cdot V^2$



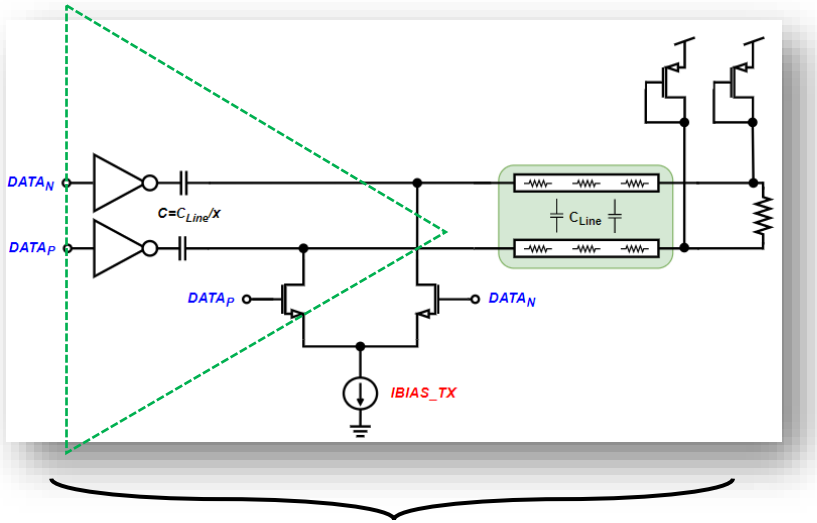




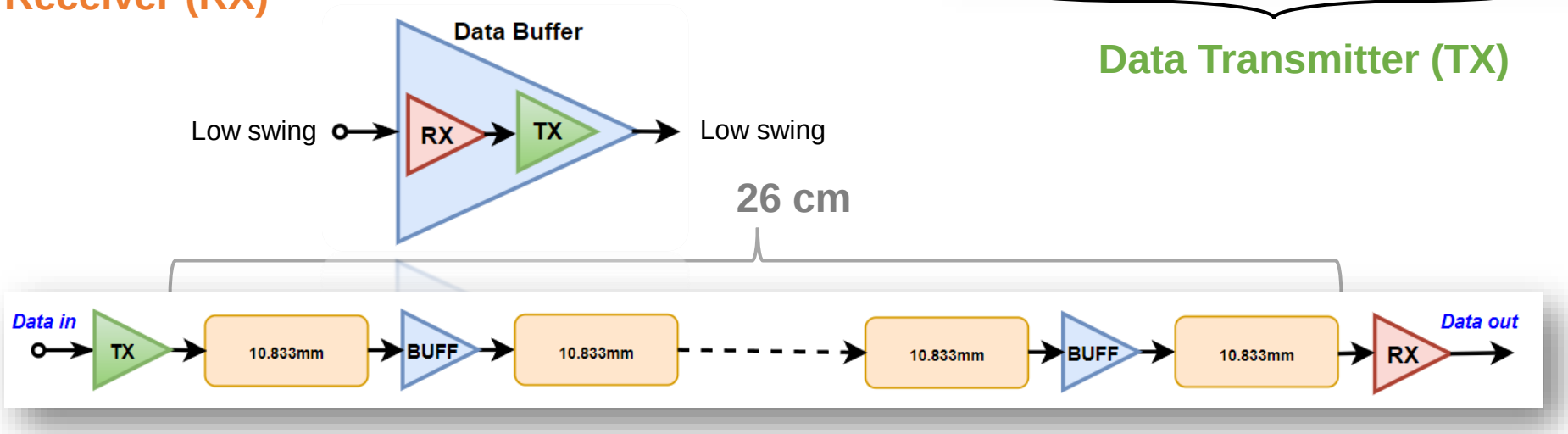
SBB – 160Mbps **Data Buffer** (RX + TX)



Receiver (RX)



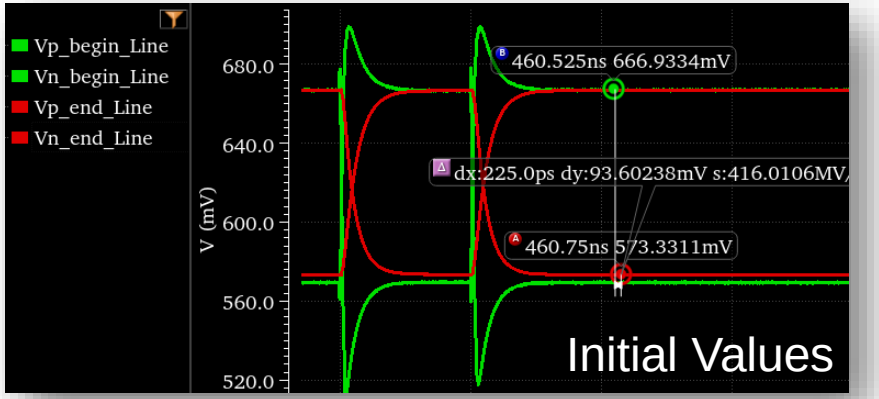
Data Transmitter (TX)

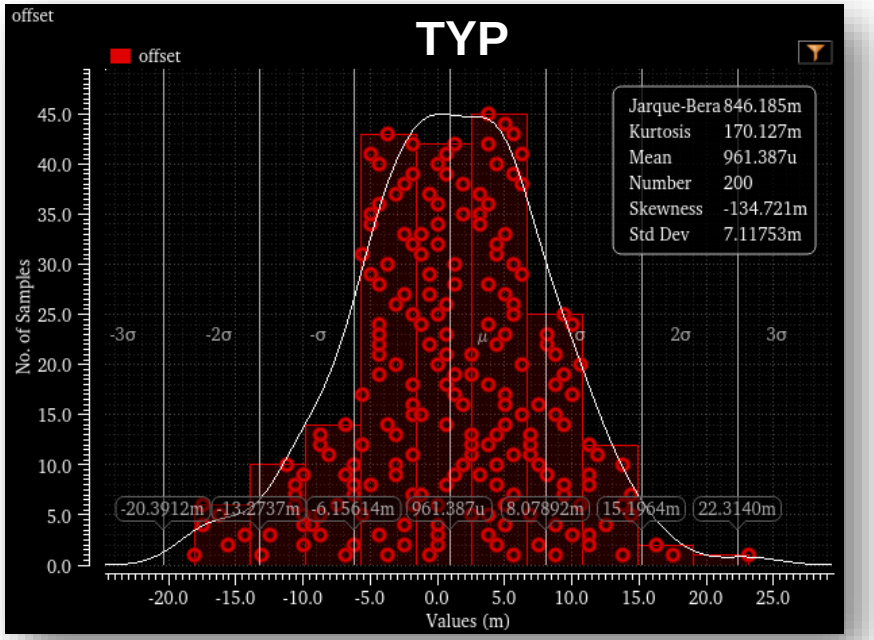


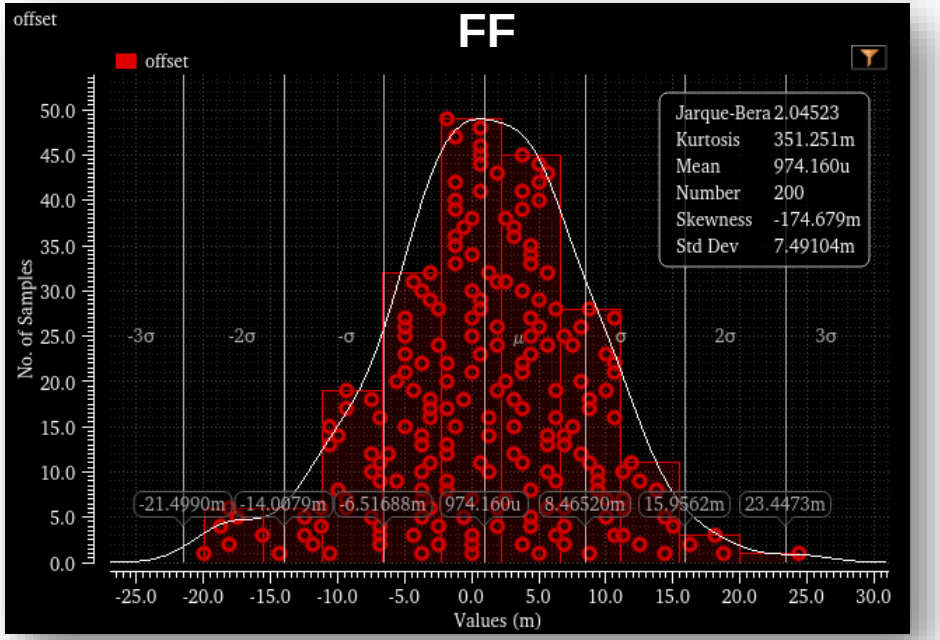
Clocked Comparator

- Dynamic comparator **offset** (diff. input)

4σ < ±30mV (margin to reduce the swing over the line)

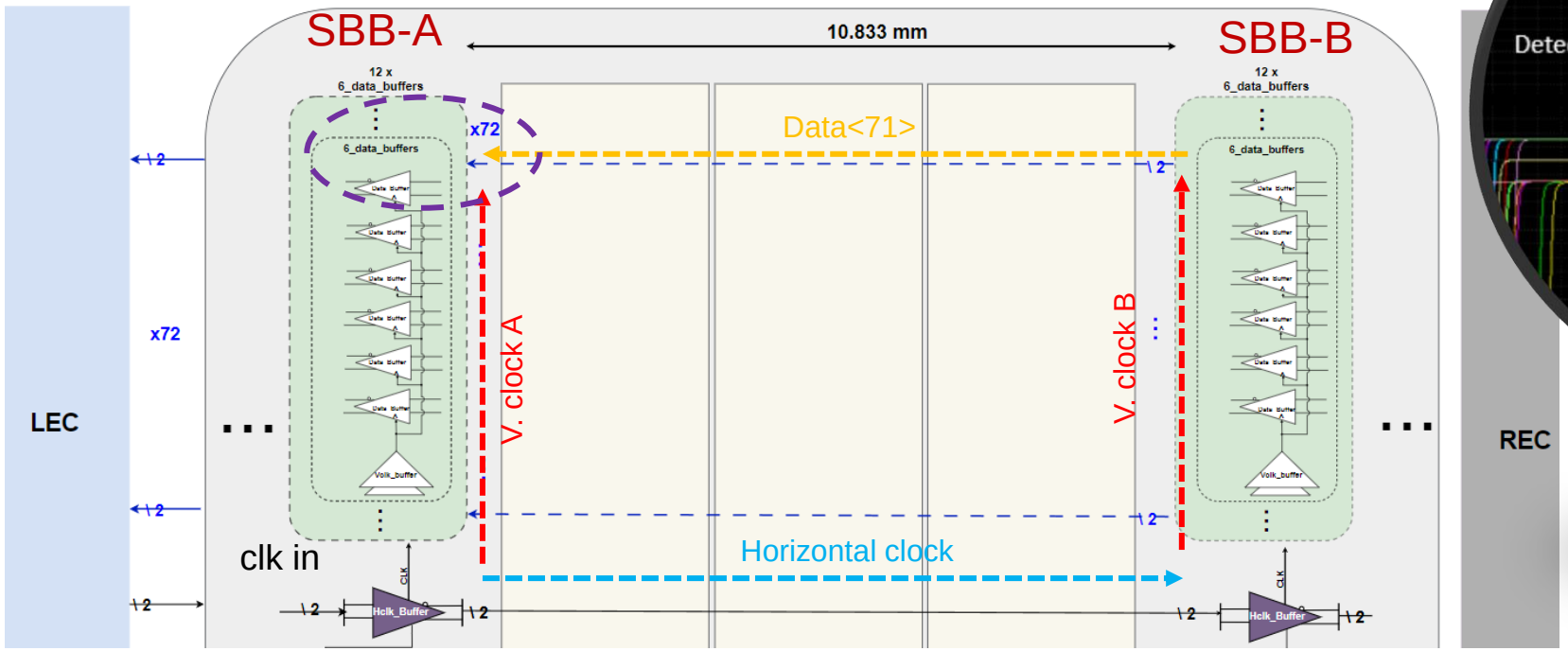


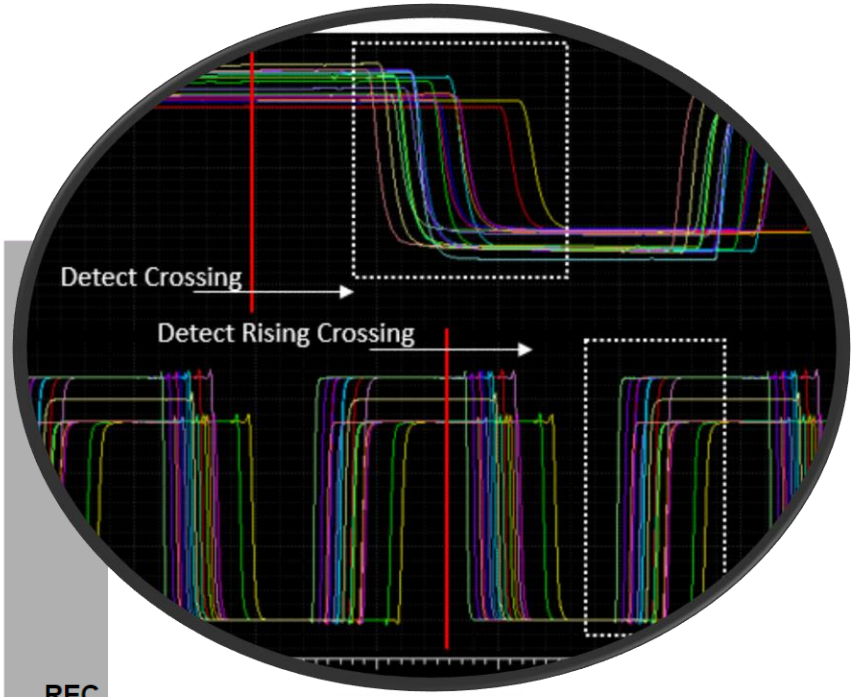




Timing analysis between SBB (Verification)

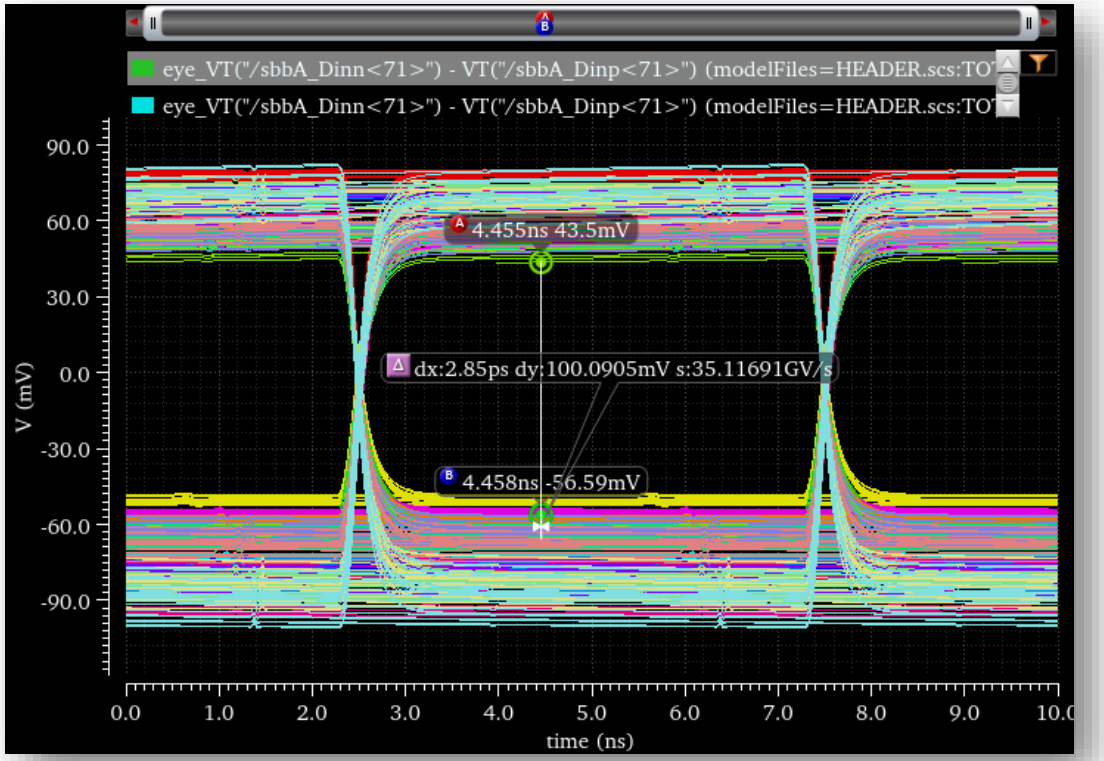
- Timing analysis of the loop @ the last Data Buffer / clk over PVT





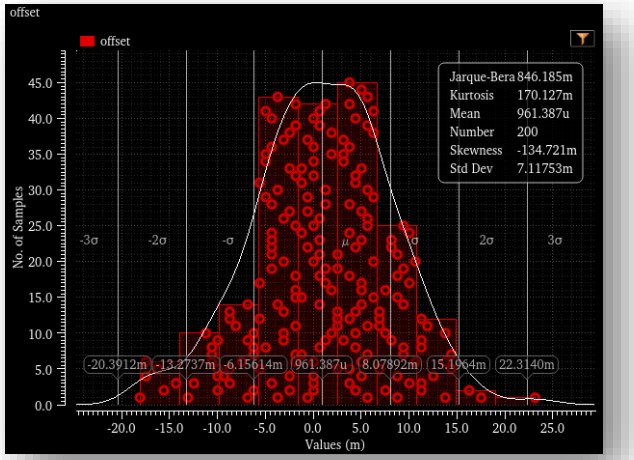
Simulation Results / Validation

- Eye diagram over corners (PRBS generator)



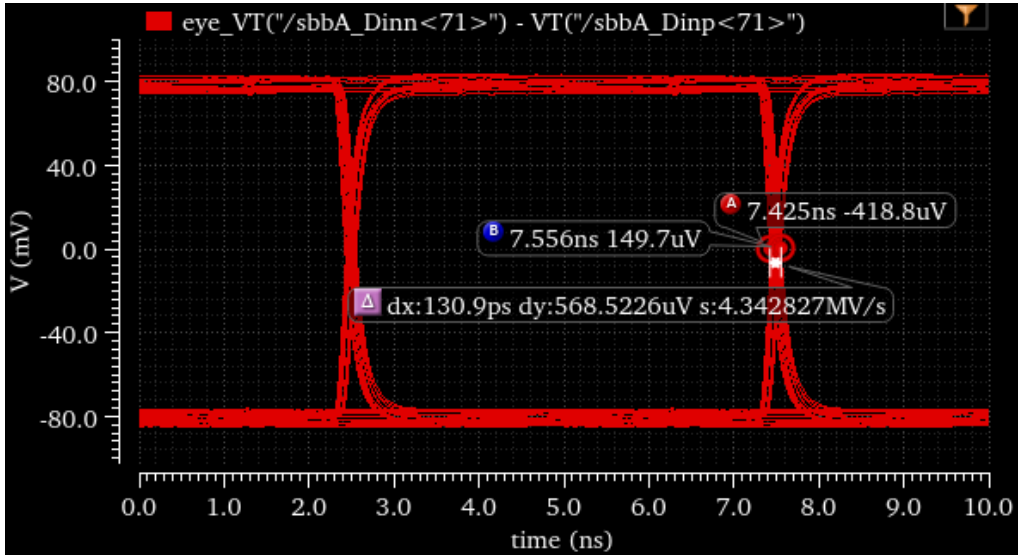
- **16 Corners**
  - MOS: SS SF FS FF
  - Temp: -20 +65 C
  - Supply: -10% 10%
- Line model **RC worst**
  - R=22 Ohm/mm
  - C=0.3 pF/mm

✓ During the design process, the DATA TX amplitude was optimized to accommodate, in the worst corner, the offset of the comparator with some margin (4σ of ±30mV plus ±20 mV).

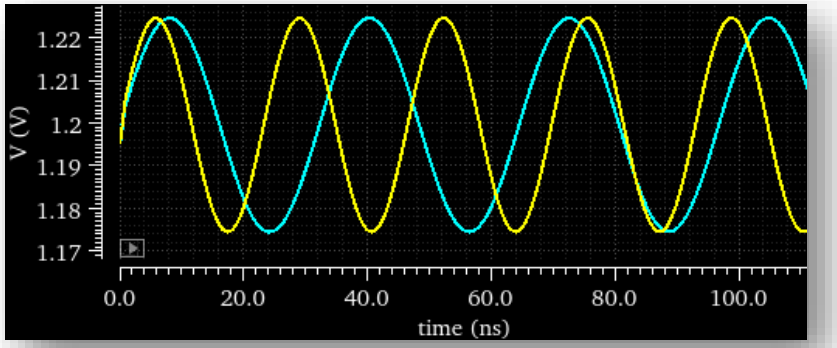


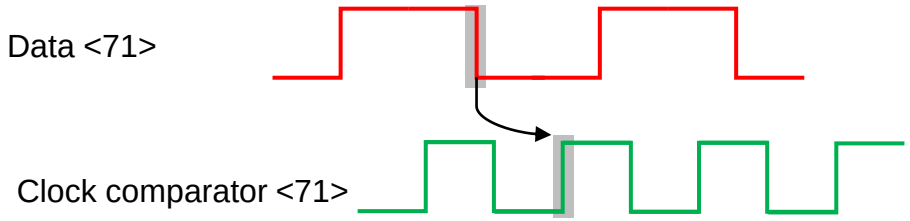
Simulation Results / Validation

- Eye and clock considering noise:
  - Transient noise (fmax=10G)
  - VDD_SBB-A with 50mVpp sine wave @31MHz
  - VDD_SBB-B with 50mVpp sine wave @43MHz



Supply noise





SBB – Power Improvements (Ongoing)

❑Power update TDR

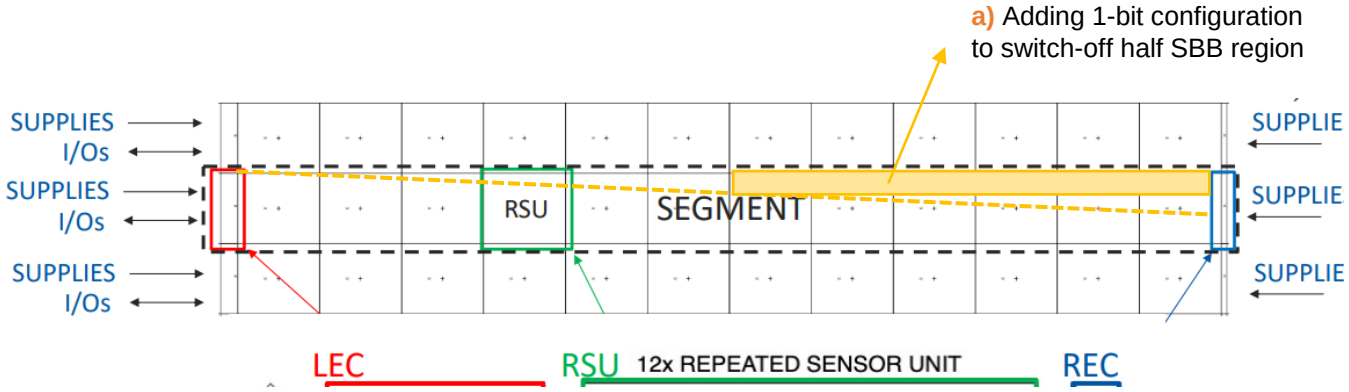
Table 3.9: Estimates of power consumption of the circuits composing one repeated sensor unit (RSU). All values are for 25 °C temperature and 1.2 V supply voltage. Changes of operating settings determine the increase between the nominal and maximum DC values. Process variations determine the increase between the expected and maximum leakage values.

	Power [mW]						
	DC		Dynamic	Leakage		Total	
	Nominal	Max		Expected	Max	Expected	Max
Analogue pixels	30	50				30	50
Digital pixels			0.2	12	32	12	32
Digital columns			2.7	16	42	18	44
Biasing and monitoring	4.3	4.3				4.3	4.3
Readout peripheries			36	1.3	3.4	37	39
Data backbone	11	11	5		13.3	16	16
RSU Total	45	65	44	29	77	118	185

(4.24 cm^2) 115

SBB power about 12% of the Total

❑Possible Improvements



a) 6 RSU x 2 half-SBB x 19uW = 8.3mW reduction for a total area of 25.43 cm^2 (**0.28 mW/cm^2**). Possible improvement of **0.32 mW/cm^2 + 0.062 mW/cm^2** (half of the vertical clock). Equivalent of ~ 1.4 % of the total power of the chip.

b) Adding a 2-bit configuration to reduce the pre-emphasis cap of the **TX** in TYP conditions

c) Calibrating the offset of the comparator to further reduce the swing in the line. Requires a state machine and a 4-bit cap DAC.

Thanks!