Precision Timing in HEP Experiments

Davide Braga, on behalf of Fermilab’s Microelectronics Division

HEPIC, 2024-05-01

Fast Timing detectors and ASICs

Disclaimer: this talk focuses exclusively on Fermilab's ASICs (ETROC, 3D LGAD, FCFD, PSEC5, DILVERT, SUNROCK)

HEP, NP:

- 4/5D detectors, PID + tracking
- DOE BRN recommended with high priority to "develop high spatial resolution, highly granular pixel detectors with **precise per-pixel time resolution**" and identified the technical requirements: timing **on the order of 10 ps** and pixel pitch on the order of 10 µm for e+ e- colliders; and **better than 10 ps** timing resolution for hadron colliders, with similar pixel pitch. Also included the need to "accommodate preamp, Time-to-Digital Converters (TDC), and RAM in a small pixel pitch of the order of tens of microns, while maintaining power consumption not significantly greater than non-timing pixel ASICs (**~1 W/cm2**).

BES: e.g. studies of molecular dynamics time resolution in the 10-100 ps range

FES: e.g. GHz pulse train imaging at LCLS for inertial confinement fusion studies; National Ignition Facility burn width below 100ps

DRD7.3:

- Development of high performance, ultra-low power TDC
- Study and proposals for generic data-driven calibration strategies for the time measurements in detectors requiring high precision timing
- Timing Distribution Techniques

RDC11 (fast timing): Specific Detector Architectures (e.g. LAPPD, LGADs), Clock distribution and synchronization…

RDC4 (readout electronics): ASICs (TDC, PLL, DLL, High Speed Tx)

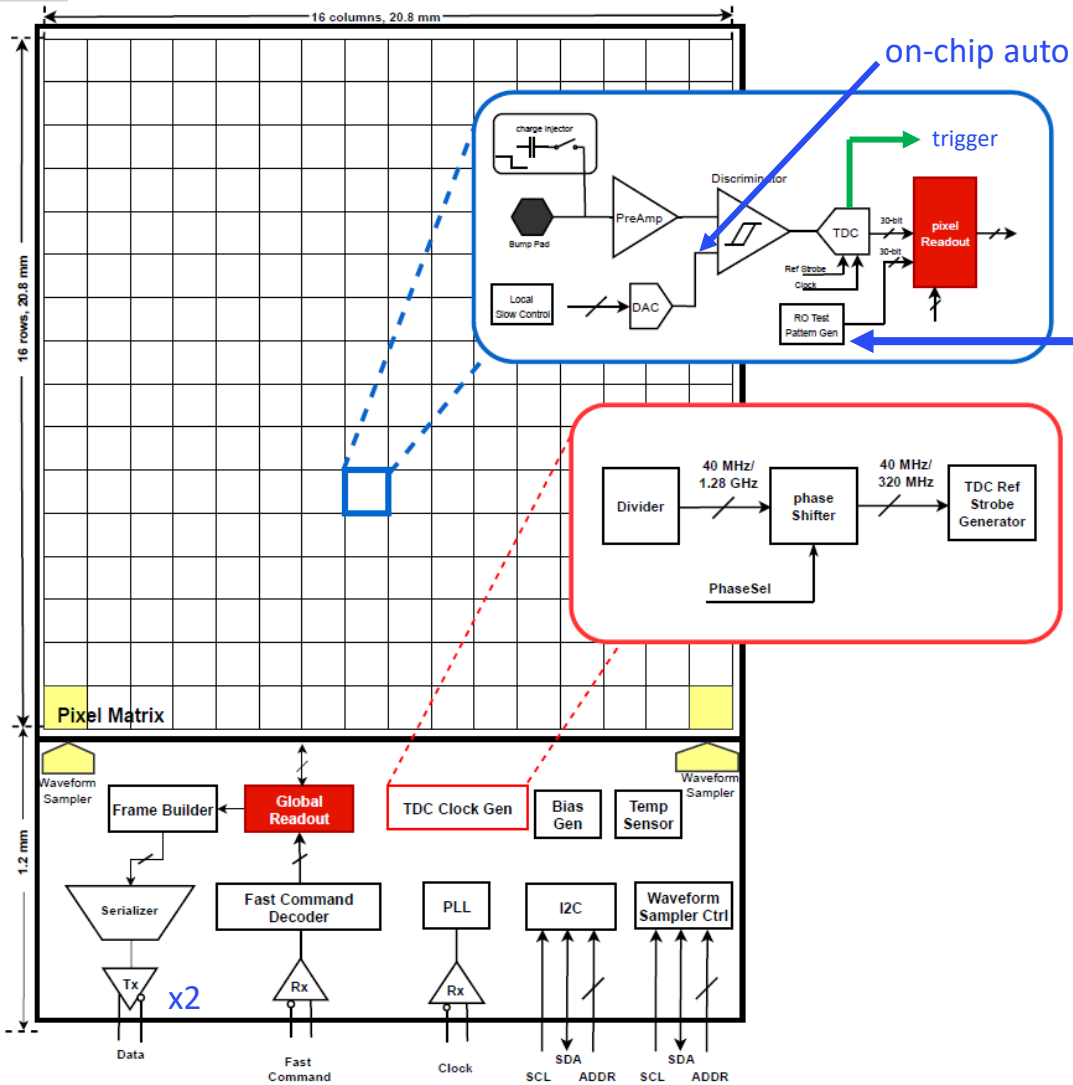
ASICs Overview

- ETROC, CMS ETL production (65nm)
- 3D LGAD, next-generation 4D detector (65nm CIS + 28nm ROIC)
- FCFD, novel front end concept, EIC (65nm)
- PSEC5, waveform sampler aiming for ultimate ps timing (65nm)
- DILVERT, cryogenic sub 5ps TDC for QIS (22nm, 4K)
- SUNROCK, SNSPD readout and time tagging ASIC (22nm, 4K)

ETROC Design

ETROC is designed to process
LGAD signals with time resolution
~50ps per hit, ~35 ps per track with 2 hits.

Ted Liu



on-chip auto threshold calibration

ASIC/FEE contribution should be kept < 40ps
Discriminator threshold: down to ~ 5fC

Self-test capability (for ***design verification*** & chip and system level testing with backend)

- Measuring arrival time of LGAD signal
  - Front-end: PA + Discriminator + TDC
  - L1 latency circular buffer
  - L1A-driven readout with zero suppression
  - A coarse map of ***delayed*** hits for L1 trigger
- Interface of ETROC2
  - 40 MHz reference clock
  - I2C-based slow control
  - 320 Mbps fast control
  - Serial data link 320/640/1280 Mbps
- Waveform Sampling of preamp output (only 1 pixel)
  - For test & monitoring purpose

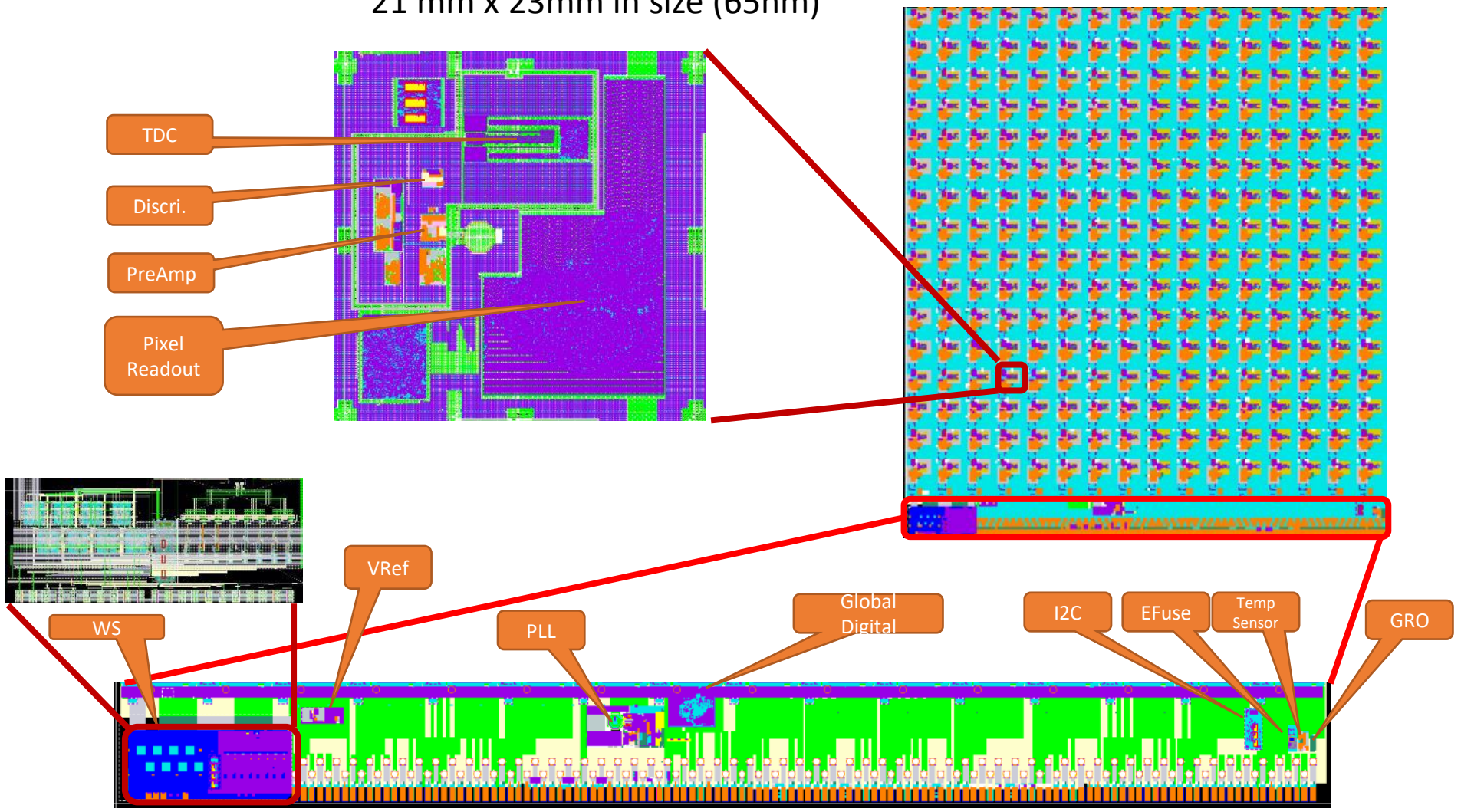
2.5 V for efuse (will require 2.5V once)

ETROC2 is designed in such a way as if it is the final design, with full functionalities

(with extra flexibilities for performance study purpose)

ETROC2 layout (submitted on Oct 21, 2022)

21 mm x 23mm in size (65nm)



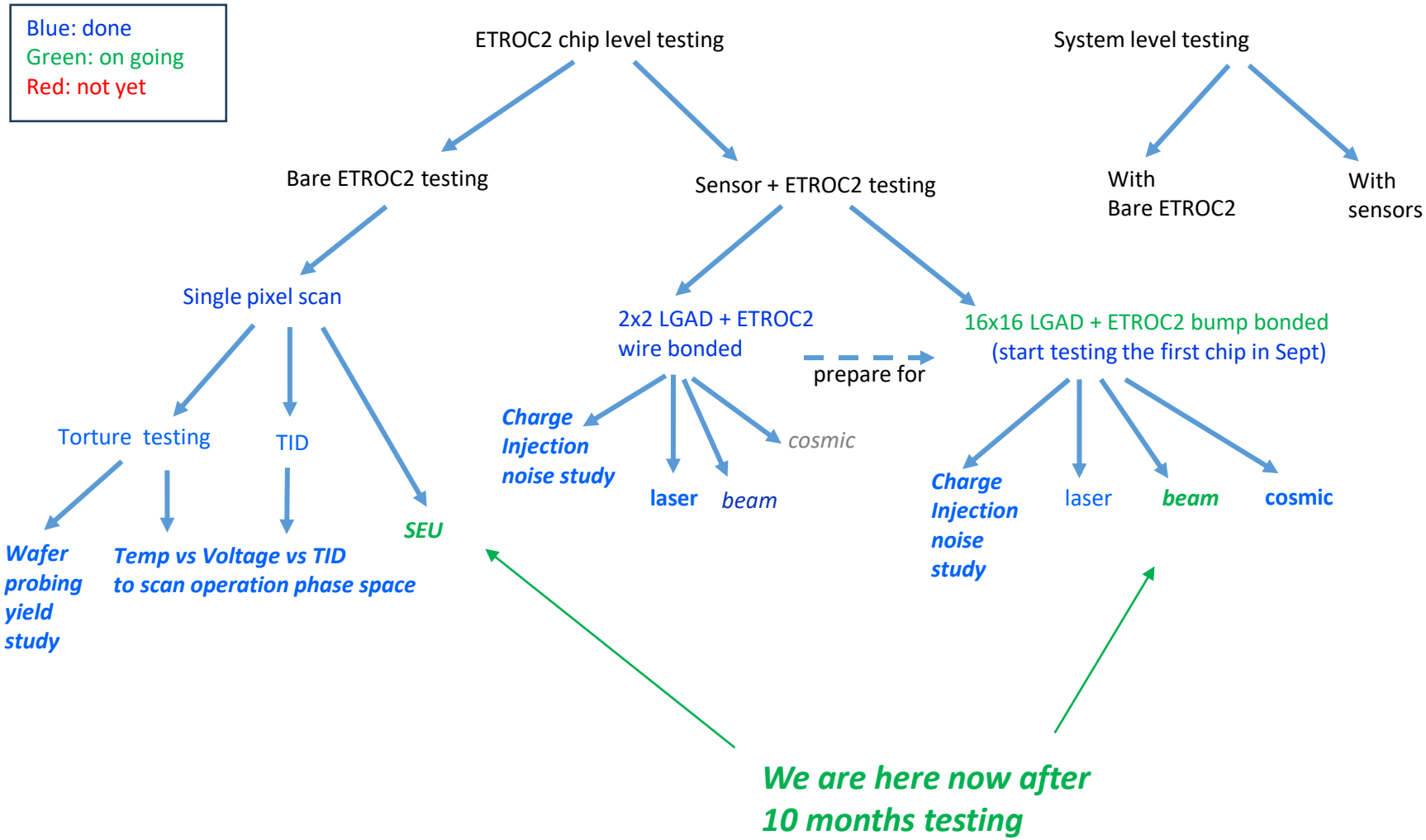
Summary: ETROC2

- ***The ETROC2 design is first full size, full functionality prototype for CMS ETL***
  - ***Fully functional with time resolution of ~10ps*** using charge/laser injection
  - ***Has passed 400 MRad TID test*** (spec is 100 MRad), works with voltage (1.3V to 1.0V) vs temperature (-30C to +30C)
  - ***The performance of the bump bonded ETROC2 is as expected (spec < 50ps/hit)***
  - ***Initial SEU testing results promising, more testing scheduled next two months***
  - *Successfully tested with the module and readout and power board prototypes together with the back-end electronics*
  - ***All known issues so far are minor and fixed with wafers on hold***

Design: FNAL/SMU/LBNL
Testing: FNAL/SMU/UIC/UCSB/Kansas/Lisbon/INFN Torino/KU Leuven with much help from CERN

ETROC2 chip level testing road map

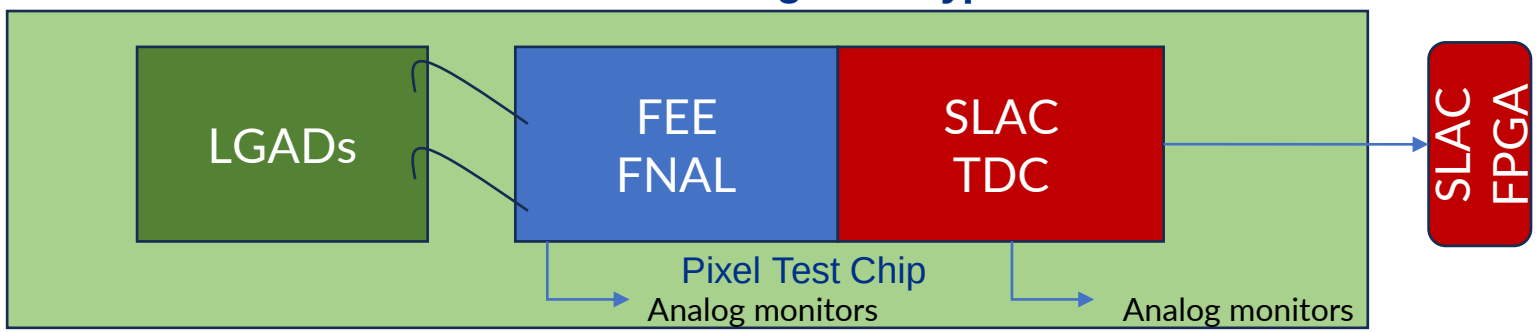
ETROC2 chips received in late April 2023



Accelerating Innovations in 3D Integrated LGADs

- Address the need for low-power, highly granular scientific detectors with excellent timing resolution
- Develop a new generation of silicon sensor detectors using low-gain avalanche diodes (LGADs) in a 12" process (also to match ROIC 12” wafers)
- Enabling the design and manufacturing infrastructure for future 3D integration
- 3D offers ideal optimization of sensor performance and low interconnect capacitance
- Joint SLAC-Fermilab: Fermilab’s pixel front end + SLAC TDC in 28 nm CMOS
- Pixel test chip tape out in July 2024 for wirebonding to LGADs
- Sensor tape out Fall 2024 with array for eventual 3D integration
- 5 mm x 5 mm ROIC tapeout Spring 2025

First Testing Prototype



CPAD Talk: 3D Integrated Sensing Solutions

SLAC NATIONAL ACCELERATOR LABORATORY
Fermilab
Lawrence Livermore National Laboratory

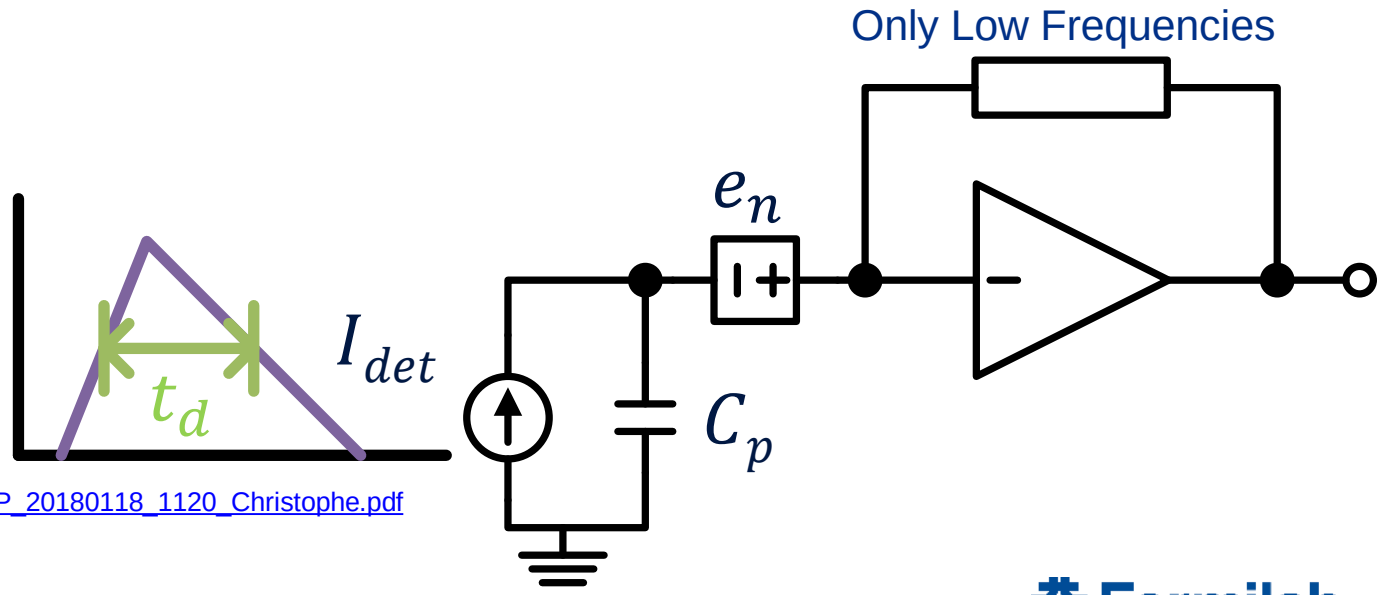
3D LGAD Front End Key Parameters

- LGADs increase charge magnitude, Q_{in}, and reduce signal duration, t_d, compared to traditional silicon detectors.
- 3D integration reduces parasitic capacitance, C_p.
- All directly improve time of arrival jitter, σ_t^J.

$$\sigma_t^J = \frac{e_n C_p}{Q_{in}} \sqrt{t_d} \quad ^{1,2}$$

- Using open loop voltage gain at frequencies of interest
- Active feedback for DC biasing and recovery[3]

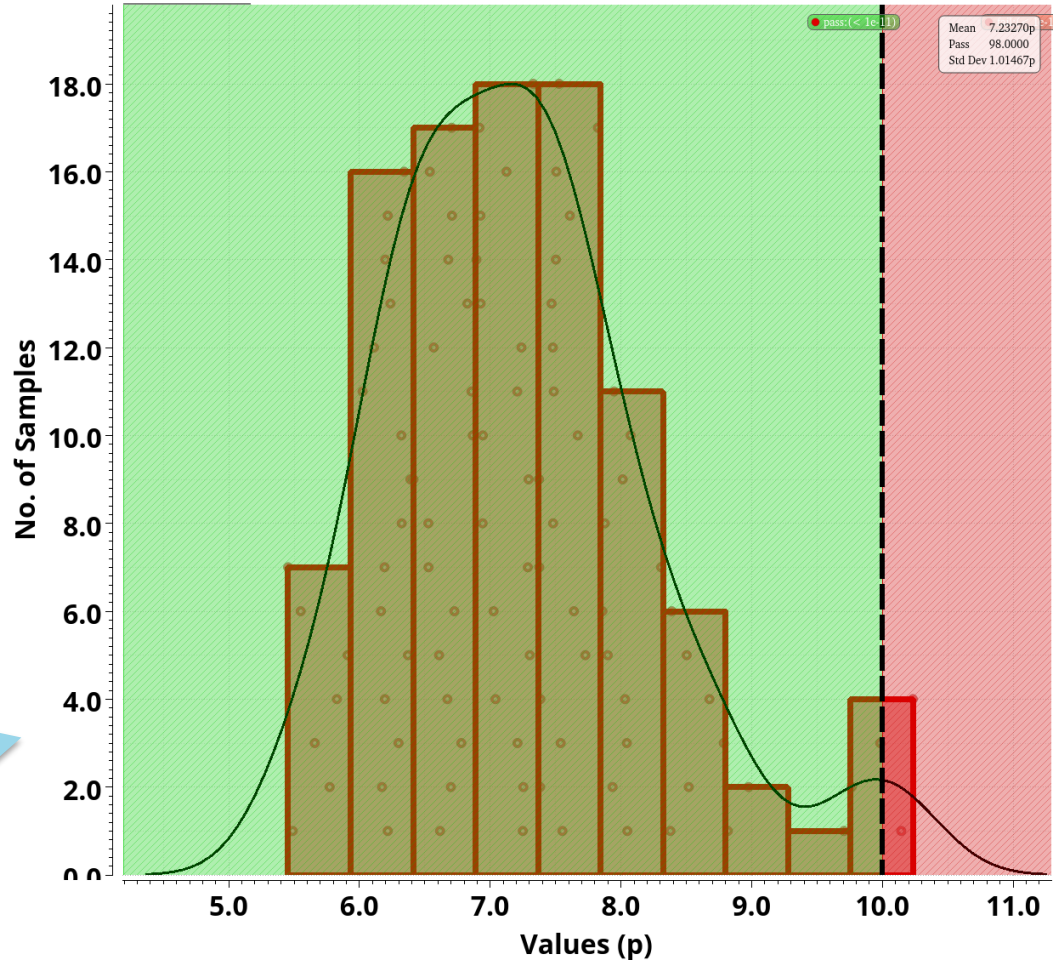
Specification	Value
Power Density	$1 \frac{W}{cm^2}$
Power 50x50 µm²	$25\ \mu W$
Time of Arrival (ToA) Jitter	$10\ ps_{rms}$
Min Q_{in} for ToA Jitter	$8\ ke^-$
LGAD Input Cap. 50x50 µm²	$28.8\ fF$
LGAD Signal Duration, t_d	$100\ ps$



1 Christophe de la Taille http://ias.ust.hk/program/shared_doc/2018/201801hep/program/exp/HEP_20180118_1120_Christophe.pdf
2 ALTIROC0 paper https://iopscience.iop.org/article/10.1088/1748-0221/15/07/P07007/pdf
3 Based on https://www.sciencedirect.com/science/article/abs/pii/016890029501454

3D LGAD Front End Approach

- Currently in schematic design
- Only small devices usable at power levels available
- Working to mitigate process variation through design and calibration
- Pre-layout estimates show about 7 ps_{rms} jitter from the front end
- 100 run Monte Carlo results with 100 transient noise simulations each
- 98 runs met jitter specification



Fermilab SLAC NATIONAL ACCELERATOR LABORATORY

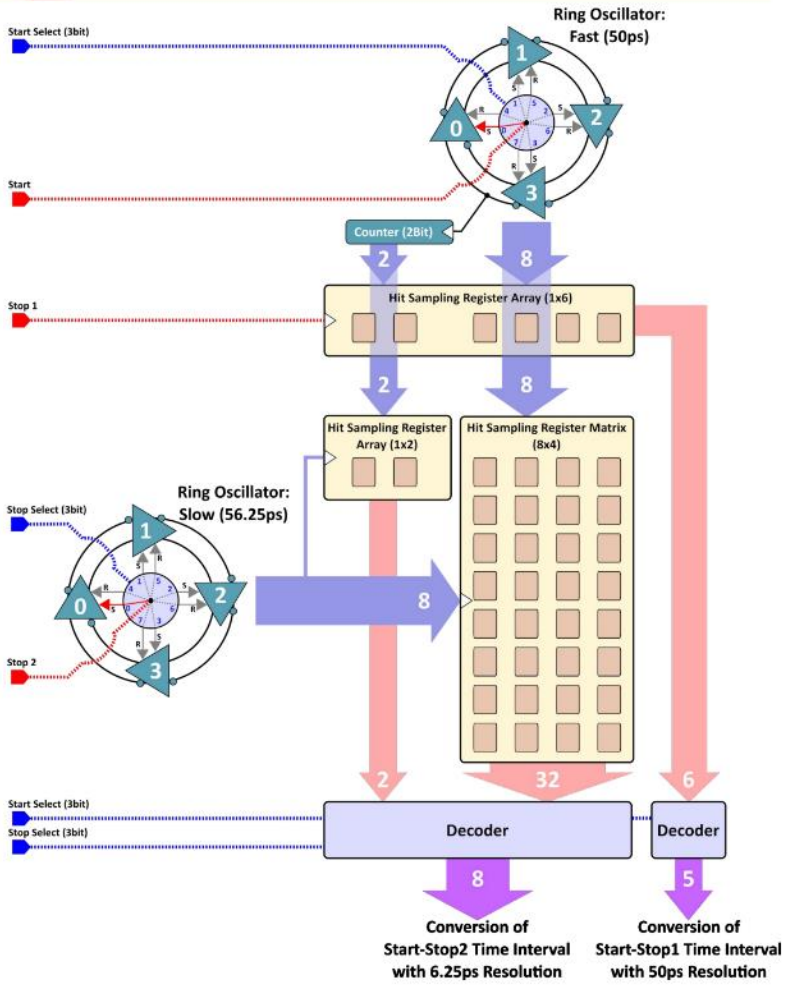
3D LGAD – TDC

- 28nm
- Small area (compatible with 50um pixels)
- Low power:
  - ~ 18.4µW for 10% occupancy
  - ~2.9µW for 1% occupancy

Bojan Markovic's CPAD talk:
Design and characterization of sub-10ps TDC ASIC in 28nm CMOS technology for future 4D trackers

28nm TDC Architecture

- **2D Vernier Architecture:**
  - Fast Ring Oscillator with 50ps propagation delay cells;
  - Slow Ring Oscillator with 56.25ps propagation delay cells;
- START + two STOP signal for simultaneous Time-Of-Arrival (TOA) and Time-Over-Threshold (TOT) measurements;
- Start-Stop1 - Coarse time resolution (TOT): 50ps;
- Start-Stop2 - Fine time resolution (TOA): 56.25ps - 50ps = 6.25ps;
- **Sliding scale technique for improvement of conversion linearity:**
  - Both ring oscillators have programable starting conditions via delay cell set/reset function;
  - Starting conditions randomly selected each measurement cycle and corresponding values subtracted from the conversion result;
  - Same time intervals converted with different parts/bins of the TDC conversion characteristics;
  - Sliding scale transforms the non-linearities into stochastic variable thus effectively improving the conversion linearity at the expense of worsening single-shoot precision.



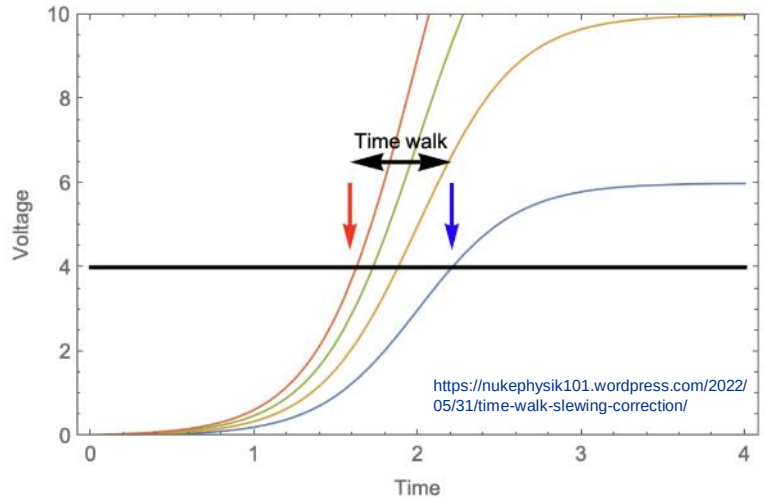
Fermilab Constant Fraction Discriminator Readout Chip (FCFD)

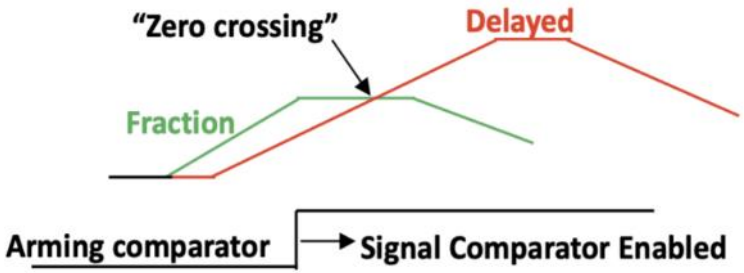
Si Xie, Artur Apresyan, Ryan Heller, Christopher Madrid, Irene Dutta, Aram Hayrapetyan, Sergey Los, Cristian Pena, Tom Zimmerman

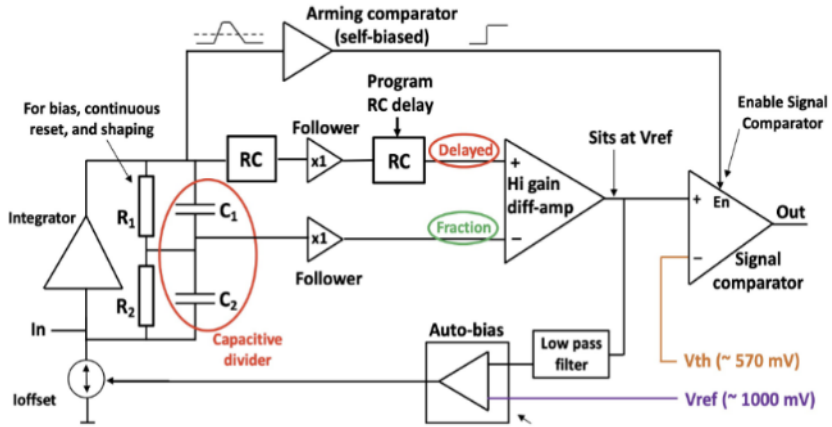
- Time-walk effect is well known & must be corrected for best performance
- Conventionally addressed with online or offline corrections via some type of LUT
- But under harsh radiation environments of future colliders, corrections may be time-dependent and intensive

- Primary application is (AC-)LGAD sensors for MIP signals
- But can be used for many types of precision timing detectors

- Main features of the CFD are:
  - Integrator & Follower to create the “fraction” signal
  - Comparators for “arming” and timestamping







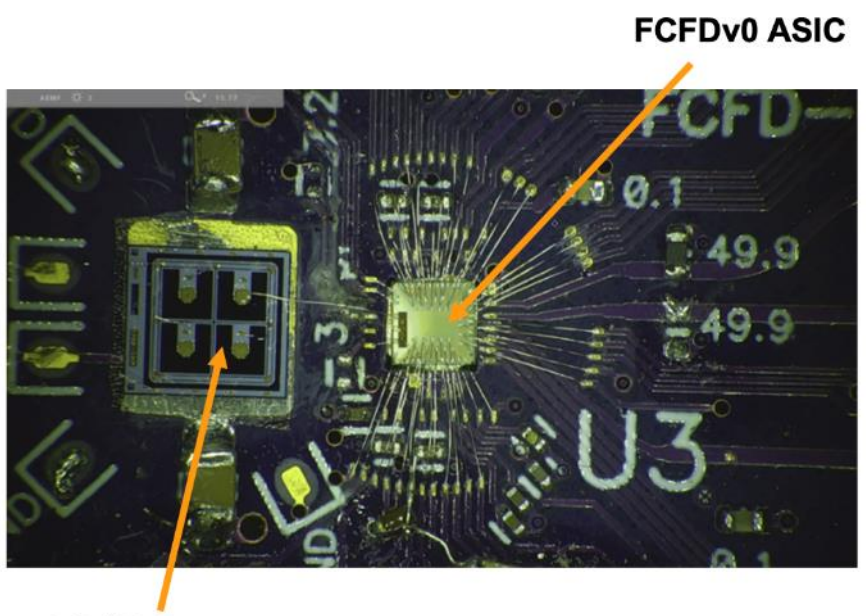
A. Apresyan et. al, **NIM A 1056, 2023, p168655**
https://doi.org/10.1016/j.nima.2023.168655

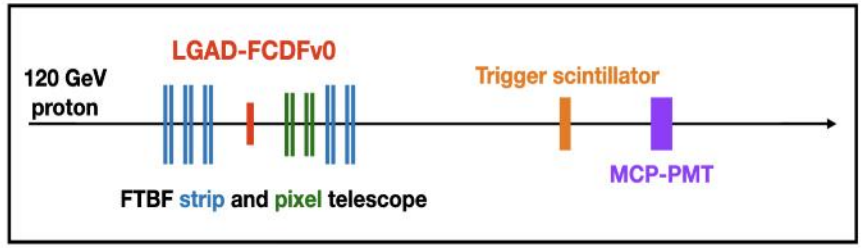
FCFD v0

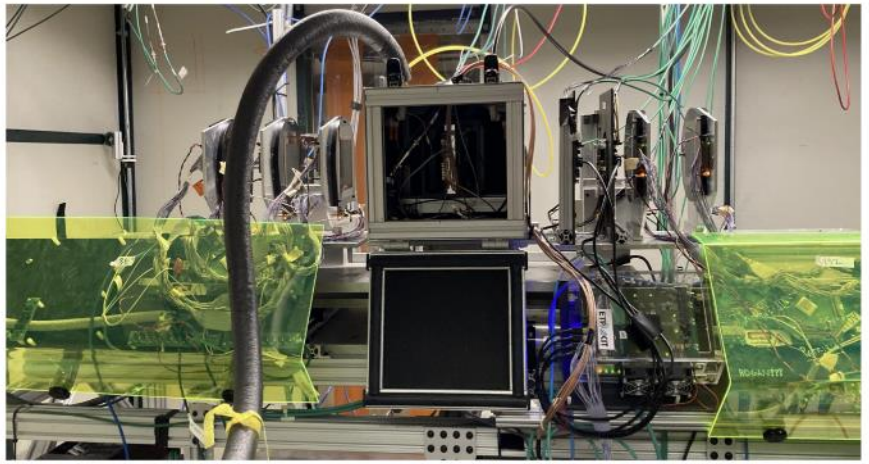
FCDF first prototype (2021):

- performance evaluated using multiple types of signals:
  - Charge-injected signal
  - Picosecond Laser signal
  - Radioactive Source signal
  - Proton Beam signal

  Measured performance consistent with design expectation and between many types of signal source







FCFD v0 testing and performance

Charge Injection

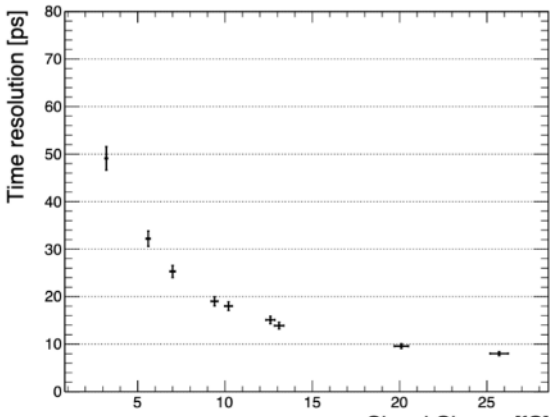
- Time resolution performance as expected
- For largest signal (before saturation) get ~8ps time resolution
- Time walk effect is reduced from 100's of ps to a ~10ps window

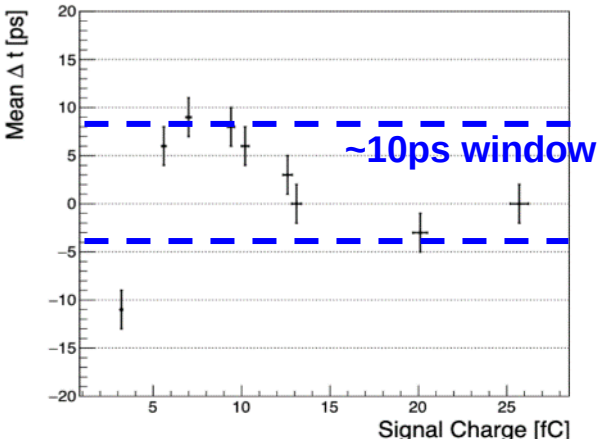
Picosecond Laser & Beta Source Setup

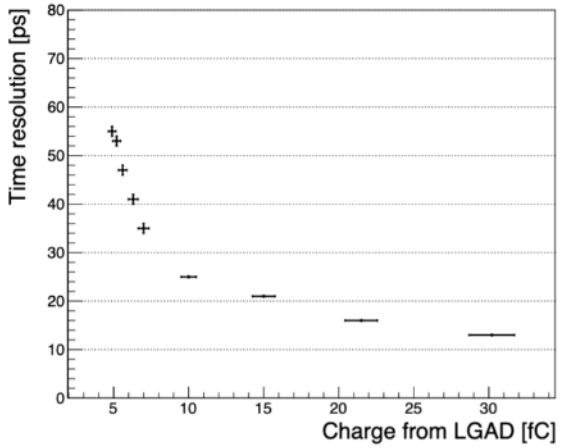
- Dark box with motorized stages, enabling laser injection and beta source
- Laser measurements confirm similar performance as charge injection

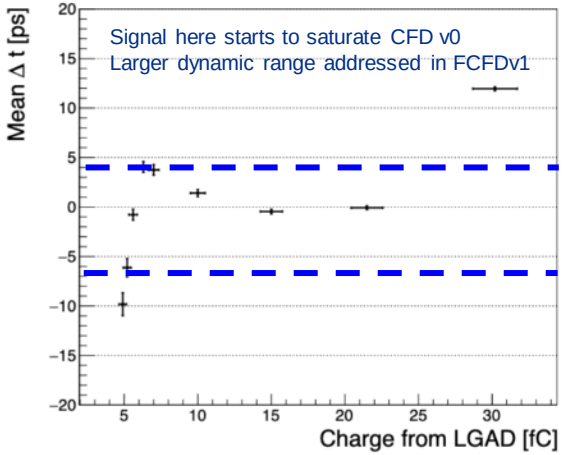
Proton Beam Measurements

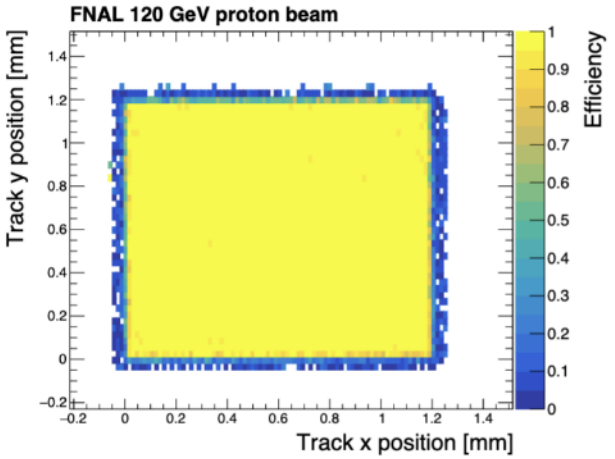
- Fermilab Test beam Facility (120 GeV p+)
- Tracking telescope used to measure hit positions and efficiency
- 100% Efficiency is maintained over full LGAD pixel sensor area
- Time resolution performance consistent with Beta Source measurement

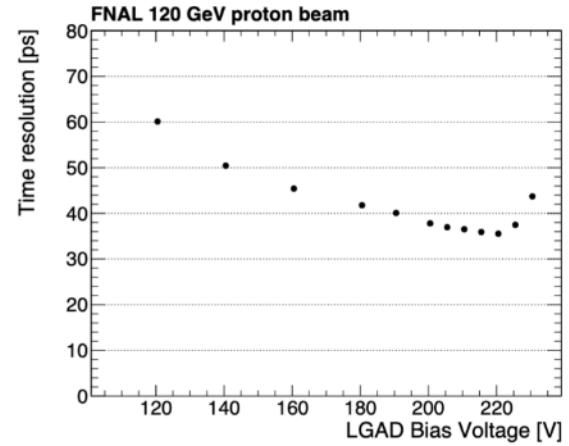








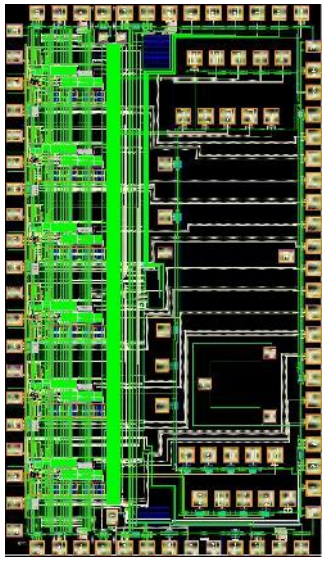




FCFD v1 and future developments

FCFD v1 (2023)

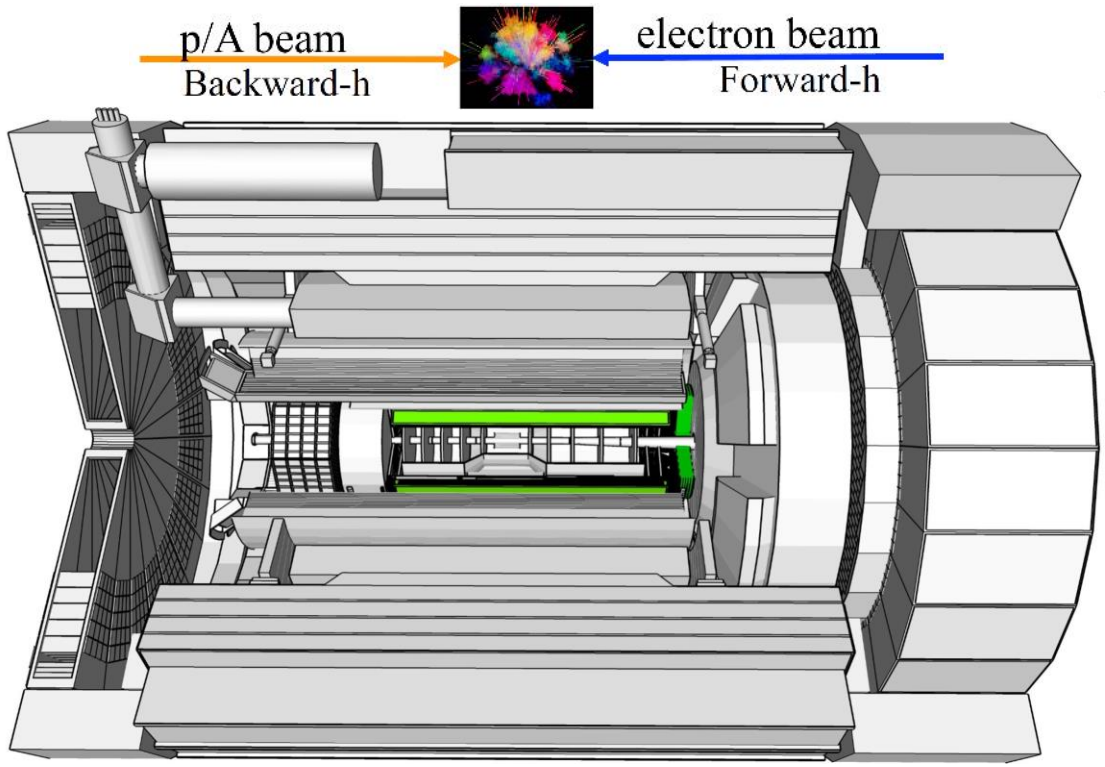
- Multi-channel (6)
- Larger dynamic range to cover full range of MIP LGAD signals
- Signal amplitude measurement
- Currently being tested with AC-LGADs



FCFDv1

Barrel Time-of-Flight for ePIC (EIC)

Discussing large FCFD multichannel ASIC with TDCs and digital readout for AC-LGAD detector

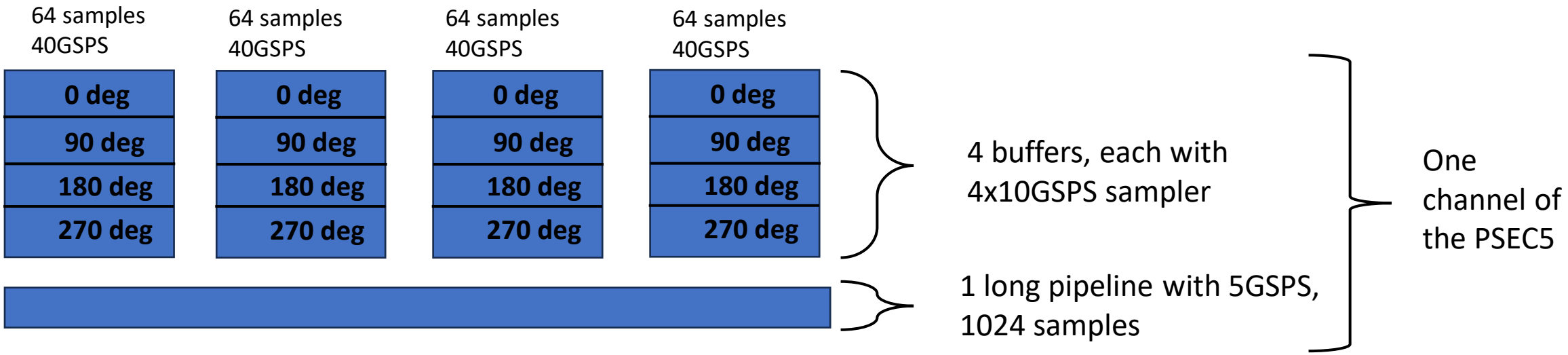


PSEC5

The key idea of the PSEC5 is to achieve optimal timing resolution (aiming for 1ps sigma) while maintaining a reasonable number of samples and a reasonable length of waveform by using a **hybrid waveform sampler.**

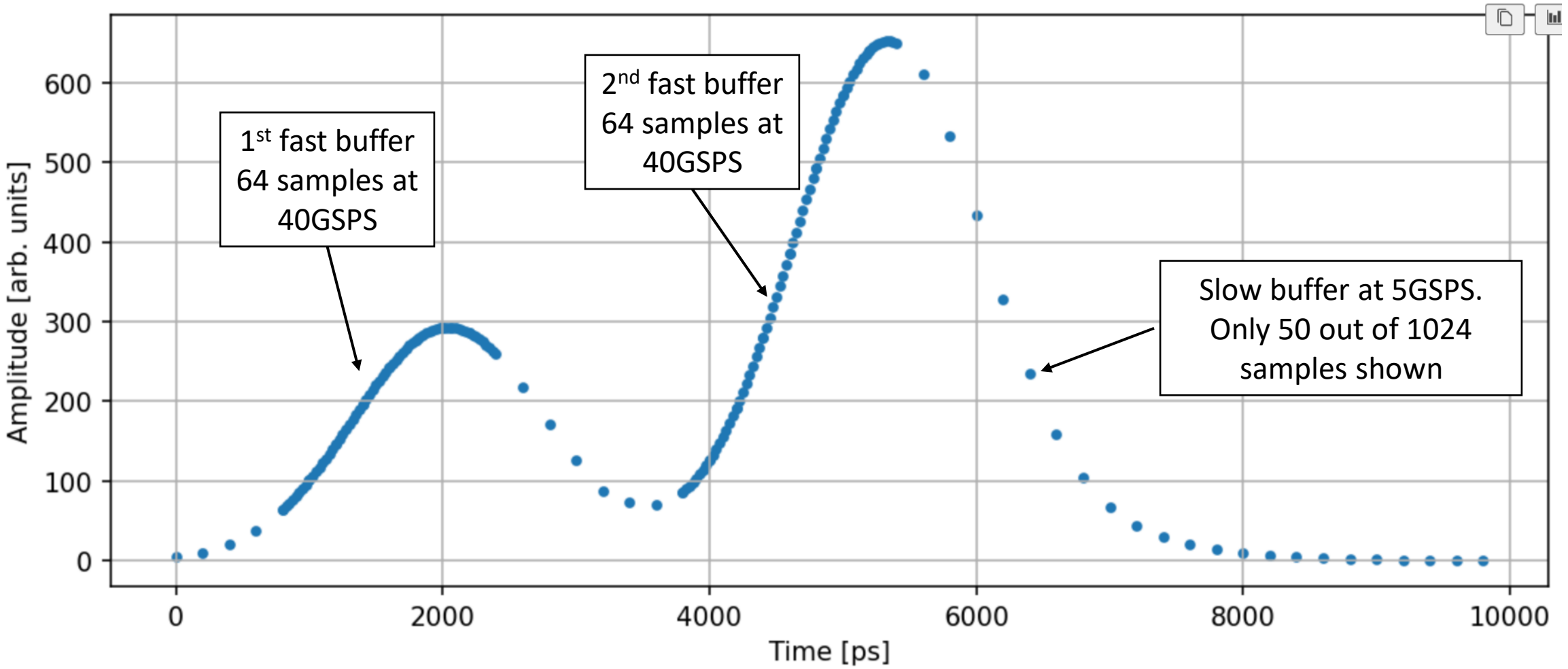
Each channel of the PSEC5 consists of 5 separate samplers: 4x short, “fast” 16 sample pipelines running at 10GSPS but with a 90deg phase shift relative to each other, resulting in effective sampling of **40GSPS** (64 samples). The “fast” samplers are multi-hit capable, with 4 buffers. The fast samplers are triggered on the rising edge of the pulse by a fast discriminator.

Each channel has one “slow” 5GSPS pipeline running with 1024 samples resulting in a waveform of ~200nS.



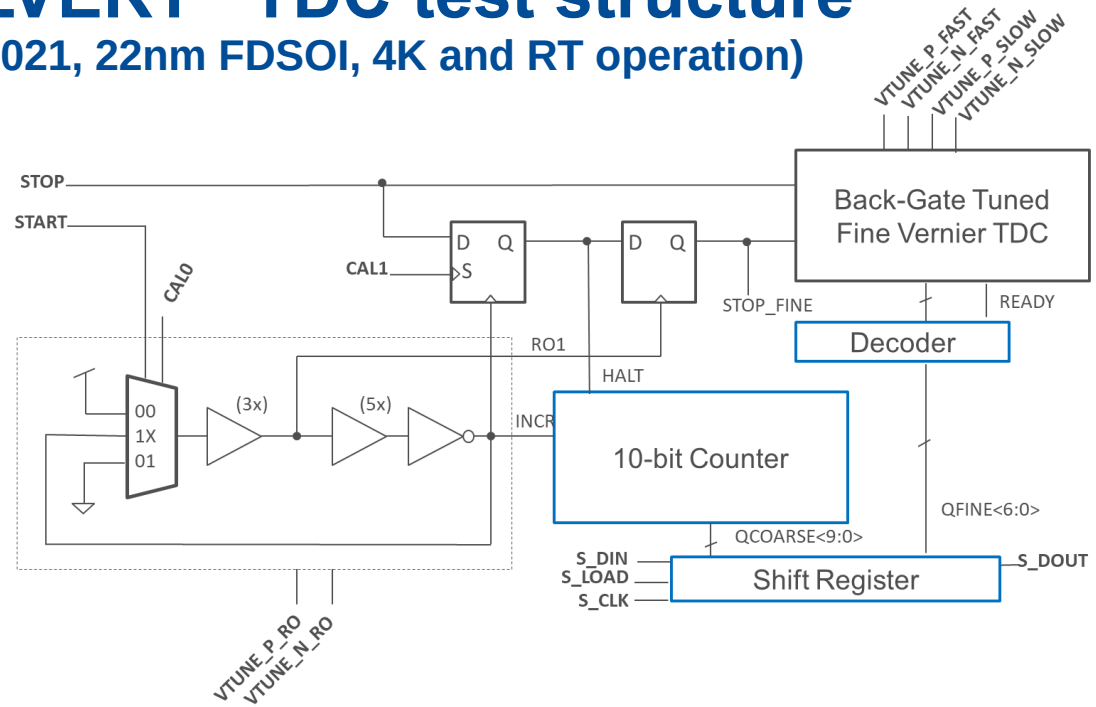
This is the “hybrid sampler”, sampling at 5 GSPS for long memory, 40GSPS for optimal timing of the pulse edges. PSEC5 is designed in TSMC 65nm.

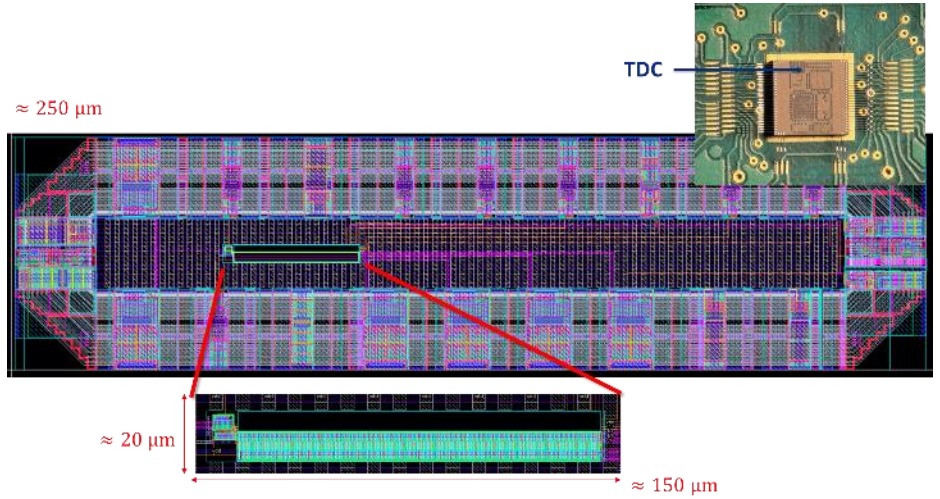
- Example of idealized waveform (no noise) demonstrating the functioning of the hybrid sampler, 5GSPS and 40GSPS.
  Note: **only 5% of the full memory** (10ns out of 200ns) is shown!

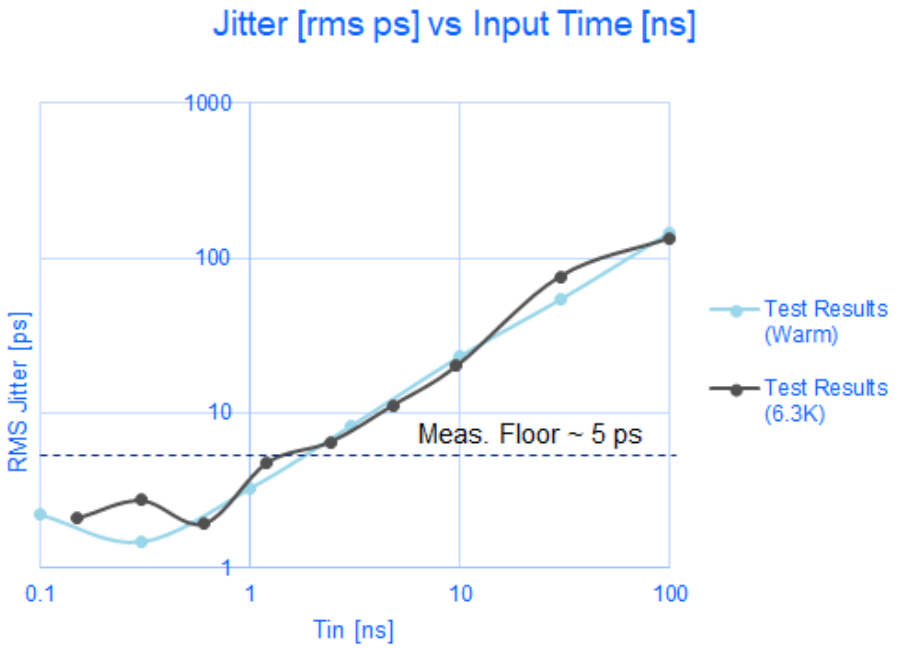


“DILVERT” TDC test structure

(Nov 2021, 22nm FDSOI, 4K and RT operation)







Speed is tuned by FDSOI back-gate biasing

- Low complexity, small footprint, no noise contribution from bias circuits

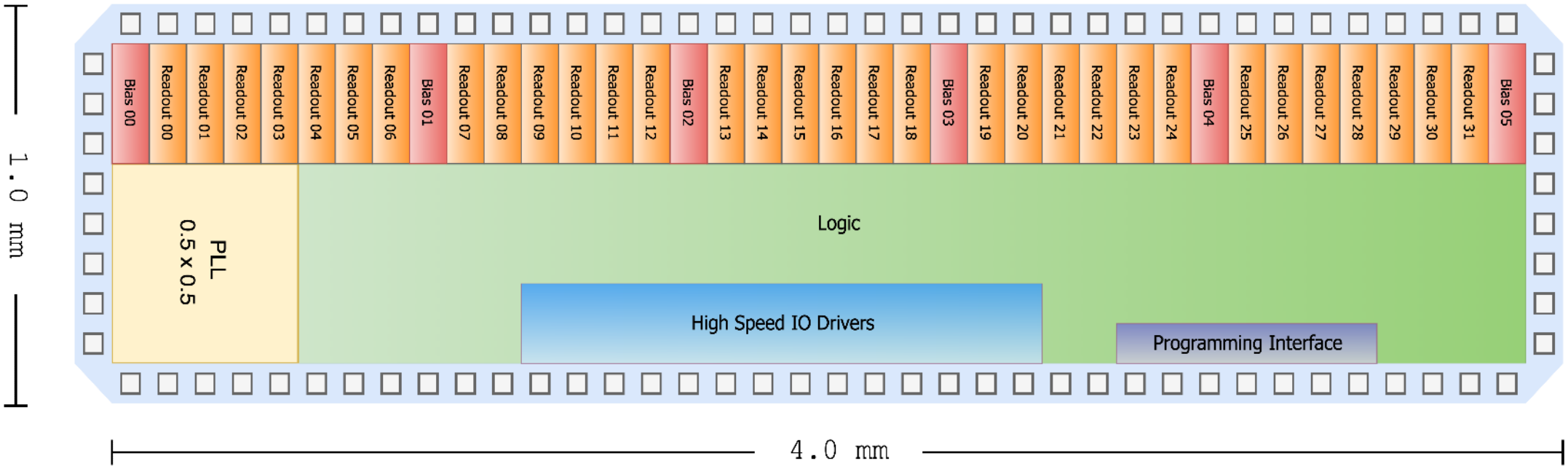
6 separate tuning voltages:

- Fine TDC fast chain, slow chain, and coarse TDC ring oscillator
- Tune NMOS and PMOS separately.
- Both 0~2V w.r.t VSS

~300 µW at 100MHz (power scales roughly linearly with rate)

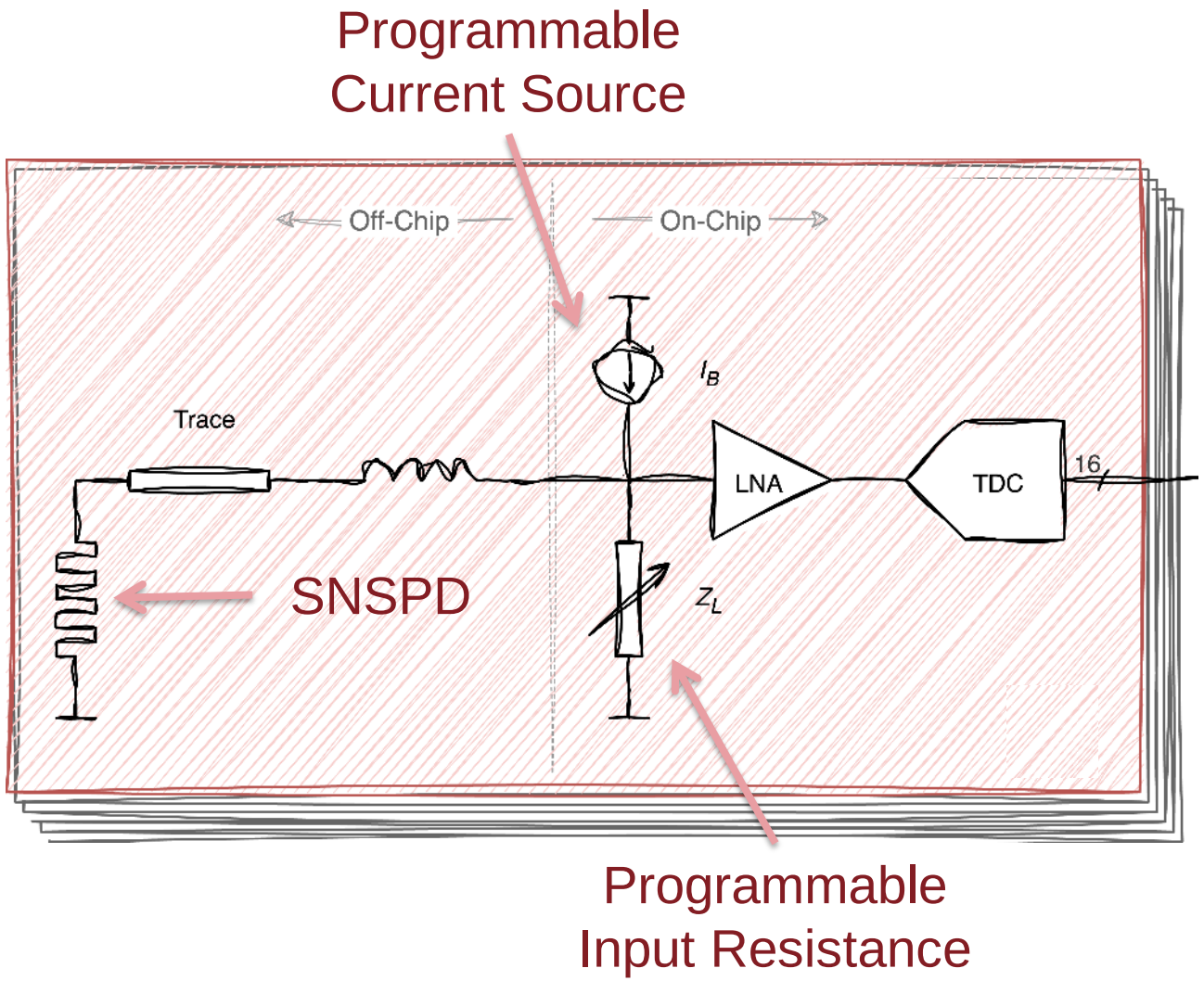
- Currently being tested with LGAD + FCFDv0 discriminator. The input of the FCFDv0 is an LGAD sensors exposed to beta source and laser. Measurements demonstrated the TDC performance achieve around 6ps resolution. Detailed results will be soon presented in a publication.

SUNROCK (SNSPD Readout Chip)



- 32x - Readout Channel
- 5x - Auxiliary Bias Channels
- 4x – 1Gbps SerDes
- <10ps RMS Timing Accuracy
- Digital Arbitration Logic
- Operation at 4°K

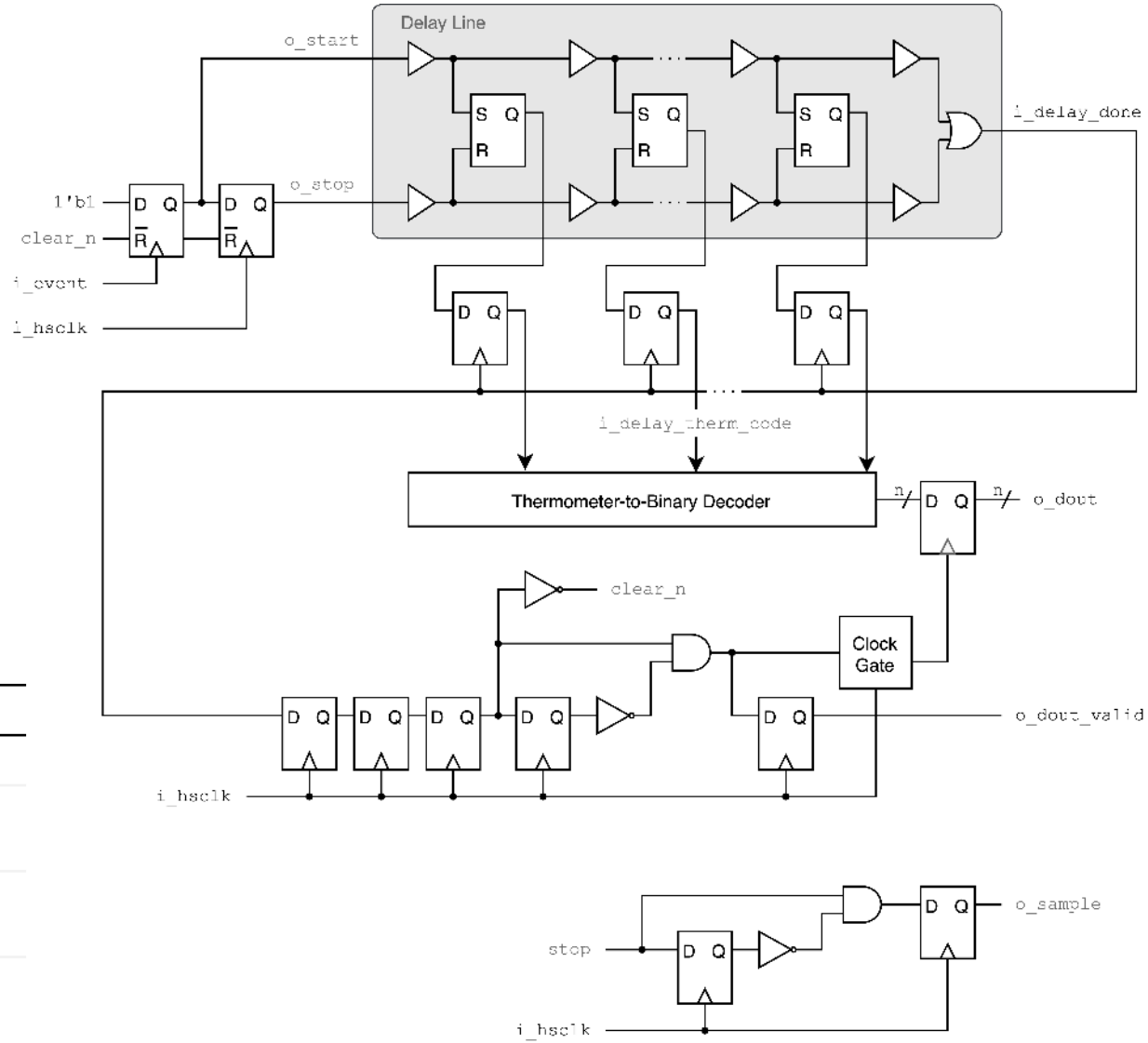
Sensor/Readout Interface Requirements



- Programmable current source to bias SNSPD/nTron
- Programmable input resistance to passively quench SNSPD/nTron after a detection event
- Low-noise amplifier (LNA) to amplify and buffer detection signal.
- TDC to measure the arrival time of the input detection

TDC

- Delay line uses both PMOS and NMOS backgate bias voltages to control delay. (A common bias is shared across all channels)
- Delay line is hand placed custom digital
- Low jitter central PLL provides a stable time reference for each of the channel TDCs.
- Clock distribution network is carefully constrained to minimize delay and jitter.



Name		Target		Description
Channel Timing Error	rms	8.0	ps	Total RMS timing error.
Amplification Jitter	rms	5.00	ps	Timing error from the amplification.
TDC accuracy	lsb	5.00	ps	Timing error from the TDC measurement.
High-Speed clock Jitter	rms	5.00	ps	Timing error from the TDC measurement.
PLL Jitter	rms	75	fs	Random jitter from PLL

Readout Chiplet Performance Specifications

Name		Target		Value		Comment
Readout Channels	-	32		32		Dedicated readout channels.
Bias Channels	-	6		6		Dedicated bias channels.
High Speed Outputs	-	4		4		The high-speed output consists of 4 low-swing differential serial outputs.
Output Driver Speed	typ	1.0	GHz	1.0		
	max	1.0	GHz	1.0		
Programming Interface Speed	max	100	MHz	100	MHz	The programming interface is limited by the speed of the GPIO pads.
Analog Core Supply Voltage	nom	0.80	V	0.80	V	Supply voltage for readout channels, bias channels, and TDC delay line.
Digital Core Supply Voltage	nom	0.80	V	0.80	V	Supply voltage for the digital arbiter and programming interface
PLL Core Supply Voltage	nom	0.80	V	0.80	V	Supply voltage for the PLL.
GPIO Supply Voltages	nom	1.80	V	1.80	V	General purpose IO used for programming interface and
HSIO Supply Voltage	nom	0.80	V	0.80	V	
Timing Accuracy	rms	8.0	ps	-	ps	Timing measurement accuracy.
Total Power	avg	~90.0	mW	~75.5	mW	
Readout Channel Power	avg	500.0	uW	400.0	uW	Readout channel power with 1% activity.
Bias Channel Power	avg	150.0	uW	125.0	uW	Bias channel power.
Digital Power	avg	20.0	mW	16.0	mW	Digital arbiter power.
SerDes Lane Power	avg	8.0	mW	6.5	mW	SerDes power.
PLL Power	avg	20.0	mW	-	mW	10.0 GHz PLL power.

Next iteration will attempt to reduce the power consumption 10x while maintain 8.0ps timing accuracy

Timing Accuracy	rms	8.0	ps	-	ps
Total Power	avg	~90.0	mW	~75.5	mW

Summary

- Fast timing becoming increasingly important across HEP and non-HEP applications
- Fermilab is working on several fast-timing chips in different technologies and with different requirements
- Sensor codesign / interconnect / distribution (local and system) key to preserving timing information
- Performance characterization requires extensive testing
- Coordination with US and international initiatives (cross-cutting)