

# Integrated Silicon Photonics

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*AMPIC Lab*

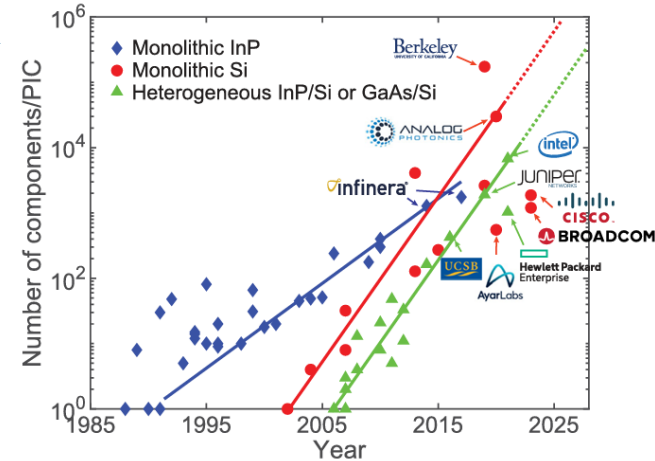


# Outline

- Introduction to Silicon Photonics
- Optical Interconnects
  - Potential for HEP applications
- Integrated RF Photonics
- Conclusion

# PICs for Beyond-Moore Era

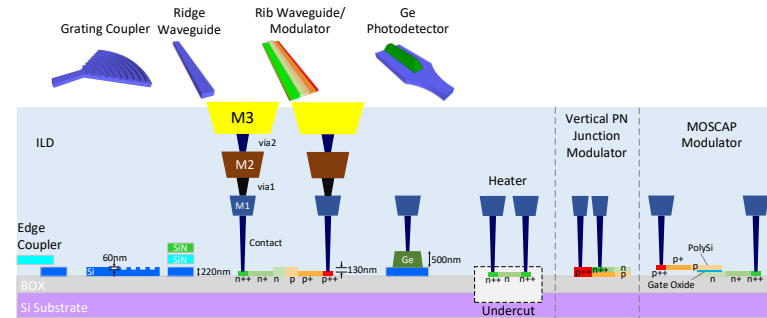
- Post-Moore or Beyond-Moore ICs require integration of novel devices with CMOS: CMOS+X
- Silicon-based Photonic Integrated Circuits (PICs) designed using the same CAD tools and manufactured using standard 300mm CMOS facilities
- ‘Moore’s law’ for PICs
  - Number of components on a PIC double every ~18 months
  - Large-scale PICs for optical transceivers, optical signal processing, and computing
    - $>10^3$  on-chip components



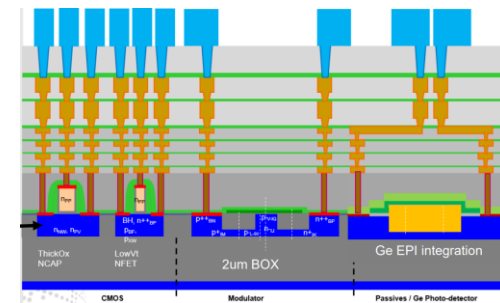
Margalit, N. et al., “Perspective on the future of silicon photonics and electronics,” *Appl. Phys. Lett.* 118, 220501 (2021).

# Silicon-Based Photonics Integration

- Silicon-on-Insulator (SOI) photonics foundry platforms enable large-scale PIC fabrication
- Passive silicon photonic components
  - Low-loss waveguides, bends, couplers
  - Grating and Edge couplers
  - Thermo-optic phase shifters
- Active silicon photonic components
  - High-speed  $pn$  junctions, modulators ( $\sim 35\text{GHz}$  BW)
  - Ge detectors ( $\sim 40\text{GHz}$  BW)
  - SiGe Electro-absorption modulators ( $\sim 50\text{GHz}$  BW)
- Heterogeneous integration of III-V lasers and on-chip optical gain



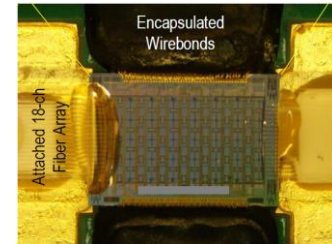
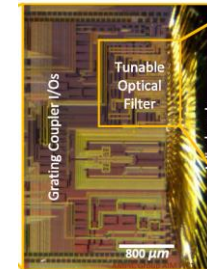
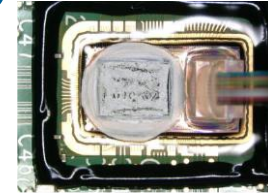
Adapted from Fahrenkopf *et al.*, "The AIM Photonics MPW: A Highly Accessible Cutting Edge Technology for Rapid Prototyping of Photonic Integrated Circuits," *IEEE JTQE*, vol 25, no 5, 2019.



Giewont *et al.*, "300-mm Monolithic Silicon Photonics Foundry Technology," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 25, no. 5, pp. 1-11, 2019.

# PIC Application Space

- **Transceivers:** Data center interconnects, coherent long-haul, 5G networks, WDM transceivers
- **RF Photonics:** Optical filters, flexible RF front-ends, RF beamforming
- Programmable Photonics
- LIDAR, Optical phased arrays, free-space optics
- **Sensors:** Chem, Bio-sensing, Optical Gyroscope
- Deep Neural Networks, AI
- Optical Quantum Computing



LiDAR

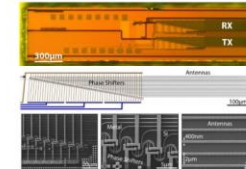
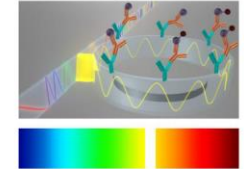


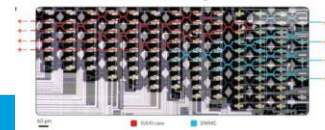
Image: Christopher V. Poulton <https://spectrum.ieee.org/tech-talk/semiconductors/optoelectronics/mit-lidar-on-a-chip>

Biosensing



Genalyte Maverick Detection System <https://www.genalyte.com/>

Artificial Intelligence



Y. Shen et al. Deep learning with coherent nanophotonic circuits, Nature Photonics, <https://doi.org/10.1038/nphoton.2017.03>

Quantum Computing

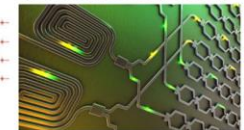


Image: Xiaogang Qiang <https://spectrum.ieee.org/tech-talk/semiconductors/optoelectronics/building-quantum-computers-with-photonics>

# SOI Phase Shifters

- Thermo-optic phase shifters
  - Strong temperature dependence, compact, lossless
- Carrier plasma-dispersion effect
  - Local refractive index depends on the free carrier concentration (1550nm)<sup>1</sup>

$$\Delta n(x, y) = -8.8 \times 10^{-22} \Delta N_e(x, y) - 8.5 \times 10^{-18} \Delta N_h(x, y)^{0.8}$$

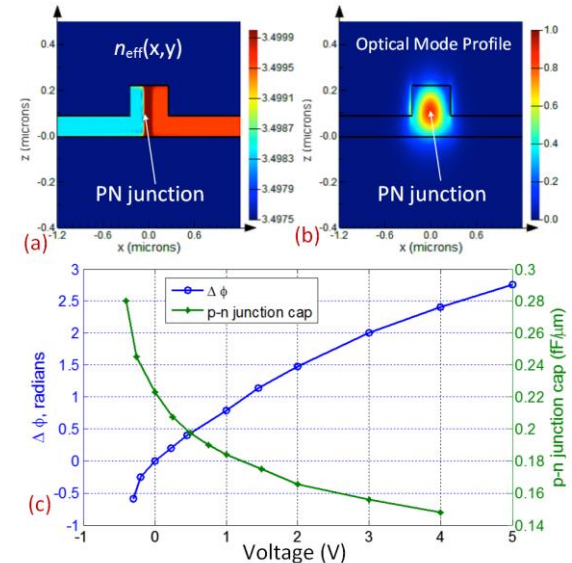
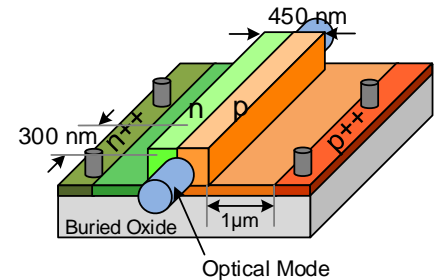
$$\Delta \alpha(x, y) = 8.5 \times 10^{-18} \Delta N_e(x, y) + 6 \times 10^{-18} \Delta N_h(x, y)$$

- voltage controlled phase modulation

$$\Delta \phi(V, \lambda) = \frac{2\pi L}{\lambda} \left( \Delta n_{eff}(V) + \frac{dn}{dT} \cdot (T - T_0) \right)$$

- Can use both reversed-biased (depletion mode) or forward-bias (injection mode) devices
  - MOSCAP-based devices also exist (e.g. SISCAP)

<sup>1</sup>R.A. Soref and B.R. Bennett, "Electrooptical effects in silicon", JQE-23, pp.123-129, 1987

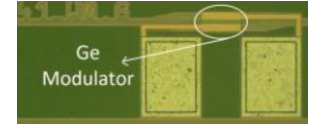
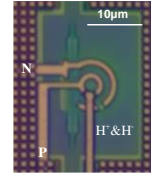


# Optical Modulation Materials and Mechanisms

Modulation Material	Modulation Mechanism	Integration in commercial CMOS foundry	PPA Highlights	Crucial PPA Limitations	
p-n dopants	Free-carrier plasma dispersion	Easy	Reliable	IL	Standard SiP
Metal or doped Si	Thermo-optic	Easy	Loss-less	Power consumption, Thermal crosstalk, E/O BW	
GeSi	Franz-Keldysh (FK) Quantum-confined Stark Effect (QCSE)	Medium (Epitaxy)	Size	O-band support (FK) IL (QCSE)	
InGaAsP/InP/Si or InGaAs/GaAs/Si	Carrier-plasma, band-filling, QCSE, FK	Medium (BEOL)	Reasonable in all	Different bandgaps for laser & phase shifter, FoM <sub>efficiency</sub> needs improvement	Heterogenous Integration
BTO	Pockels effect	Medium (BEOL)	Good in all	Newer technology	
Polymer	Pockels effect	Difficult (poling, FBEOL)	Good in all	High-temp. operation, hermetic sealing	
LNOI	Pockels effect	Medium (Different expansion coef., BEOL)	BW	Size	
PCM	Phase Change/Transition	Medium (BEOL)	Low-power (static)	E/O BW, IL, Dynamic power	
Nematic LC	Birefringence	Medium (BEOL)	Low-power	E/O BW, IL, High-temp. operation, Packaging	Liquid crystal/MEMS
MEMS/NOEMS	Optomechanical deformation	Medium	Low-power	E/O BW, Packaging	

S. Shekhar et al., "Roadmapping the next generation of silicon photonics," *Nature Communications* 15.1 (2024): 751.

# Silicon-Based Modulator Devices



	<b>Mach-Zehnder Modulator</b>	<b>Microring Modulator</b>	<b>Electro-Absorption (EAM)</b>
Mechanism	Interferometric Plasma dispersion	Resonant (ring or disk) Plasma dispersion	Franz Keldysh effect (Ge/SiGe) Absorption
Device Size	>3mm pn-junction length	Very compact (<10µm radius)	Compact (~40µm length)
Driver Type	Current-mode or distributed driver	Lumped voltage-mode drive	Lumped voltage-mode drive
Drive Voltage	2.4V <sub>pp</sub>	1.2-4V <sub>pp</sub>	2-3V <sub>pp</sub>
EO Bandwidth	>35 GHz	>40 GHz	>50 GHz
TX Energy-efficiency (NRZ)	2.4 <sup>†</sup> , 2-11 pJ/bit	0.685 <sup>†</sup> , 2-4.5* pJ/bit	0.78* pJ/bit
TX Energy-efficiency (PAM4)	2.4-13.64* pJ/bit	0.685 <sup>†</sup> , 5.8* pJ/bit	1.5* pJ/bit
TX Design Challenge	Quadrature bias control	Continuous Resonant wavelength control	No tuning required but generates large photocurrent

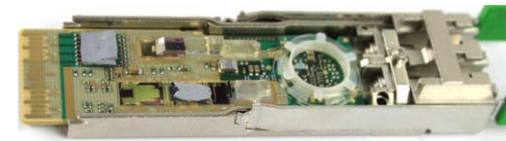
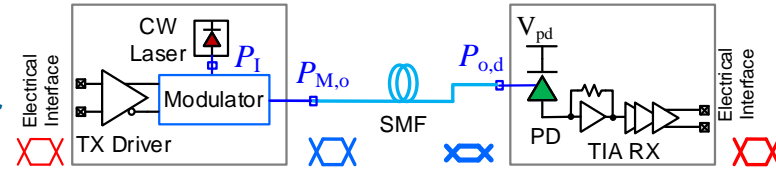
†Monolithic Integration, \*Hybrid Integration



# SiP-based Optical Interconnects

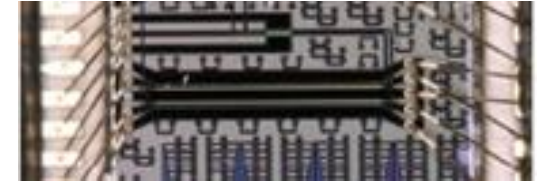
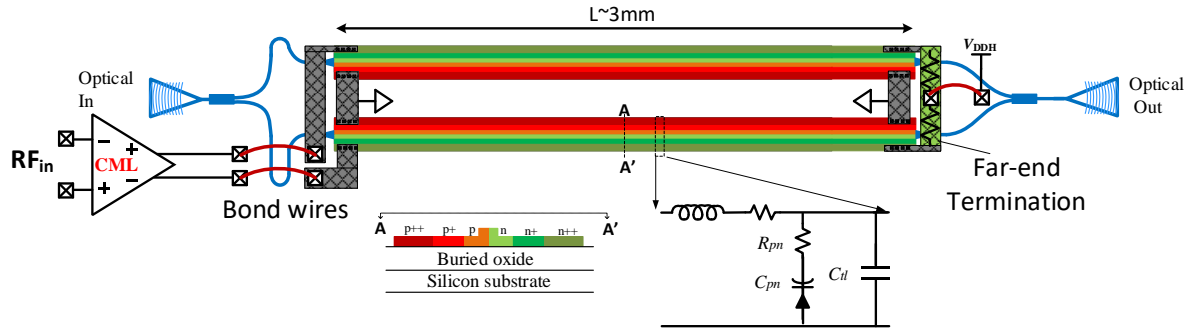
# SiP Optical Interconnects

- AI and Cloud computing drive the demand in data center usage
- SiP is ideal for high-bandwidth, low-cost, and long-distance interconnects
- Low-loss fiber channel enables *distance-independent communication*
- Data center interconnects evolved from demos in year 2007 multi-million units per year
- EIC integrated with PICs
  - Evolution from separate ICs to monolithic or 3D integrated PIC/EICs



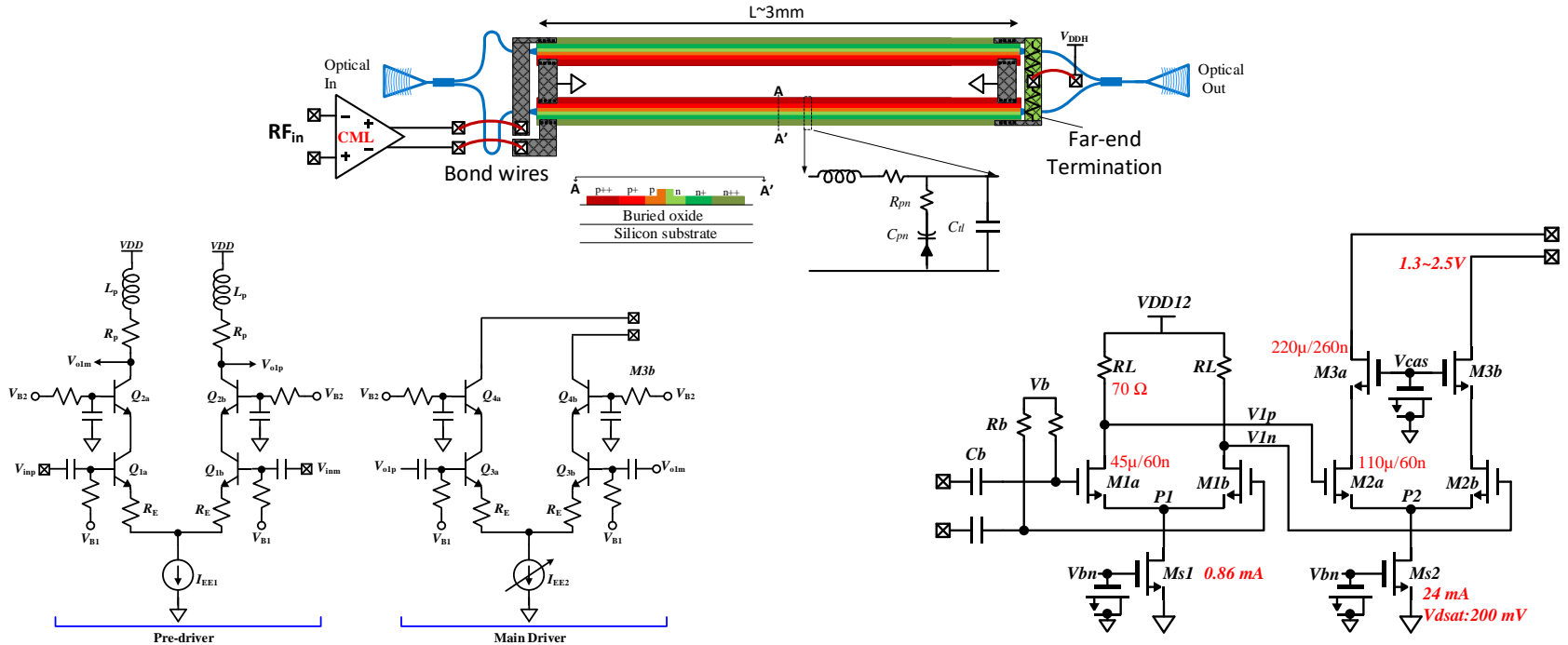
Intel's 100G CWDM-4 QFSP28 transceiver module

# Current-mode TW-MZM Driver



- Silicon MZMs exhibit  $V_{\pi}L_{\pi} \sim 1.2-2 \text{ V}\cdot\text{cm}$ 
  - long ( $>3\text{mm}$ )  $pn$  junctions for  $V_{\pi}$  in the CMOS range
  - Push-pull drive used to half drive voltage
  - Typically, 2.4-3V drive voltage
- Electrical and optical velocities should match; else bandwidth reduces

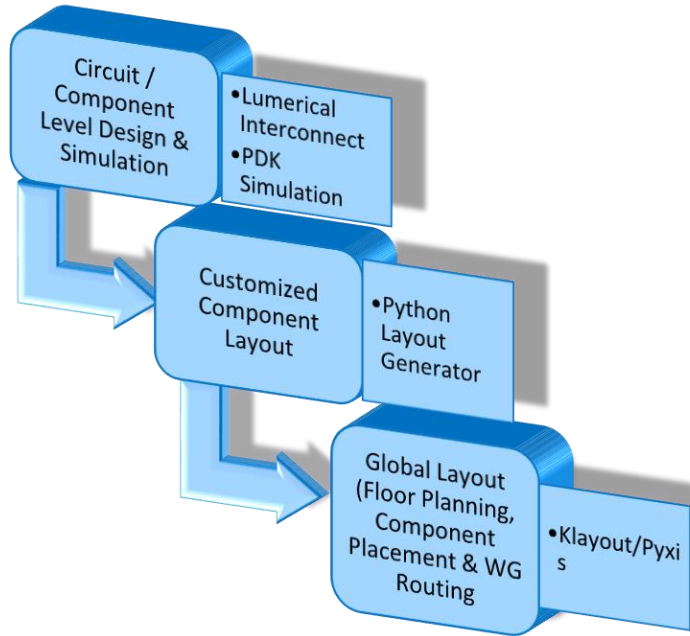
# Current-Mode MZM Driver



K. Zhu, V. Saxena, et al, "Design Considerations for Traveling-Wave Modulator Based CMOS Photonic Transmitters," IEEE TCAS-II, vol. 62, no. 4, pp. 412 – 416, April 2015.

# CMOS Photonic Co-simulation

## PIC Design Flow

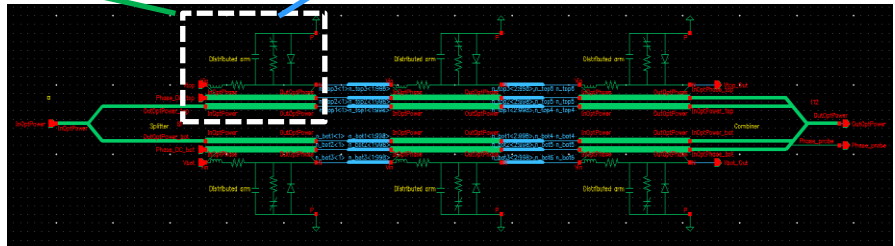
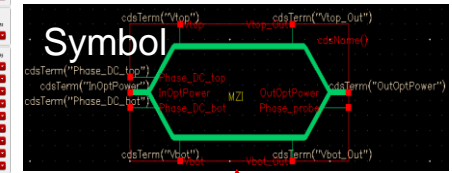


## Compact Models for Photonic Components

### Verilog-A

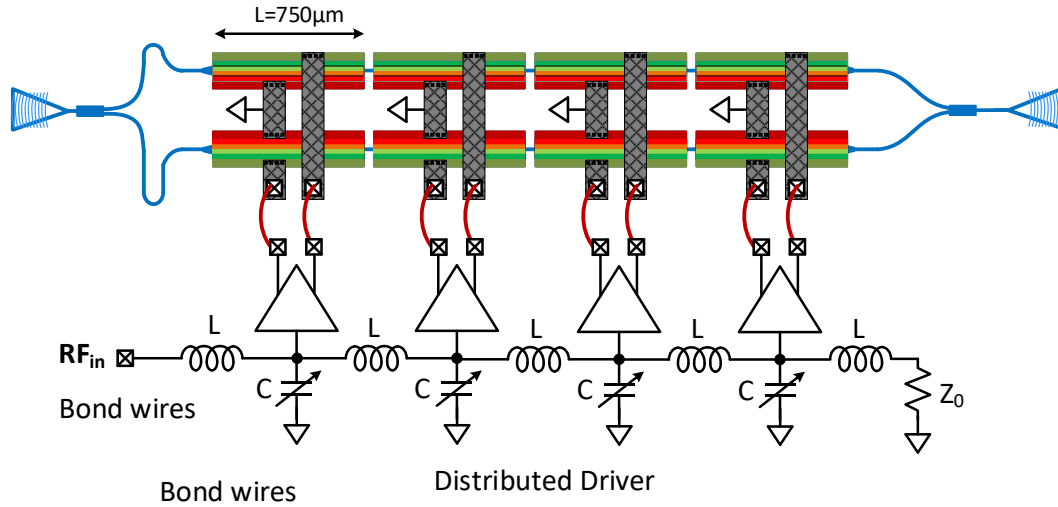
The image shows a Verilog-A code editor window with a snippet of code defining a component. To the right is the 'Edit Object Properties' dialog box for the component, showing various parameters like 'Phase', 'InOptPower', 'OutOptPower', 'Phase\_Dc\_top', 'Phase\_Dc\_bot', 'MZI', and 'Phase\_probe' with their respective values and units.

Editable component variables

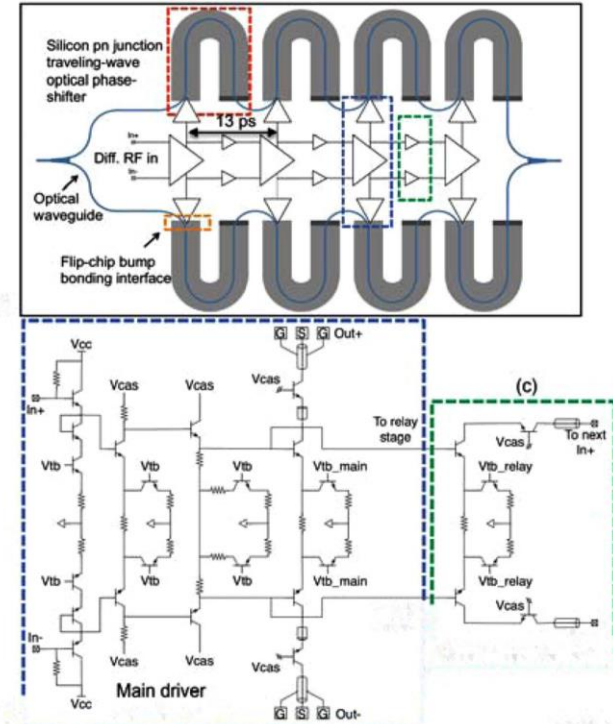


K. Zhu, Saxena, V., X. Wu, and W. Kuang, "Design Considerations for Traveling-Wave Modulator Based CMOS Photonic Transmitters," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, no. 4, pp. 412 – 416, April 2015.

# Distributed MZM Driver



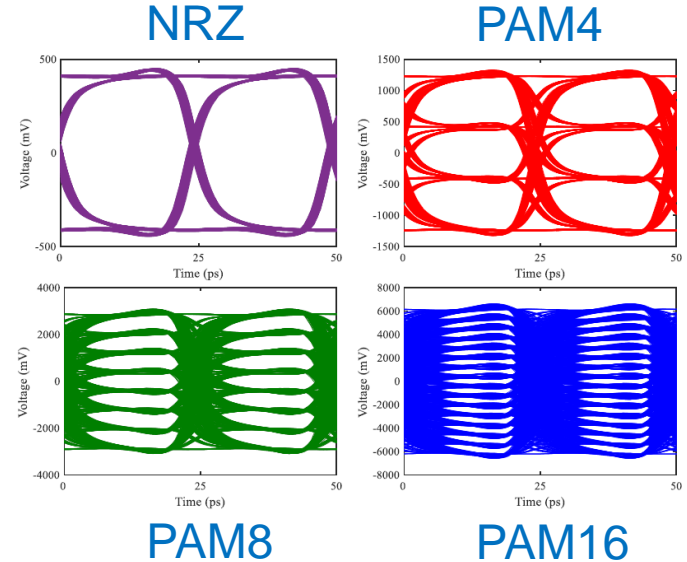
- Active transmission line
  - Lower RF loss in electrodes
- Voltage-mode drive
  - Segments driven as lumped capacitance
- Electrical and optical velocities matched



Ding, Ran, et al. "100-Gb/s NRZ optical transceiver analog front-end in 130-nm SiGe BiCMOS." 2014 Optical Interconnects Conference. IEEE, 2014.

# Advanced Modulation Transceivers

- IEEE 802.3bs standard included 400 Gb/s (25-100 Gb/s/λ) for short-range (<100m) interconnects
- The 802.3df roadmaps 800 Gb/s and 1.6 Tb/s using 112 Gb/s/λ and 224 Gb/s/λ interconnects
- The UCle chiplet ecosystem requires >5Tb/s/mm<sup>2</sup> bandwidth density
- Pulse amplitude modulation (PAM-4) doubles spectral efficiency
- Coherent links employ phase and/or polarization for quadrature amplitude modulation (QAM)

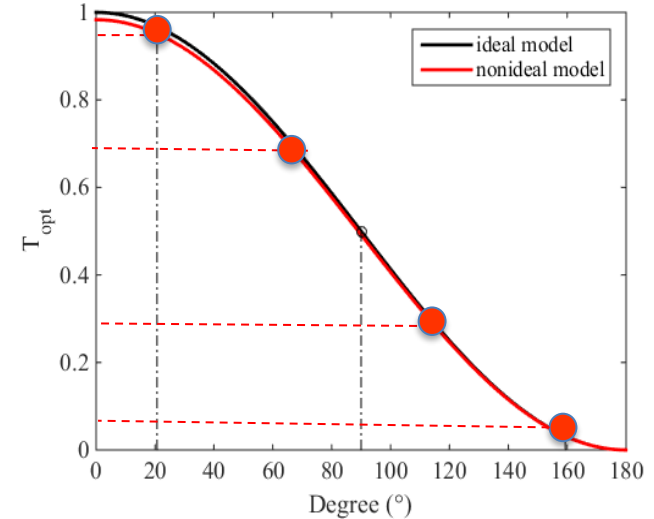
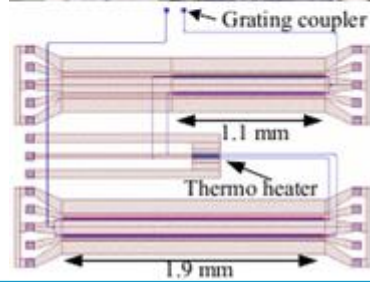
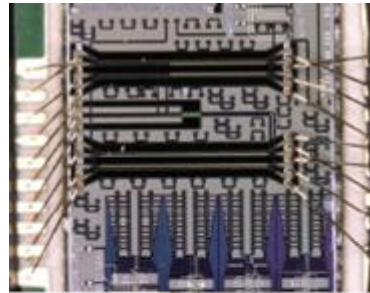
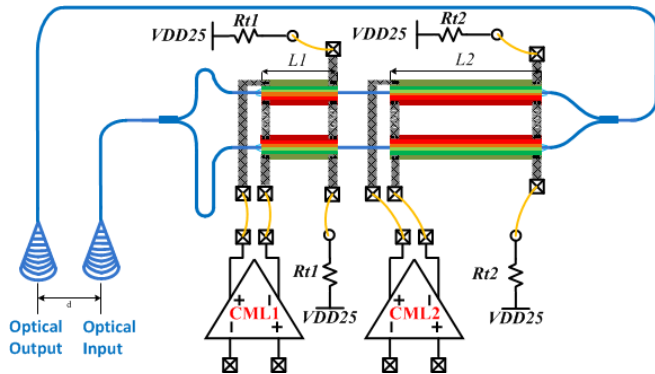


# Current-Mode PAM-4 with Segmented MZM

- Equivalent to 2-bit DAC processing signal in optical phase domain
- PAM4 Linearity is important

$$W = \begin{bmatrix} -1 & -1 & +1 & +1 \\ -1 & +1 & -1 & +1 \end{bmatrix}^T \text{ and } l = [L2 \quad L1]^T$$

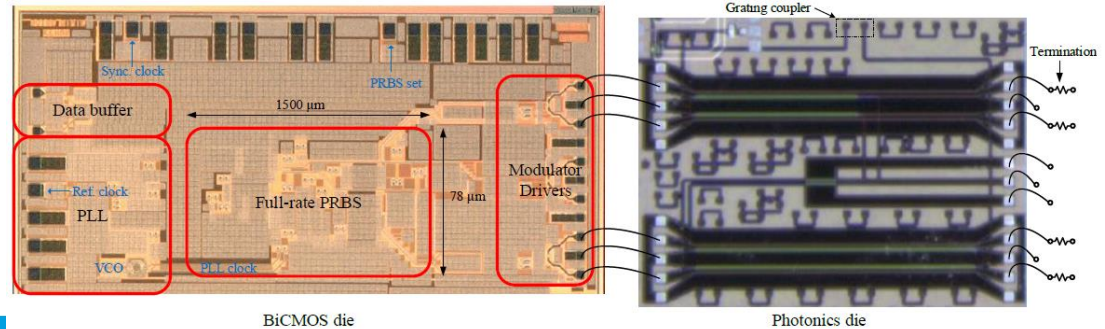
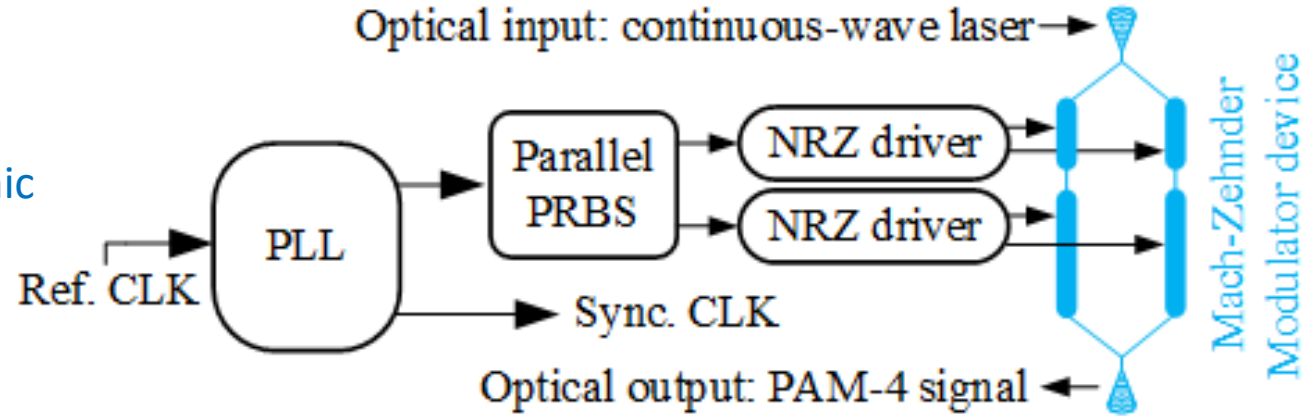
$$\Delta\phi_{DAC} = \frac{2\pi\Delta n_{eff}(V)}{\lambda} Wl$$



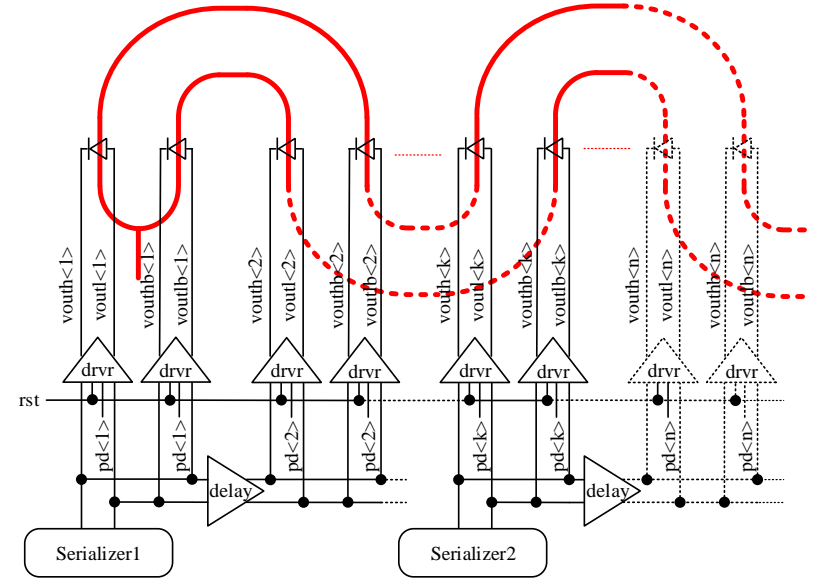
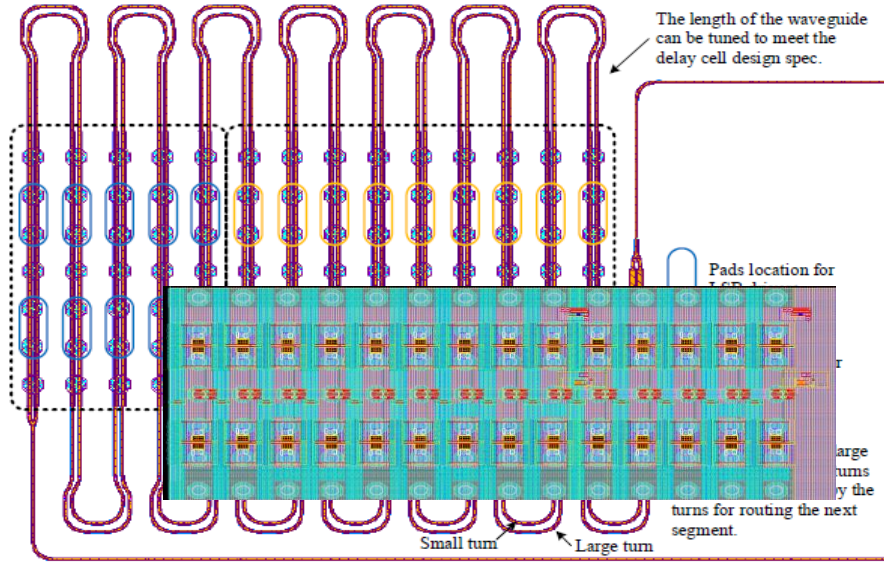


# PAM-4 Segmented MZM Driver

- IBM 8HP 130nm SiGe BiCMOS
- IME Silicon Photonic Process
- Chip-on-board packaging
- PLL for on-chip clock and data pattern generation

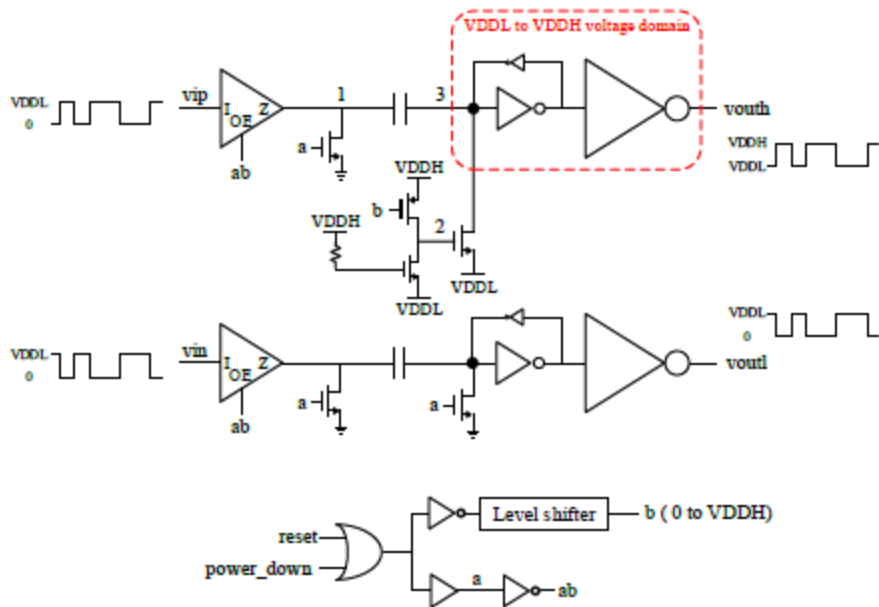


# CMOS-based Reconfigurable Segmented MZM

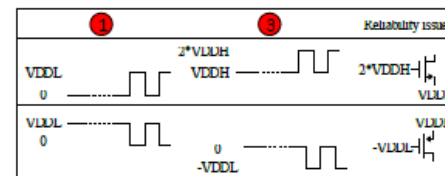
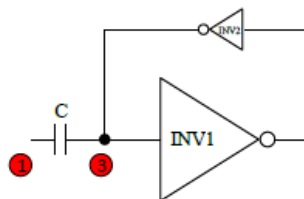
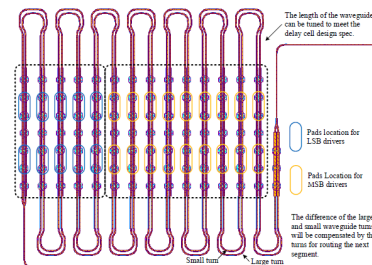


- Segment MZM arms and drive them like lumped elements (voltage-mode drive)
- Individual driver (drv) selectively powered by control signal  $pd\langle\#\rangle$
- NRZ can be achieved by only enable the LSB or MSB
- Different PAM-4 ER can be achieved by choosing between segment combinations

# Voltage-mode Segmented MZM

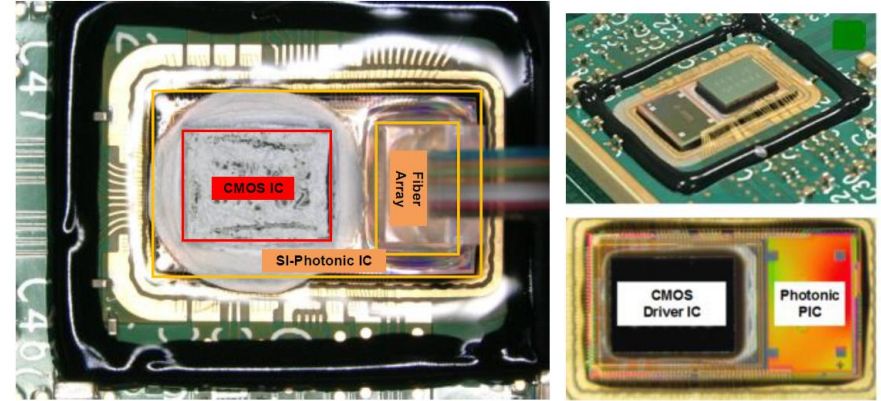
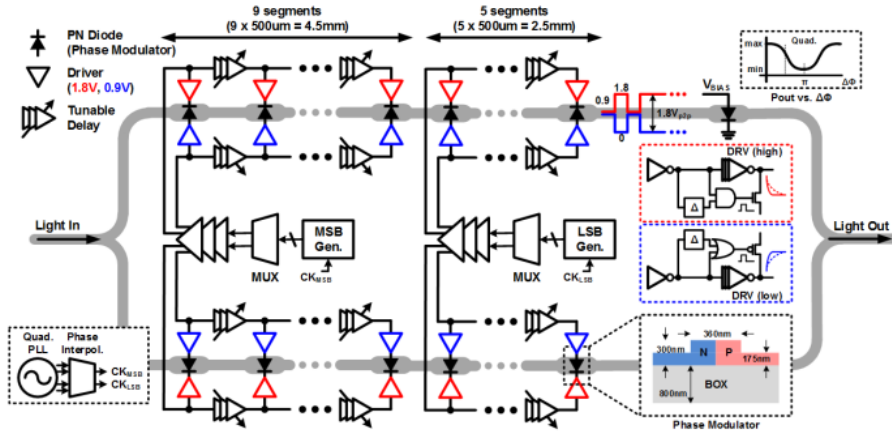


Push-pull inverter based driver



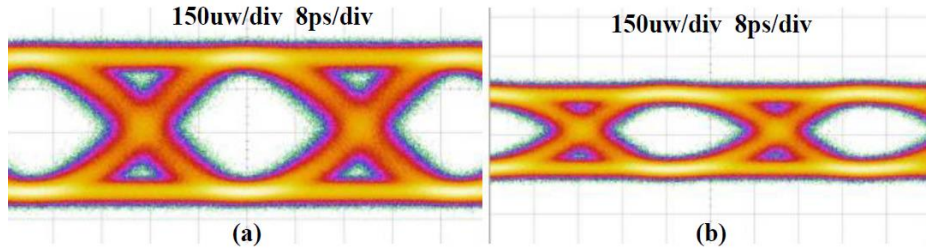
- Compared to the traditional AC coupling, the latch-based level shifter has no RC time constant constraint.

# Reconfigurable Segmented MZM

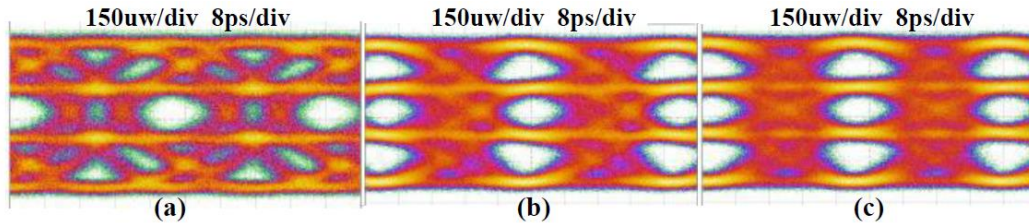


C. Li, K. Yu, J. Rhim, K. Zhu, N. Qi, V. Saxena, M. Fiorentino, and S. Palermo, "A 3D Integrated 56 Gb/s NRZ/PAM4 Reconfigurable Segmented Mach-Zehnder Modulator based Si-photonics Transmitter," in *IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2018.

# Reconfigurable Segmented MZM



28Gbps optical NRZ eye diagram (a) MSB driver enable only (b) LSB driver enable only.



56Gbps optical PAM-4 eye diagrams (a) without velocity mismatch compensation; (b) with phase interpolator aided compensation; (c) with both PI and delay line aided compensation.

TABLE II: PERFORMANCE SUMMARY

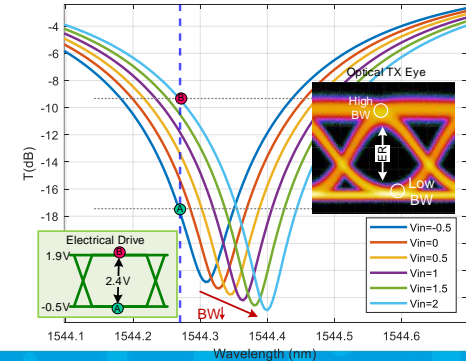
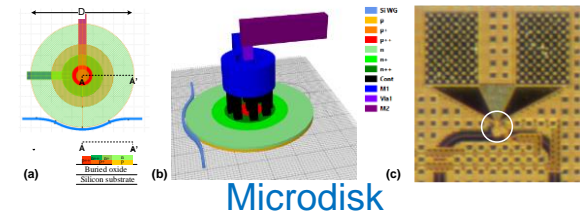
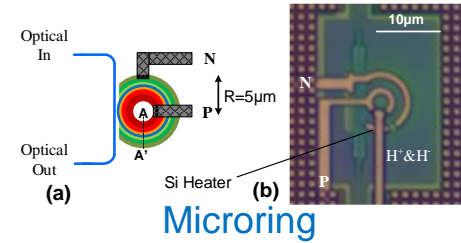
References	This Work	[4]	[5]	[6]	[7]
Data Rate (Gb/s)	56	25	56	50	56
Modulation	NRZ/PAM4	NRZ	NRZ	NRZ/PAM4	PAM4
Modulator Structure	SE	SE	TW	TW	TW
Integration Technology	Copper Pillar	Copper Pillar	Copper Pillar	Wire Bond	Monolithic
MZM Length	7mm	3mm	3mm	NA	3mm
Test Pattern	PRBS 23	PRBS 7	PRBS 31	PRBS 31	PRBS 23
Extinction Ratio (dB)	9.5	4-6	2.5	5.6	6
Power (mW)	708*	275	300	613	135mw@ 50Gbps
Power Efficiency (pJ/bit)	12.6 (ER=9.5 dB) 8.8 (ER=6.4 dB)	11	5.35	12.26	2.7
Technology	16nm FinFET (CMOS) 130nm SOI (Photonics)	65-nm CMOS	55-nm BiCMOS	65-nm CMOS	90-nm CMOS SOI

\*Clocking and data serialization and digital backends power are included

C. Li, K. Yu, J. Rhim, K. Zhu, N. Qi, **V. Saxena**, M. Fiorentino, and S. Palermo, "A 3D Integrated 56 Gb/s NRZ/PAM4 Reconfigurable Segmented Mach-Zehnder Modulator based Si-photonics Transmitter," in *IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2018.

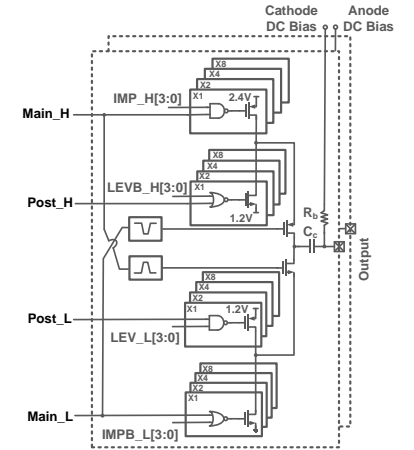
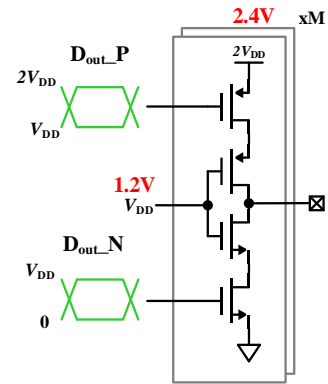
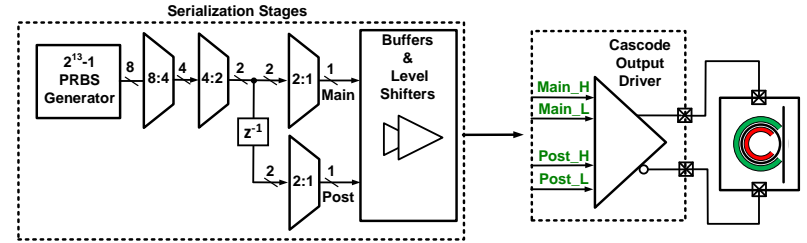
# Resonant Modulators

- Microring Modulators (MRM) & Microdisk modulators
- Resonant structure forces several roundtrips for the optical signal
  - More phase shift in a smaller geometry
- $3\mu\text{m}$ - $10\mu\text{m}$  ring radius
  - $\sim 3\mu\text{m}$  disk diameter
- Quality factor  $>8,000$
- Lumped load cap  $<100\text{fF}$
- Ideal for WDM links and high-density switches
- Resonance wavelength is process and temperature sensitive



# MRM NRZ TX Driver

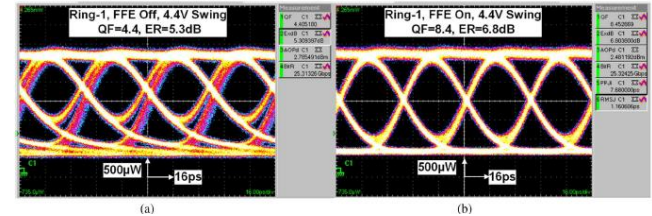
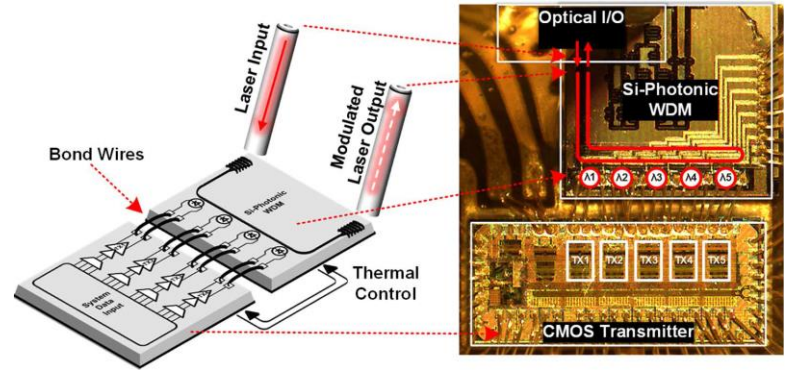
- Voltage-mode drivers
- $2V_{DD}=2.4V$  drivers realized using stacked CMOS transistors
  - $N=16$  tunable segments
- 4.4V driver realized using AC coupling
- High-Q rings exhibit unequal rise and fall times
  - Dynamic nonlinearity
  - Non-linear 2-tap FFE employed to equalize the eye



V. Saxena, V., A. Kumar, A., S. Mishra, S. Palermo, and K. R. Lakshmi Kumar, "Optical Interconnects Using Hybrid Integration of CMOS and Silicon-Photonic ICs," *IEEE TCAS II*, vol. 71, no. 3, 2023.

# MRM NRZ TX Driver

- MRMs and driver EIC are integrated using
  - Short wire-bonds
  - Flip-chip
  - Monolithic process
- Non-linear 2-tap FFE segment tuned to equalize the optical eye
- MRMs are amenable to WDM links
  - Each ring is tuned to the wavelength grid
  - A low-speed feedback controller is used to lock the MRM to its desired resonant wavelength



Hao Li, et al. "A 25 Gb/s, 4.4 V-swing, AC-coupled ring modulator-based WDM transmitter with wavelength stabilization in 65 nm CMOS." *IEEE JSSC*, vol. 50, no.12, pp. 3145-3159, 2015



# MRM NRZ TX Comparison

PERFORMANCE COMPARISON OF SiP MRM TRANSMITTERS.

	Technology	Ring-Mode	Supply Voltage	Data Rate	Output Swing	Equalization	Coupling	Efficiency <sup>†</sup> pJ/bit	Wavelength Stabilization	ER <sup>‡</sup>
Buckwalter [9] JSSCC2012	130nm SOI Monolithic	Depletion	1.5V, -1.5V	25Gbps	2.4 $V_{pp}$	Pre-emphasis	DC	10.2	N/A	6.6dB
Moss [3] ISSCC2013	45nm SOI Monolithic	Injection	1.1V, 1.5V	2.5Gbps	1.5 $V_{pp}$	Split Supply Pre-Emphasis	DC	1.23	N/A	3dB
Cheng Li [6] JSSC2014	65nm CMOS, 130nm SiP	Injection	1V, 2V	5Gbps	4 $V_{pp}$ 2 $V_{pp}$	Assymmetric Pre-Emphasis	DC	0.81	Auto-Align	12.7dB
Hao Li [2] JSSC2015	65nm CMOS, 130nm SiP	Depletion	1.2V, 2.4V	25Gbps	4.4 $V_{pp}$	2-Tap NL FFE	AC	4.532	Auto Align and Tracking	7dB
Rakowski [5] ISSCC2015	40nm LP CMOS, 130nm SiP	Depletion	1.3V	20Gbps	1.95 $V_{pp}$	No EQ	DC	1.6 <sup>∇</sup>	Manual	9dB
Chen [10] ISSCC2015	28nm CMOS Monolithic	Injection	0.9V, 1.8V	25Gbps	1.8 $V_{pp}$	2-Tap FFE	AC	4.9	Manual	6.5dB
Moazeni [4] ISSCC2017	45nm SOI Monolithic	Depletion	1V, 1.55V	20Gbps	1.55 $V_{pp}$	No dynamic EQ	DC	0.685	Auto Align	3dB
This Work	65nm LP CMOS, 130nm SiP	Depletion	1.2V	25Gbps	1.7 $V_{pp}$	2-Tap NL FFE	DC	1.85	Manual	5.86dB

<sup>†</sup>Energy-efficiency figure-of-merit (FoM) expressed as pJ/bit. The energy consumption of the thermal bias stabilization is not included. <sup>‡</sup>Extinction ratio (ER).

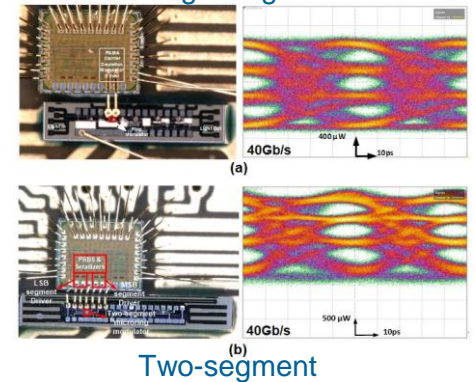
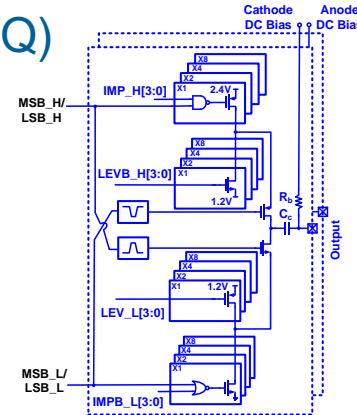
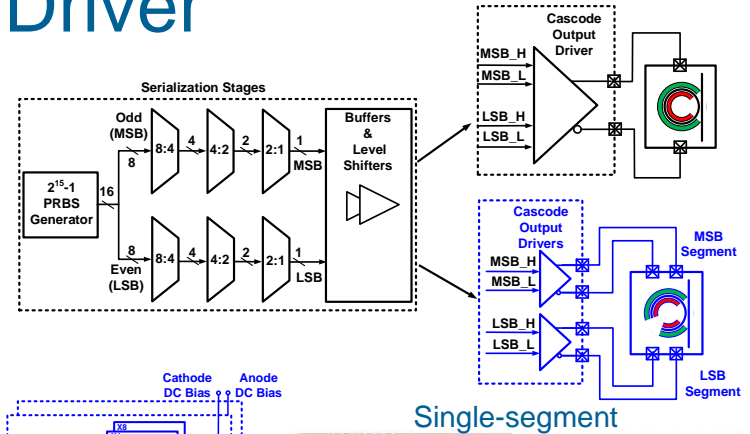
<sup>∇</sup> Doesn't include the serializer energy consumption.

- Monolithic integration enables <1pJ/b energy-efficiency
- Serializer consumes most of energy budget
- Higher MRM modulation efficiency allows lower voltage swing and lower power

S. Mishra et al. "A hybrid cmos photonic 25gbps microring transmitter with a-0.5–1.2 v direct-coupled drive." 2022 IEEE International Symposium on Circuits and Systems (ISCAS). IEEE, 2022.

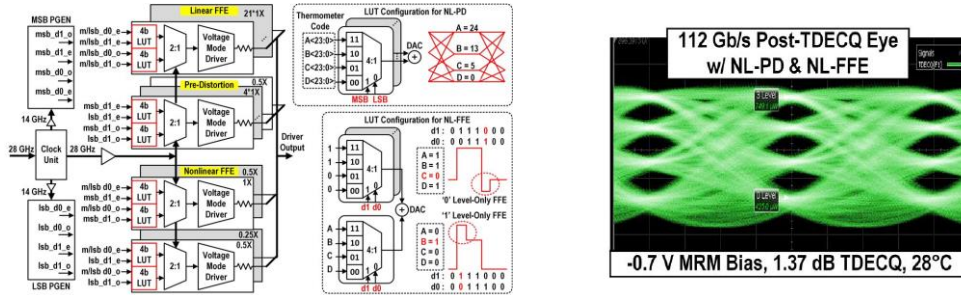
# MRM PAM4 TX Driver

- Single-segment and segmented MRM and driver designs
- MRM static nonlinearity causes degradation of ratio of level mismatch (RLM)
- MRM dynamic nonlinearity degrades the transmitter eye closure quaternary (TDECQ)
- Segmented MRM relaxes the linearity requirements
- Recent literature has more complex EQ schemes

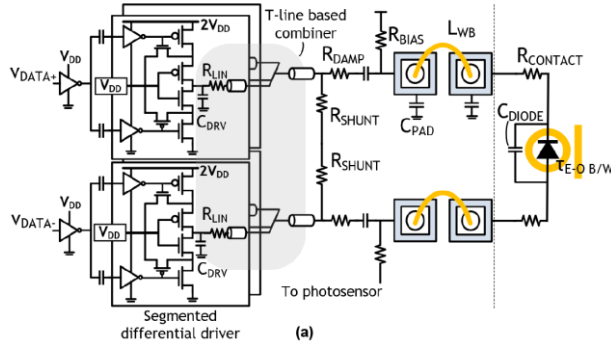


- V. Saxena, V., A. Kumar, A., S. Mishra, S. Palermo, and K. R. Lakshmi Kumar, "Optical Interconnects Using Hybrid Integration of CMOS and Silicon-Photonic ICs," *IEEE TCAS II*, vol. 71, no. 3, 2023.

# MRM PAM4 TX Comparison



Li, Hao, et al. "A 3-D-integrated silicon photonic microring-based 112-Gb/s PAM-4 transmitter with nonlinear equalization and thermal control." *IEEE Journal of Solid-State Circuits*, vol. 56, no. 1, pp. 19-29., 2020



J. Sharma, et al. "Silicon photonic microring-based 4x 112 Gb/s WDM transmitter with photocurrent-based thermal control in 28-nm CMOS." *IEEE JSSC*, vol. 57, no. 4, pp. 1187-1198, 2021.

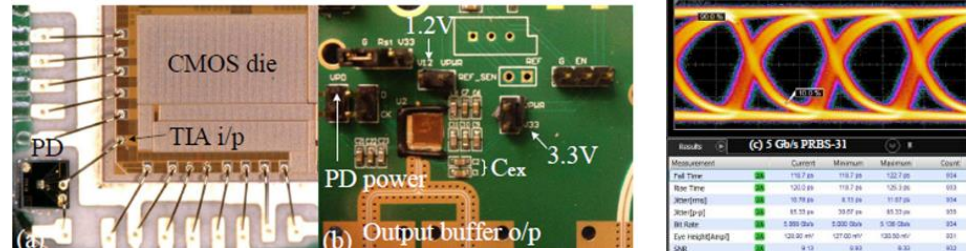
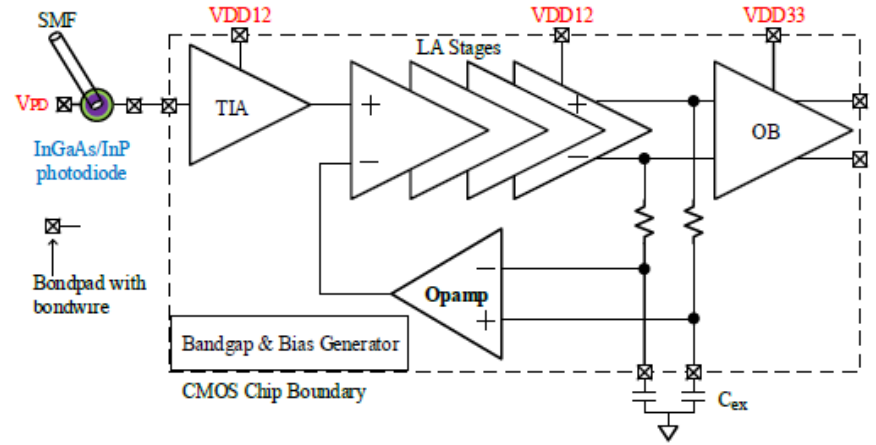
TABLE I  
MRM-BASED SI-PH WDM TX WITH INTEGRATED DRIVERS

Reference	This work	[35]	[25]	[15]	[21]	[14]
# Wavelengths	4	11	8	4	5	8
Laser band	O	O	O	O	C	C
Gb/s Per-λ	112	5	25	50	25	100
Modulation	PAM4	NRZ	NRZ	NRZ	NRZ	PAM4
FFE scheme	NL <sup>1</sup>	None	N/R <sup>2</sup>	None	NL	None
EIC process	28nm CMOS	45nm SOI CMOS (monolithic)	55nm SiGe	65nm CMOS	22nm CMOS	
Integrated thermal control	Yes	Yes	Yes	No	Yes	N/R
Thermal control sensor	MRM <sub>iPH</sub>	Drop port + MPD <sup>3</sup>	N/R	N/A <sup>4</sup>	MPD	N/R
Maximum heater DAC power (mW)	50	2	N/R	N/A	5	N/R
Tuning range (nm)	4.8	2.5	10	N/A	0.8	N/R
Tuning resolution (pm)	< 1	5	N/R	N/A	< 1	N/R
Measurement configuration	Per-λ	Per-λ	All-λ	Per-λ	Per-λ	All-λ
Energy efficiency (pJ/bit)	5.8	0.17	0.58 <sup>5</sup>	2	4.5	2.25
B/W Density (Gb/s/mm <sup>2</sup> )	448 <sup>6</sup>	391	N/R	N/R	250	370

<sup>1</sup>Nonlinear; <sup>2</sup>Not reported; <sup>3</sup>Monitor PD; <sup>4</sup>Not applicable; <sup>5</sup>Excluding clock; <sup>6</sup>Includes active area of TX per-channel clock, serialization, driver, bias and output networks, pads and TCU

# Traditional Optical Receivers

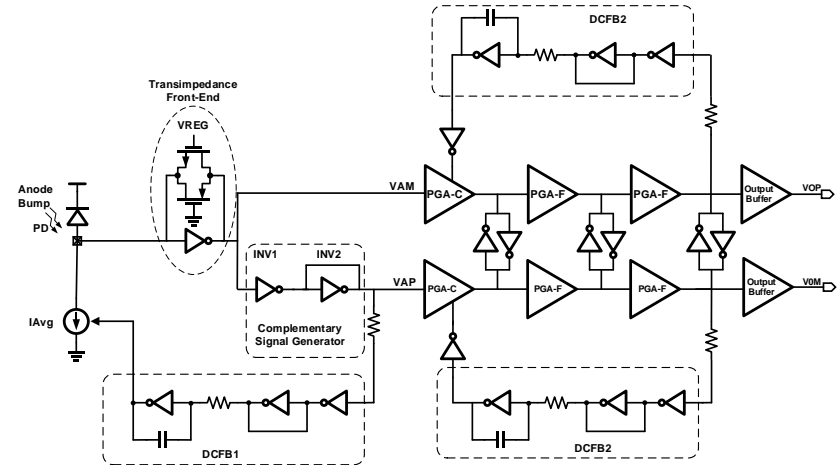
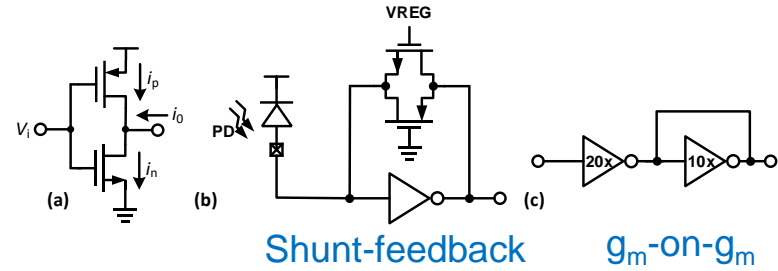
- III-V or on-PIC Ge Photo-detectors
  - >50GHz BW in SiP platforms
- First stage transimpedance amplifier (TIA) sets the overall sensitivity and linearity
  - Noise vs TIA bandwidth
- Limiting receivers for NRZ data
- Multistage amplifiers to obtain the required voltage swing
- A DC offset cancellation (DCOC) loop sets common-mode levels
- Output buffer to drive 50Ω load



K. Zhu and V. Saxena, "Case Study of a Hybrid Optoelectronic Limiting Receiver," IEEE TCAS I: Regular Papers 64.10 (2017): 2797-2805.

# Modern Optical Receivers

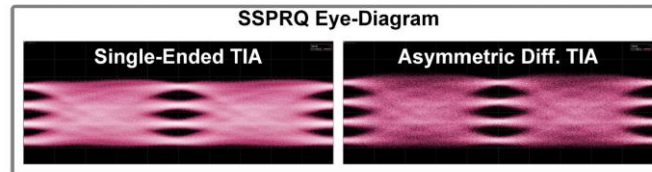
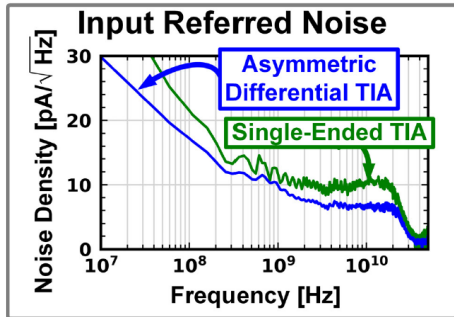
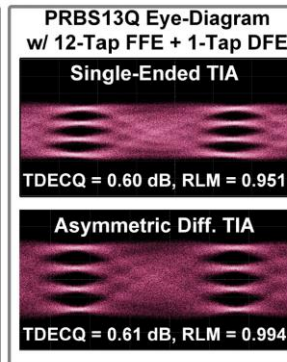
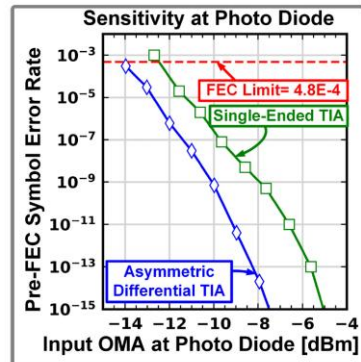
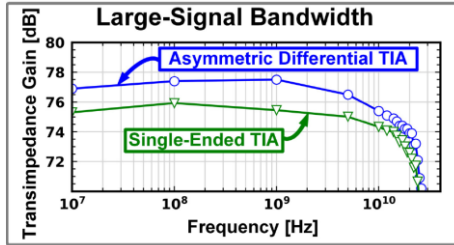
- SiGe BiCMOS RX are commonly used for high baud rates
- Receiver (RX) in advanced CMOS nodes allows higher integration and lower power
- PAM4 requires a linear RX to preserve symbol shape
- $i_o = i_n - i_p \approx (k_n V_{ov,n} - k_p V_{ov,p})v_i + \left(\frac{k_n}{2} - \frac{k_p}{2}\right)v_i^2$
- In 16nm FinFET,  $k_p \approx k_n$ , yielding linear transconductance
- Shunt-feedback or  $g_m$ -on- $g_m$  linear stages



Figures courtesy K. Lakshmikumar

K. R. Lakshmikumar et. al., "High-Performance CMOS TIA for Data Center Optical Interconnects," in IEEE BCI-CTS, 2022, pp. 9–16

# Modern Optical Receivers



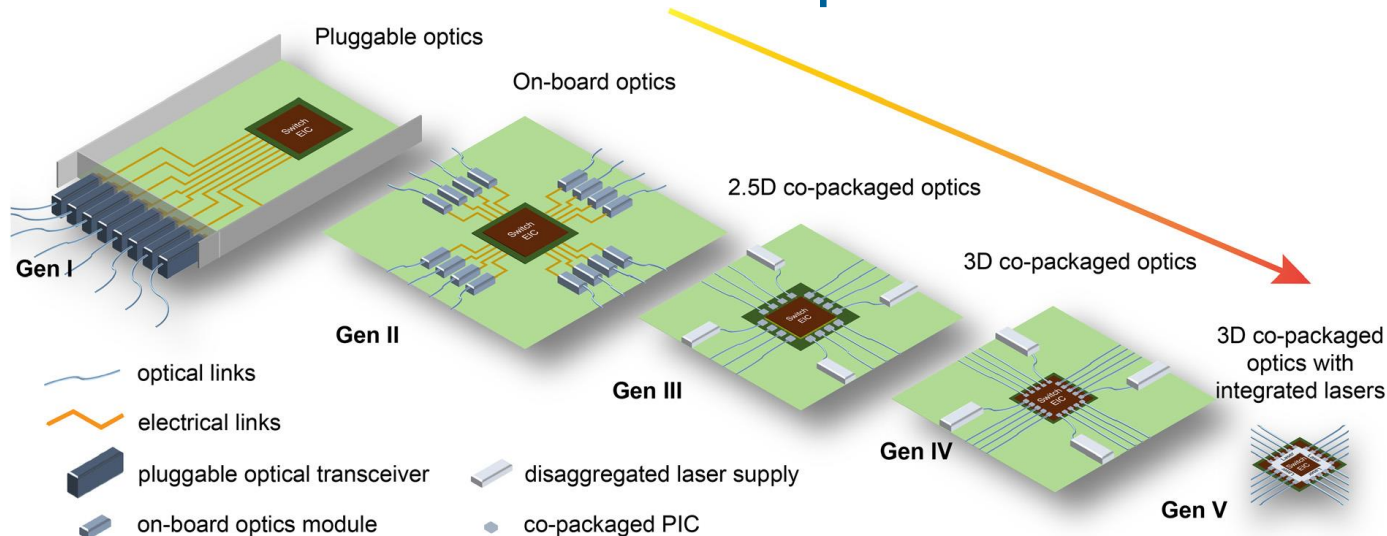
	JSSC'19 [1]	ESSCIRC'18 [2]	JSCC'22 [3]	CICC'22 [4]	PTL'19 [5]	This work	
Technology	16nm FinFET	28nm Bulk	28nm Bulk	16nm FinFET	55nm SiGe	16nm FinFET	
Data Rate (Gbps)	106.25	112	100	112	106	106.25	
Modulation Format	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4	
Supply Voltage (V)	1.8	2.5/1.2	1.5	0.9	3.3/2.5	1.8	3.3/1.8
TIA Architecture	Single-Ended	Single-Ended	Single-Ended	Single-Ended	Differential	Single-Ended	Differential
Optical Measurements	Yes	No	Yes	Yes	Yes	Yes	Yes
Bandwidth (GHz)	27	60	20	32	N/A	18.4	18.4
Transimpedance (d $\Omega$ )	78	65	66	63	66	75.5	77
Input ref. noise ( $\mu\text{A}_{\text{rms}}$ )	2.7 <sup>1</sup>	4.7	2.5	3	3.2	1.5	1.14
Input ref. noise density ( $\text{pA}/\sqrt{\text{Hz}}$ )	16.7	19.3	17	16.9	N/A	9.2	7
Power (mW)	60.8	107	117	47 <sup>4</sup>	160	103.6	108
Output Swing (mVpp diff.)	600 <sup>2</sup>	300	600 <sup>2</sup>	450	N/A	300	300
Sensitivity at KP4 pre-FEC SER (dBm)	-11 (5-tap FFE)	-5.1 <sup>5</sup> (5-tap FFE)	-8.9 (2-tap FFE + 2-tap DFE on-Chip)	-9.6 (4-tap FFE + 4-tap DFE)	-5 <sup>6</sup> -7 <sup>6</sup>	-12.48 (12-tap FFE + 1-tap DFE)	-13.97 (12-tap FFE + 1-tap DFE)

<sup>1</sup>Calculated <sup>2</sup>Without 50 $\Omega$  termination <sup>3</sup>Simulated <sup>4</sup>No supply regulation <sup>5</sup>In-fiber OMA <sup>6</sup>Calculated with PD responsivity

Figures courtesy K. Lakshmikumar

- K. Lakshmikumar et. al., "A 7  $\text{pA}/\sqrt{\text{Hz}}$  Asymmetric Differential TIA for 100Gbps PAM-4 links with -14dBm Optical Sensitivity in 16nm CMOS," in IEEE ISSCC, 2023, pp. 206–207
- V. Saxena, V., A. Kumar, A., S. Mishra, S. Palermo, and K. R. Lakshmikumar, "Optical Interconnects Using Hybrid Integration of CMOS and Silicon-Photonic ICs," *IEEE TCAS II: Express Briefs*, vol. 71, no. 3, 2023.

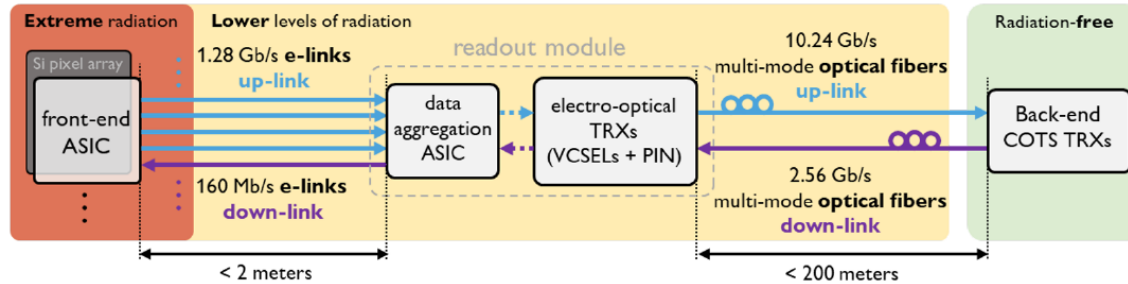
# Evolution of Data Center Optical Interconnects



- Pluggable modules to co-packaged optics (CPO) with the Switch ASIC
- Disaggregated laser supply in earlier generations, now heterogeneously integrated
- Industry is moving towards DSP-based links
  - DSP and DAC/ADC are integrated in the Switch ASIC
  - TX drivers and RX need to be linear

Margalit, N. et al., "Perspective on the future of silicon photonics and electronics," *Appl. Phys. Lett.* 118, 220501 (2021).

# SiP Interconnects for HEP Applications



- Thousands of VCSEL-based optical data transmission links are used in LHC
  - Transmission of timing, control, and read-out of HEP detectors
- VCSEL-based links are susceptible to performance degradation at higher radiation
  - Bulky electrical links are used in extreme radiation zone; limits scaling
- SiP based transceivers are being developed for next generation readout
  - Can deliver >50Gb/s/lane data rates, higher level of integration, and lower optical fiber count
- Rad-hard MZM designs employ optimized doping levels and compact device footprint

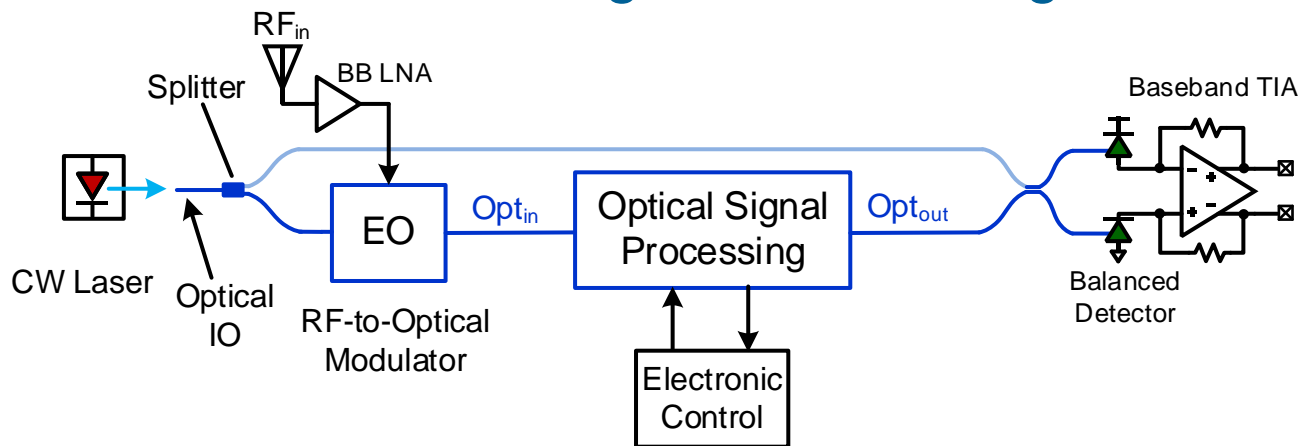
- Cammarata, S., et al. "Compact silicon photonic Mach-Zehnder modulators for high-energy physics." *Journal of Instrumentation* 19.03 (2024): C03009.
- El Nasr-Storey, Sarah Seif, et al. "Silicon photonics for high energy physics data transmission applications." *11th International Conference on Group IV Photonics (GFP)*. IEEE, 2014.



# RF Photonic Signal Processing

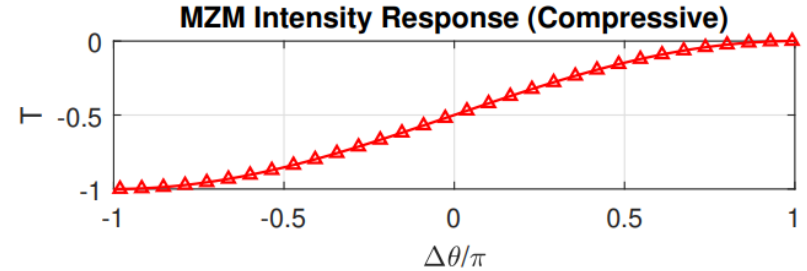
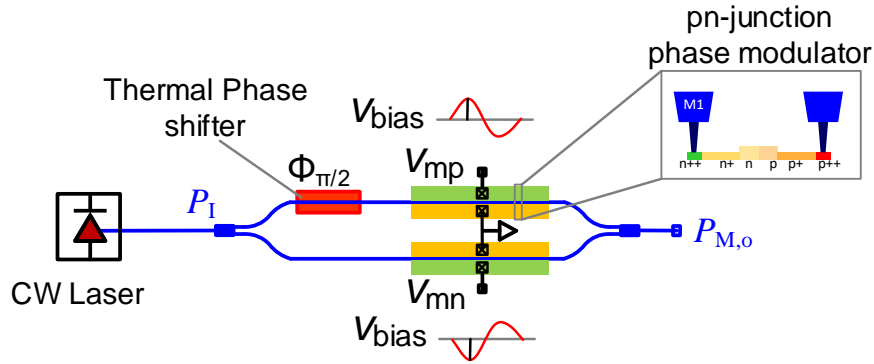
## Linear EO Modulators

# RF Photonic Signal Processing



- Optical-domain RF signal processing allows very wide bandwidths and tunability over a large frequency range
- Widely-tunable RF front-end for software-designed radio (SDR) is a long-standing challenge for electronics
- Requires a highly-linear RF-to-optical (EO) modulator for RF modulation of the laser
- Radio-over-fiber analog links

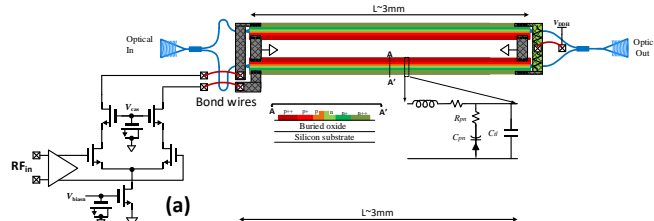
# Modulator Nonlinearity



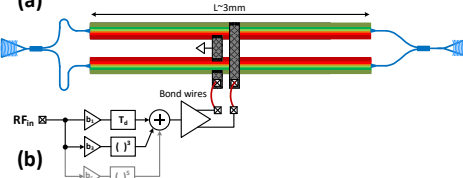
- MZM presents odd-order nonlinearity (assuming no mismatch between arms)
  - Biased at quadrature point
- Significant nonlinearity limits SFDR below  $100\text{dB}/\text{Hz}^{2/3}$ 
  - Insufficient for RF photonic or radio-over-fiber applications
- Ring modulator presents even-order as well as odd-order non-linearity

# MZM Linearization Schemes

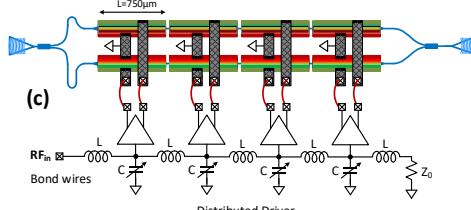
TWMZM  
Driver



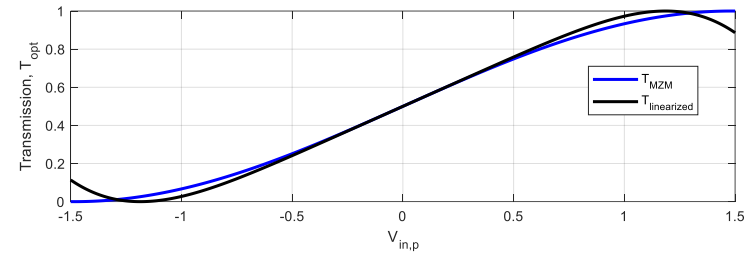
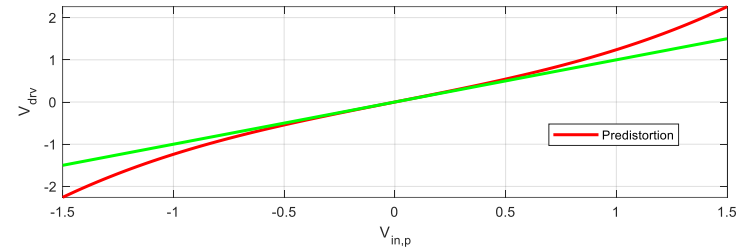
Electronic  
Predistortion



Distributed  
Electronic  
Predistortion



Dual parallel  
MZM



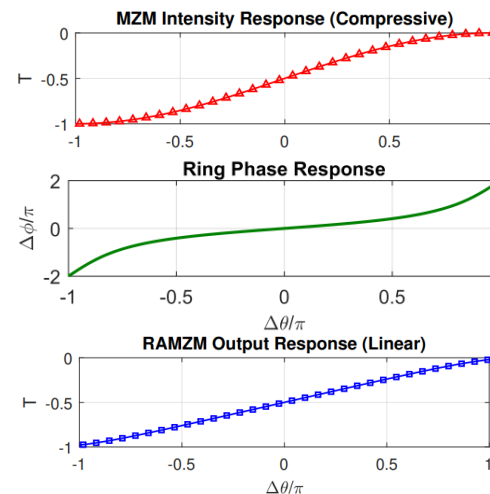
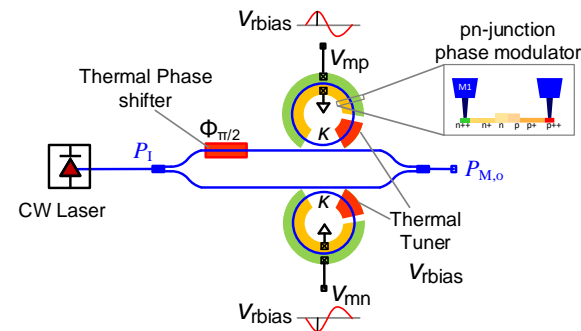
$$\varphi = f(V)$$

$$T_{opt,MZ} = \sin\left(\frac{\varphi_{top} - \varphi_{bot}}{2}\right)$$

$$V_{pre} = \beta_1 V + \beta_3 V^3$$

# Ring-Assisted Mach-Zehnder Modulator (RAMZM)

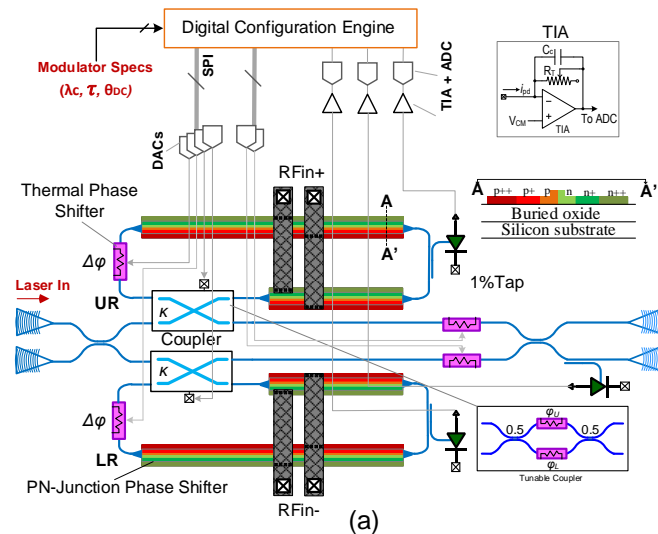
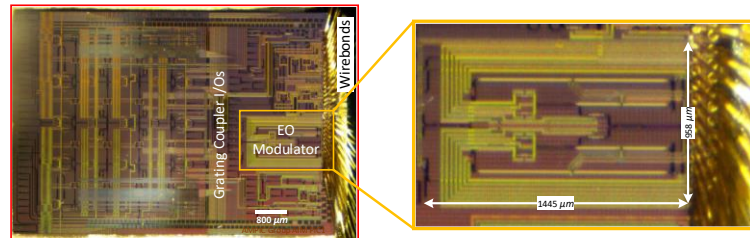
- Broadband active linearization of the MZM response required 3X bandwidth
- Ring-assisted Mach-Zehnder Interferometer (RAMZI)
  - Overcoupled ring exhibits expansive voltage-to-phase (V2P) response
  - MZ combiner has compressive phase-to-intensity (P2I) response
  - The V2P and P2I can be made to compensate each other at an optimal coupling ( $\kappa$ )
  - Higher-linearity with passive RF drive



Md J. Shawon and V. Saxena. "Automatic In-situ Optical Linearization of Silicon Photonic Ring-Assisted MZ Modulator for Integrated RF Photonic SoCs," *OFC 2023*, Feb 2023.

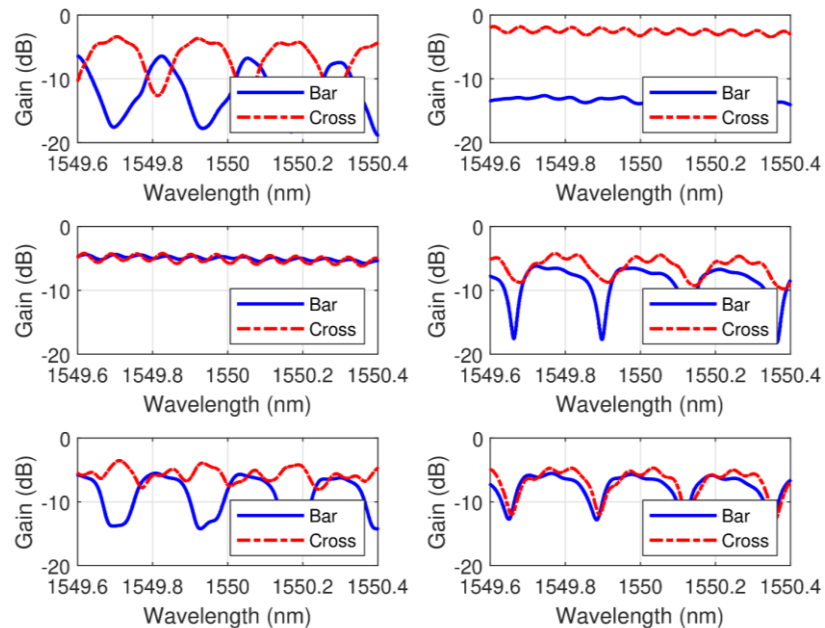
# RAMZM PIC

- Mach Zehnder arms are loaded with ring modulators
  - Differentially driven (push-pull)
- Tunable couplers are realized using 2x2 switch
- 1% and 10% detector taps to assist with chip configuration
- Microheaters for bias tuning
- Electronic backend for tuning algorithm



# Automatic In-situ Tuning (Anti-resonance)

- Laser is aligned with the anti-resonance
- Automatic tuning algorithm biases the two rings in anti-resonance, and the outer MZI in quadrature bias

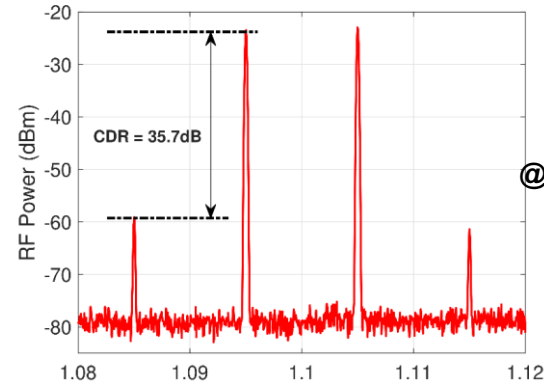


Tuning Steps

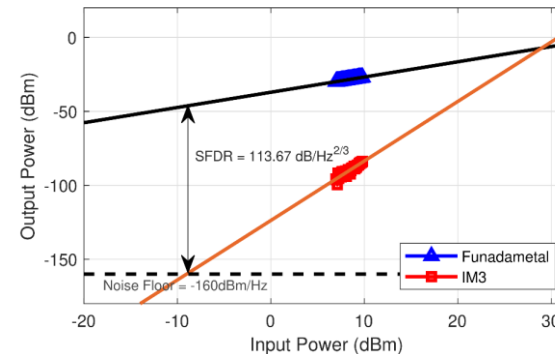
Md J. Shawon and V. Saxena. "Automatic In-situ Optical Linearization of Silicon Photonic Ring-Assisted MZ Modulator for Integrated RF Photonic SoCs," *2023 Optical Fiber Communication Conference (OFC)*, San Diego, Feb 2023.

# RAMZM SFDR (IM3 Products)

- Experimental results demonstrate record linearity in silicon photonic modulators
- SFDR with two-tone test around 1GHz  $\sim 110.11 \text{ dB}\cdot\text{Hz}^{2/3}$ 
  - Over 18dB improvement
- This was a lumped design with Kerr linearized pn-junction of 1.5mm length
  - Bandwidth with  $50\Omega$  drive is around 3GHz
- Bandwidth can be extended to 20GHz with a linear driver in BiCMOS technology
- Shows promise for Active COB or standalone block for RF Photonics



**CDR: 35dB**  
**@Fundamental Tone**  
**power of**  
**-23.46dBm**



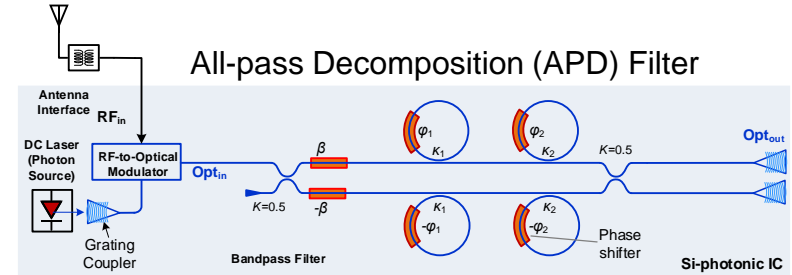
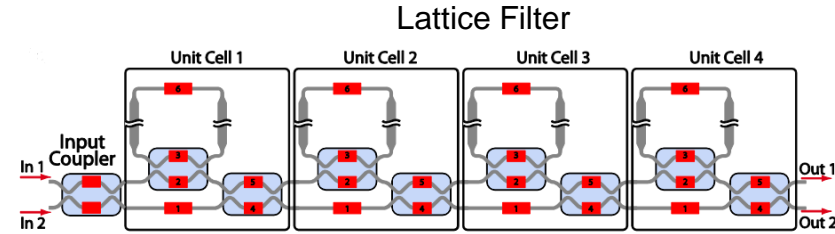
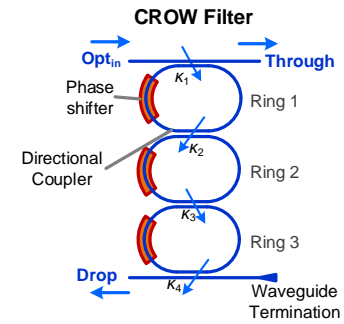
**SFDR**  
**113dB.Hz<sup>2/3</sup>**



# Integrated Optical Filters

# Optical Filters in SiP Platform

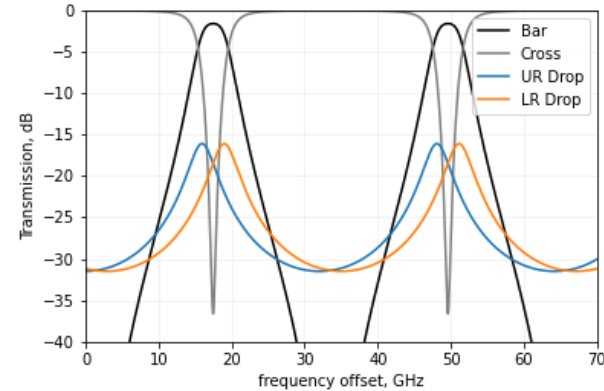
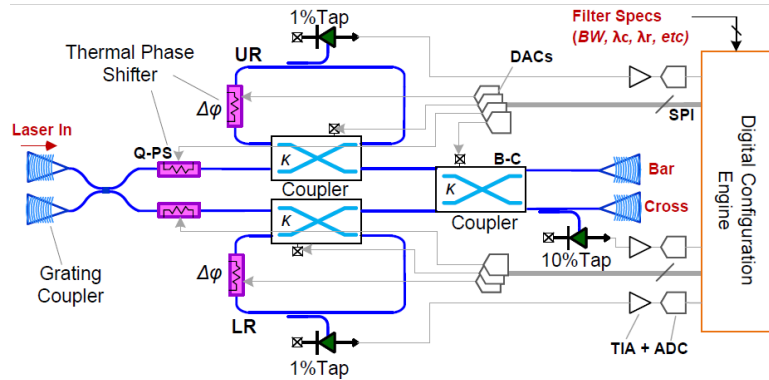
- SiP Filter Topologies:
  - FIR filters: Delay line based
  - IIR filters: Bragg gratings, Ring Based
  - Lattice structure (2N+1 couplers, 2N phase shifters)
  - APF (N+2 couplers, N+2 phase shifters)
- APF requires less couplers and phase shifters



<sup>1</sup> S. Ibrahim, et al., "Demonstration of a fast-reconfigurable silicon cmos optical lattice filter," *Optics express*, vol. 19, no. 14, pp. 13245–13256, 2011.

<sup>2</sup> G. Choo, et. al, "Automatic Monitor-Based Tuning of Reconfigurable Silicon Photonic APF-Based Pole/Zero Filters," in *JLT*, vol. 36, no. 10, pp. 1899-1911, 2018

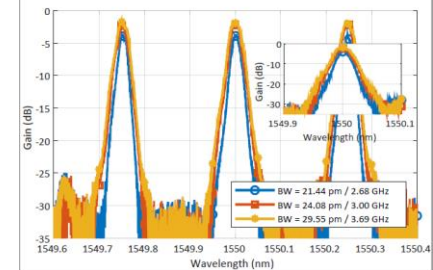
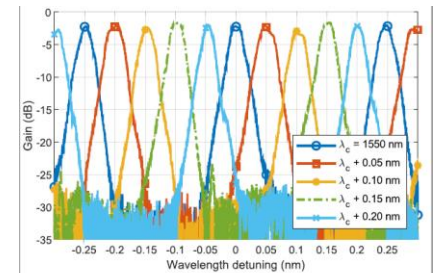
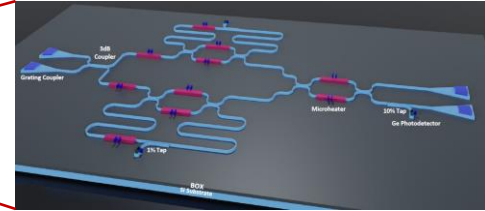
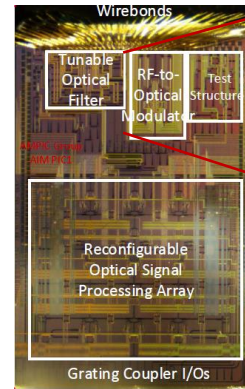
# Automatic Tuning of RF Photonic Filters



- On-chip 1% optical taps serve as observables
- Thermo-optic phase shifters provide controllability
- Configure desired filter response on the fly
- Algorithms to estimate and compensate for thermal crosstalk

# RF Photonic Filter PIC

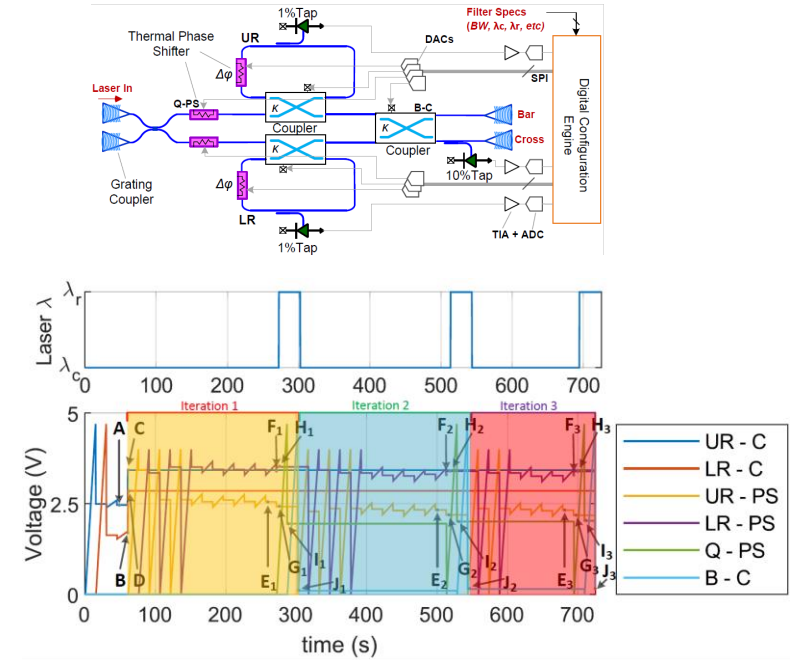
- Fabricated in AIM Active SiP process
- Automatic in-situ filter reconfiguration
- Developed algorithms to tune optical components to achieve the desired filter shape and center frequency
- Can tune filter center frequency over 25GHz FSR and BW
- Min BW~3GHz with 2.2dB insertion loss



Md J. Shawon, and V. Saxena, "Fully Automatic In-Situ Reconfiguration of RF Photonic Filters in a CMOS-Compatible Silicon Photonic Process," *IEEE J. Lightwave Technology*, vol. 41, no. 5, pp. 1286-1297, 2023.

# RF Photonic Filter Tuning

- The residual thermal crosstalk still creates coupling between components
- An iterative algorithm is developed to first characterize each coupler
- Use on-chip monitors to center the ring center wavelength, coupling coefficients and sideband suppression
- Current state-of-the-art is ~300-700 seconds for filter reconfiguration
  - Needs to be significantly reduced to a few seconds or lower for SDR
  - Need to drastically reduce thermal xtalk

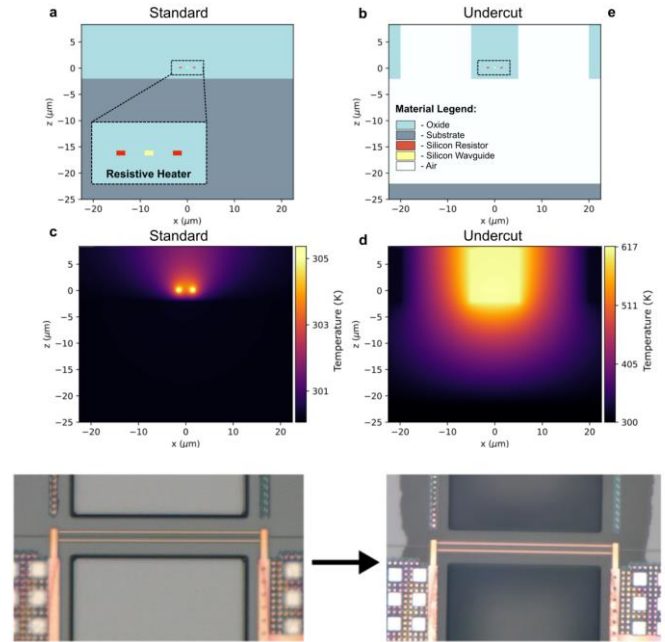


Filter Tuning Process

Md J. Shawon, and V. Saxena, "Fully Automatic In-Situ Reconfiguration of RF Photonic Filters in a CMOS-Compatible Silicon Photonic Process," to appear in *J. Lightwave Technology*, 2023.

# Roadmap for LSPICs

- We have pursued large-scale PICs (LSPICs) for signal processing and computing
- Encountered and addressed major challenges with PIC scaling with the SiP foundry processes available now
  - We demonstrated low-cost packaging approaches, electronic interfaces and configuration algorithms
- Thermal crosstalk is a primary challenge to scaling
  - Process improvements and new materials can help address this challenge



Rizzo, Anthony, et al. "Petabit-Scale Silicon Photonic Interconnects With Integrated Kerr Frequency Combs." *IEEE Journal of Selected Topics in Quantum Electronics* 29.1: Nonlinear Integrated Photonics (2022): 1-20.

# Conclusion

- Availability of silicon photonic foundry platforms enables fabrication of large-scale PICs
- SiP based optical Interconnects continue to evolve and gain market share
  - Application in HEP readout
  - SiP devices have shown promise in high radiation environment
- Packaging of EICs and PICs requires careful planning
- LSPICs can address several applications in signal processing and computation

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- Any opinions, findings and conclusions expressed are those of the authors and do not necessarily reflect those of the sponsor.





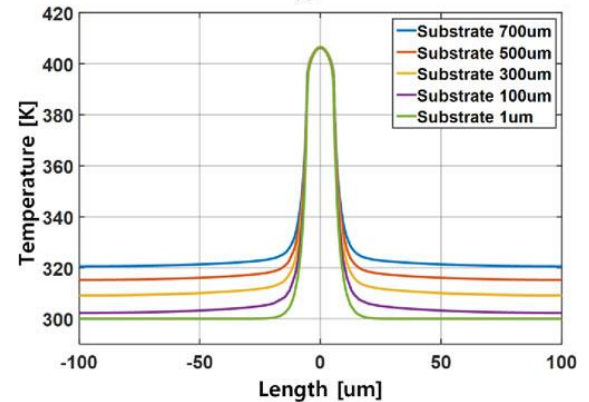
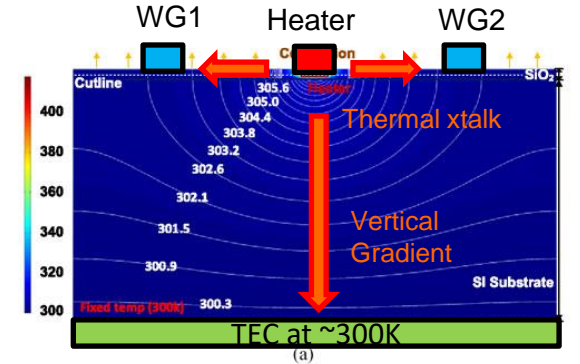
# Questions?



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# Challenges with PIC Scaling: Thermal Crosstalk

- Thermo-optic is the most effective PIC tuning mechanism
  - Doped waveguide or metal heaters create optical phase shifts localized heating
- Microheaters crosstalk (xtalk) with other optical components through the substrate
  - Small amount through the inter-layer dielectric as well
- Thermal crosstalk poses significant difficulty in PIC configuration and tuning
- Challenging problem as the NxN Adjacency matrix has non-diagonal terms for N tunable components on PIC
- In our PICs, thermal crosstalk is managed by using a combination of die thinning and thermal management



Thermal crosstalk from a single heater as a function of substrate thickness. A TEC is located at the bottom of the substrate<sup>1</sup>