22FDX Cryogenic Modeling

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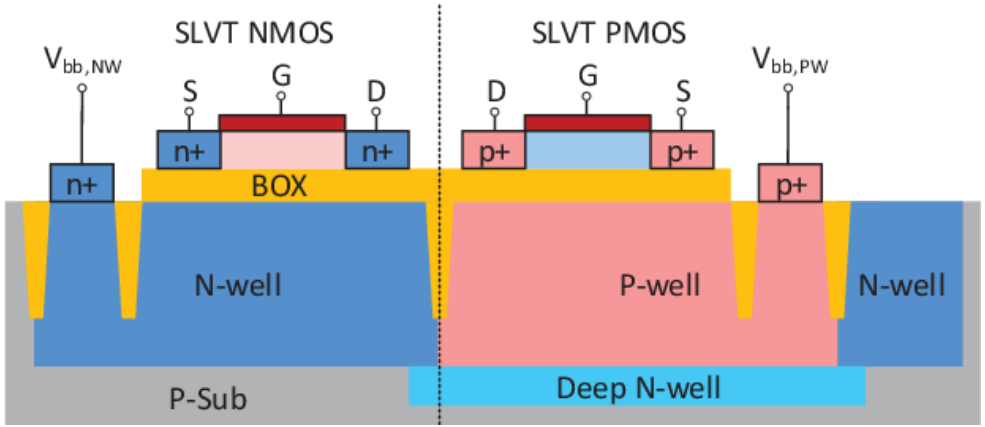
HEPIC Workshop 2024

22FDX Advantages for RF/Analog Design

- Confined electrons in an undoped channel and total dielectric isolation → ultra low leakage
- Fully depleted → lower power
- Tighter V_T distribution
- Low parasitics → faster switching
- Ultra thin body → Reduced short channel effect, DIBL
- Back gate used to recover threshold shift at cryo → critical for low power at cryo



[1]

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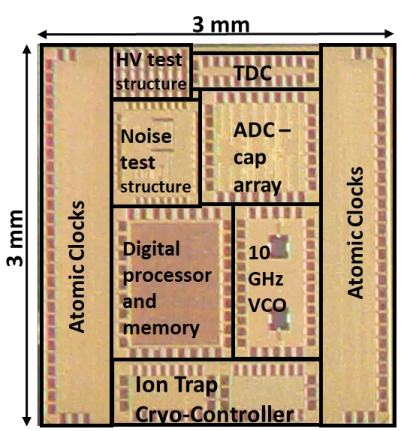
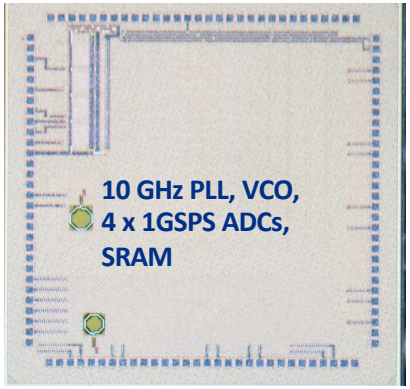
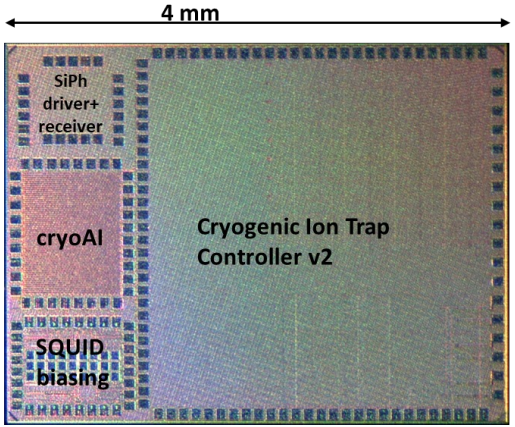
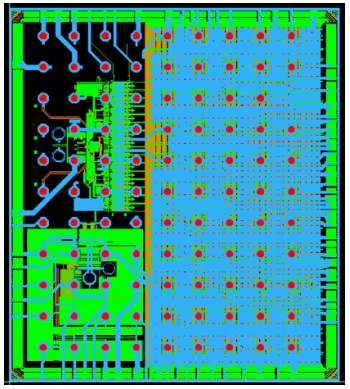
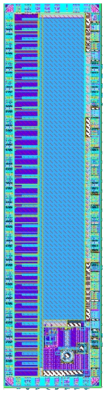
22FDX cryoChips at Fermilab











- **GF_test chip: (**11/21) Various designs
- **Michigan:** (07/22) 10 GHz PLL, VCO, 4 x 1GSPS ADCs, SRAM
- **Cryogenic Ion trap controller:** (01/23) 16 channel Ion trap control chip;
- **Si Photonic driver/receiver**;
- **cryoAI:** ultrafast NN for anomaly detection;
- **SQUIDDAC**: SLUG_biasing; various level shifter test structures
- **Glebe:** (with Microsoft) 10 GSPS ADC
- **Sunrock:** 32 channel SNSPD readout with ~ps time tagging

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Overview of Fermilab's 22FDX Cryo-CMOS modeling activities

Fermilab is leading several activities for the cryogenic characterization of 22FDX transistors:

GlobalFoundries™

EPFL

SYNOPSYS®
Silicon to Software™

With EPFL:

- Measurements of transistors at 4K
- Development of simplified EKV model for analog design
- Low noise test structure measurements

With Synopsys:

- Extraction of PDK-compatible BSIM-IMG (independent multi-gate) for 4K

In-house:

- Measurement and modeling of high voltage devices at 4K (BOXFET, LDMOS)
- ML/AI for Cryo-modeling

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22FDX Cryogenic modeling - EKV

Collaboration with EPFL (Han, Enz, Charbon) for simplified EKV (S-EKV) modeling for inversion coefficient design methodology (for analog design)

Only four parameters:

1. n = slope factor
2. I_{spec} = specific current
3. V_{T0} = threshold voltage without short-channel effects
4. λ_c = parameter for velocity saturation

Developed an open-source Python-based parameter extractor (SEKV-E) for the simplified EKV (sEKV) model
https://gitlab.com/moscm/sekv-e

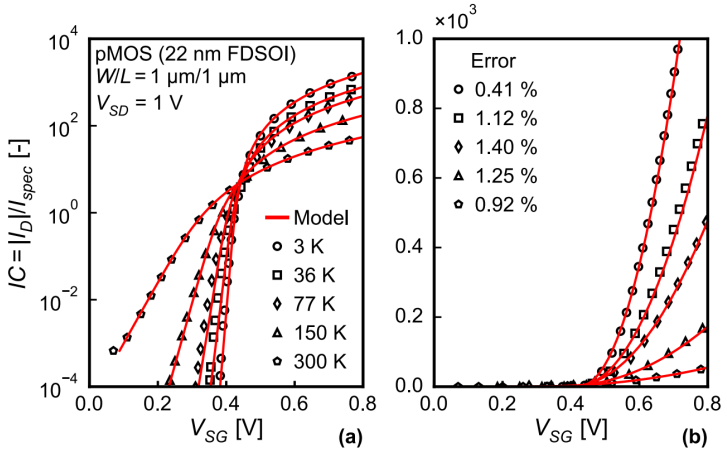


FIGURE 5. **Applying SEKV-E to a pMOS device of 22 nm FDSOI technology in saturation with V_{back} = 0 V [14] from room temperature down to deep cryogenic temperature. The legend in (b) shows the percent error.**

- Han, Hung-Chi, Antonio D'Amico, and Christian Enz. "Comprehensive Design-oriented FDSOI EKV Model." *2022 29th International Conference on Mixed Design of Integrated Circuits and System (MIXDES)*. IEEE, 2022.
- H.-C. Han, F. Jazaeri, Z. Zhao, S. Lehmann, C. Enz, "*An improved subthreshold swing expression accounting for back-gate bias in FDSOI FETs*", in *Solid-state Electronics*, vol. 202, 108608, April 2023. Doi: 10.1016/j.sse.2023.108608
- Han, Hung-Chi, et al. "In-depth cryogenic characterization of 22 nm FDSOI technology for quantum computation." *2021 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS)*. IEEE, 2021.
- Han, Hung-Chi, et al. "Cryogenic RF Characterization and Simple Modeling of a 22 nm FDSOI Technology." *ESSDERC 2022-IEEE 52nd European Solid-State Device Research Conference (ESSDERC)*. IEEE, 2022.
- H. -C. Han, A. D'Amico and C. Enz, "SEKV-E: Parameter Extractor of Simplified EKV I-V Model for Low-Power Analog Circuits," in IEEE Open Journal of Circuits and Systems, vol. 3, pp. 162-167, 2022, doi: 10.1109/OJCAS.2022.3179046.

Measurement data (300K and 3.8K, N/PFets):

EGLVT Flavor:

- Gate lengths: 0.07/0.2/2um
- Gate widths for each length: 0.16/0.5/2um
- Vd=0.01, 1.2, 1.5, 1.8V for various Transfer Characteristics
- Vg=1.0, 1.4, 1.8V for various Output Characteristics

SLVT Flavor:

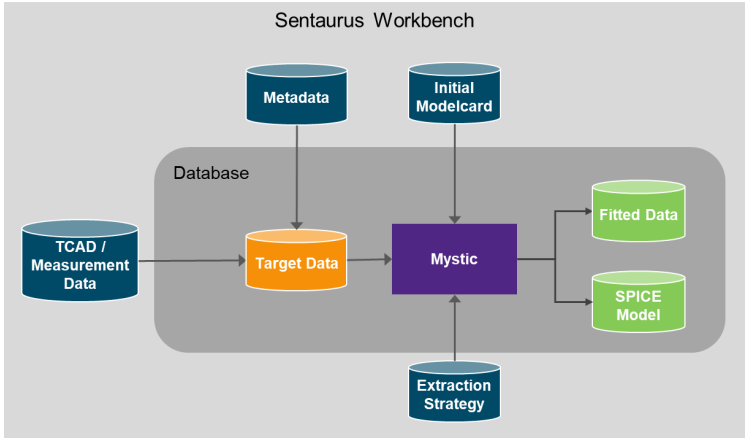
- Gate lengths: 20nm-500nm for Gate Width=1um
- Gate Widths: 120-500nm for Gate Length=20nm
- Vd=0.01/1.0/1.5/1.8V at Vb=0 for various Transfer Characteristics
- Vg=1.0/1.4/1.8V at Vb=0 for various Output Characteristics
- High and low Drain for Vb=0.5/1/1.5/2 on nFet device of L=0.5/W=1um

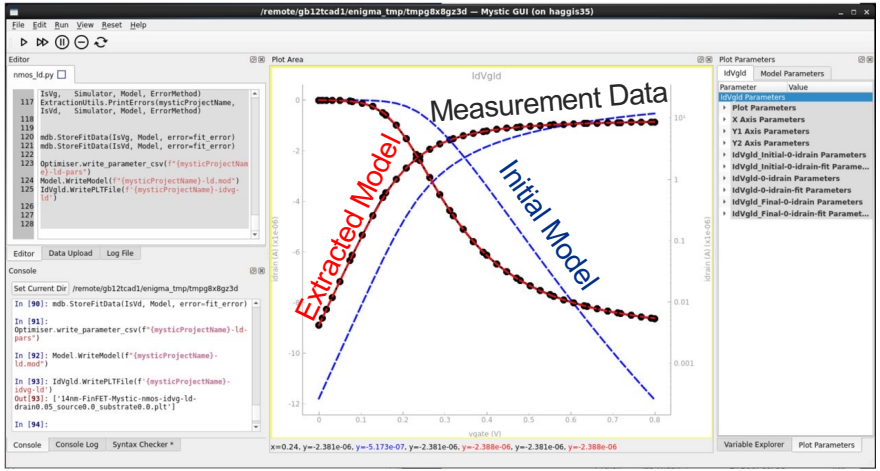
RVT Flavor:

- Gate lengths: 20nm-500nm for Gate Width=1um
- Vd=0.01/1.0/1.5/1.8V at Vb=0 for various Transfer Characteristics
- Vg=1.0/1.4/1.8V at Vb=0 for various Output Characteristics
- High and low Drain for Vb=0.5/1/1.5/2 on nFet device of L=0.5/W=1um

Mystic Software

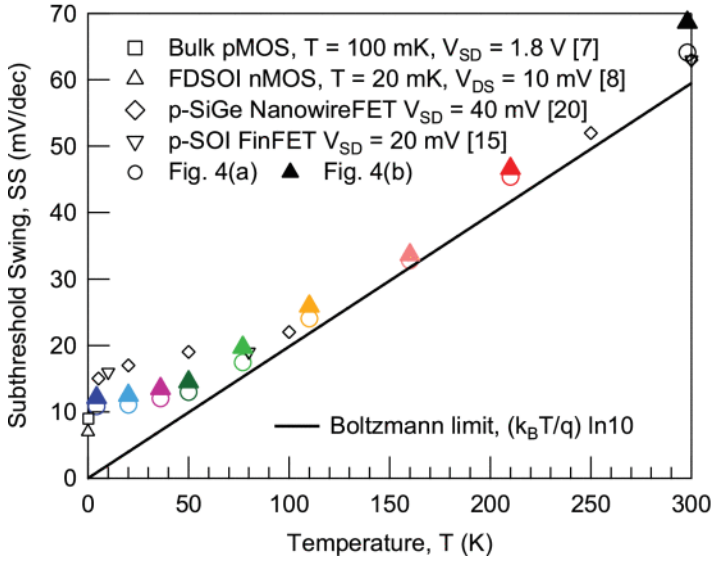
- Synopsys SPICE model extraction tool for creating **automated parameter extraction** methodologies Integrated in the Synopsys Sentaurus Workbench TCAD platform
- Use **Synopsys Primesim HSPICE** as circuit simulator
- Features an interactive GUI, a custom **Python scripting environment,** and an extensive **optimization library** for finding the best parameter set for the selected SPICE model





Our Model Approach

- Start with foundry PDK provided by GF --> **re-extract** the parameters we think will change at cryo
- Constrain the parameters to reasonable ranges based on physics expectations and literature when applicable
- **Isothermal** model at 3.8K
- Change the input pdk:
  - BSIM-IMG 102.8 doesn't include effects like subthreshold slope saturation [14][18] (but the latest **BSIM-IMG 102.9.6** does)
  - We model that by setting **temp** to the value where our **subthreshold slope saturates**
  - **Set temp = tnom** to remove temp dependent params
- Extracted values back into the PDK



Subthreshold Swing Saturation as a function of Temperature for various devices [18]

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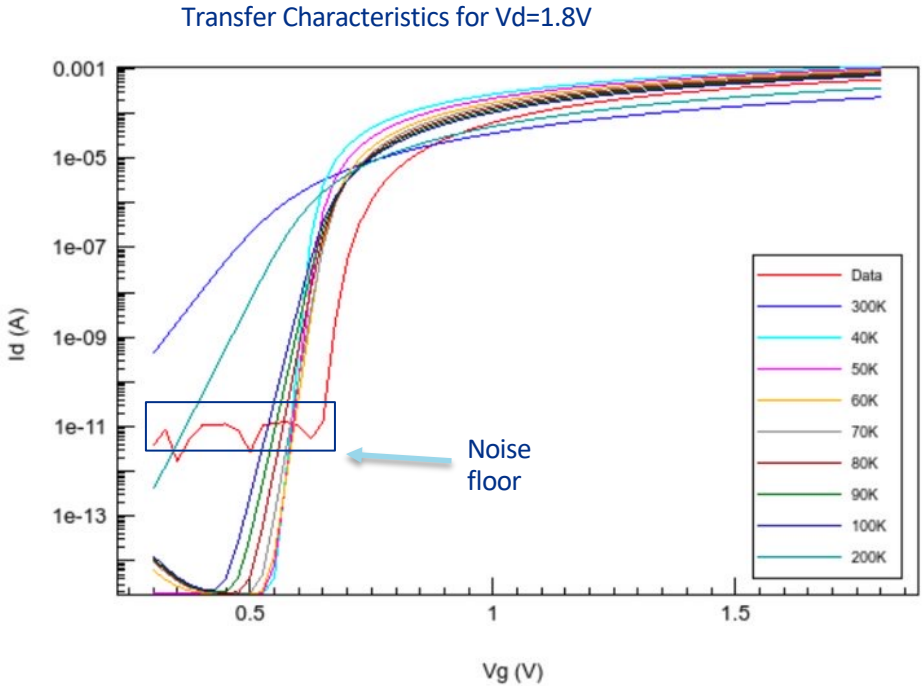
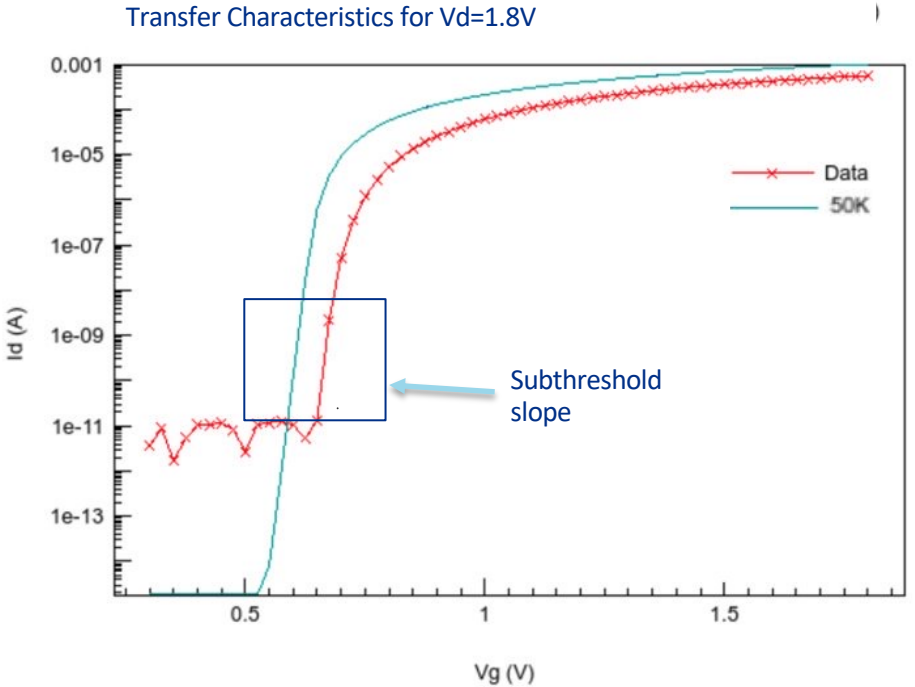
Setting TNOM Value

Adjust temp=tnom and find where the subthreshold slope best fits:





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Our Model Approach – PDK modification

- Typical PDK structure has both **HSPICE** and **Spectre** versions
  - We have modified the PDK in both versions

- PDK model parameter values usually have **values defined in libraries hidden** in layers in the PDK
  - For example, the BSIM mobility parameter u0 could look something like (I made this up, not from actual PDK):

    u0 = u0_ext(del_0*c_u0 + 0.003) + m_u0

    Where every variable pulls from a web of various hidden libraries

    (this applies different values for corners, mismatch, capacitance, etc)

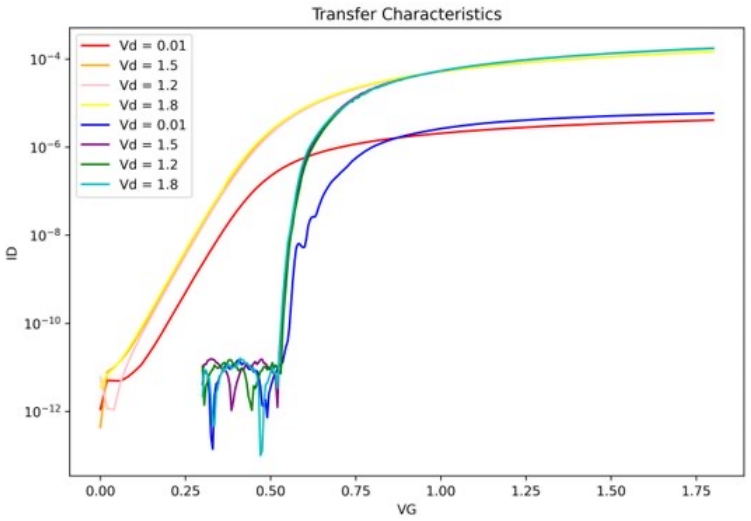
- We **multiply the nominal parts** of the target model params by a scaling factor "param_nom = 1"
- **Adjust the "_nom" variables** until a fit is found (and set boundaries based on physics still, but rather than the whole parameter value, we calculate the allowed limits for the scaling factor)

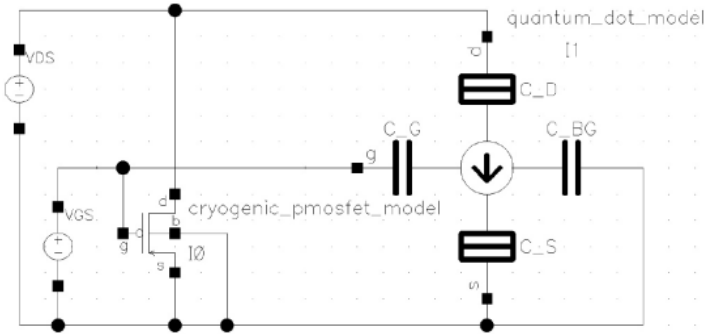
Subthreshold Current Jumps

Some short channel lengths show this effect in our measurement data

This is caused by resonant tunneling via the ionized dopant [15] [16] [19]

These effects are not modeled for the time being, but can be modeled via Verilog wrappers (see S. Tripathi paper)





Tripathi, S. Pati, et al. "Characterization and modeling of quantum dot behavior in FDSOI devices." *IEEE Journal of the Electron Devices Society* 10 (2022): 600-610.

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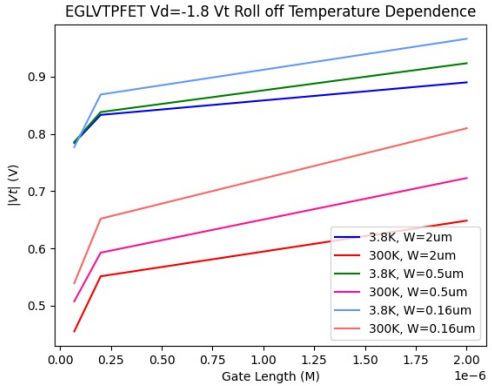
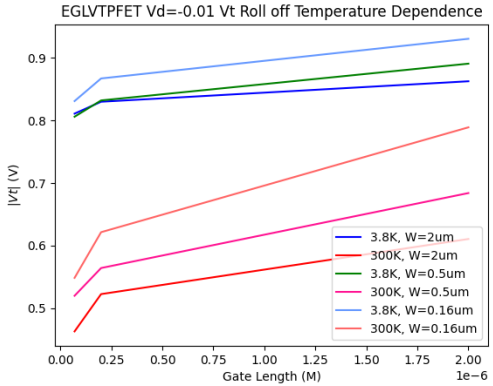
Behavior Changes at Cryogenic Temperatures

- Electron Mobility [2]
- Phonon scattering, coulomb scattering [3]
- Capacitance effects [4]
- Resistance due to self-heating [5]
- Source drain extension resistance [6]
- Velocity saturation [7][8]
- Work function [7][9]
- Subthreshold slope [10]
- Drain induced barrier lowering [11]
- …etc

Threshold Voltage Expectation at Cryogenic Temperatures

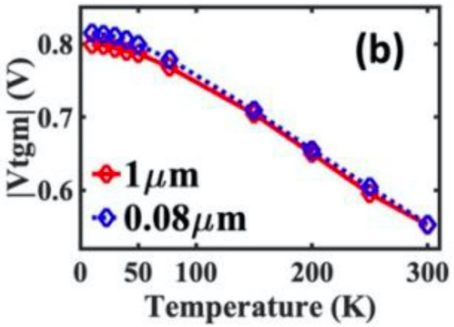
- Increase in Vt as temperature decreases seen in 28nm FDSOI [12]
- Our 22nm FDSOI data reflects this trend, with an average





Used **fixed current criteria** rather than GmMax to get a smoother roll off across geometries (GmMax method in backup slides)

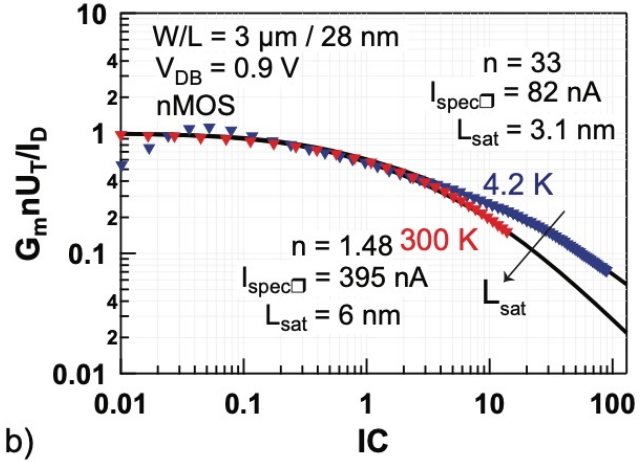
High drain roll-off usually shows a **bigger difference in Vt because of DIBL**, at cryo we want Vt geometry dependence to be **more linear,** which is seen in the rightmost plot



|Vt| vs temperature at Vds=50mV using maximum transconductance method for a 28nm FDSOI pmos device at Vb=0, taken from [12]

Velocity Saturation Expectation at Cryogenic Temperatures

Decrease in impact of velocity saturation seen in 28nm FDSOI [7][8]



b) Normalized transconductance efficiency versus the inversion coefficient for nMOS W/L = 3 µm / 28 nm, showing a decreased velocity saturation effect at 4.2 K. [7]

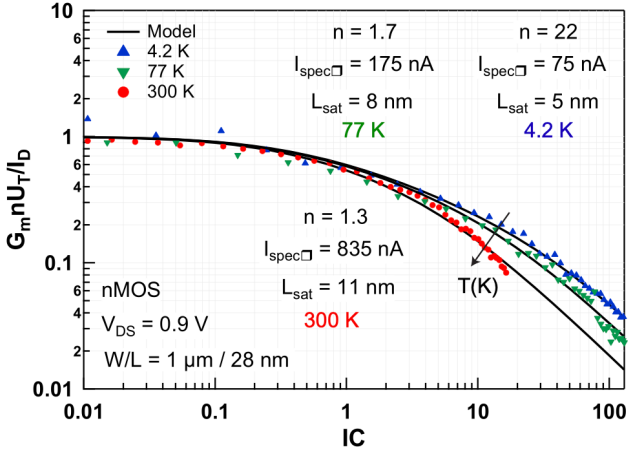


Figure 10: Modeling the normalized transconductance efficiency at 300, 77, and 4.2 K in a short 28-nm FDSOI nMOS in saturation. Model parameters are given in the figure. [8]

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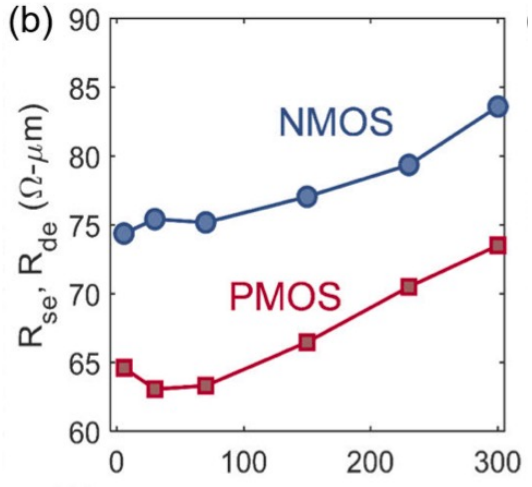
Source/Drain Resistance Expectation at Cryogenic Temperatures

- In 22nm FDSOI a **11-15% decrease** seen in S/D resistance [13]

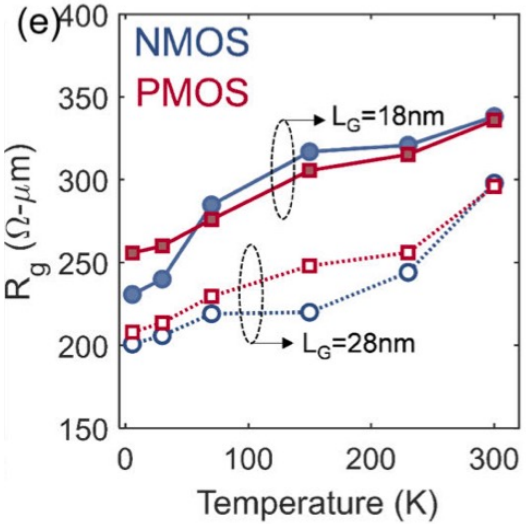
- Improvement in gate resistance:
  - **Prwg** models gate dependence of S/D resistance in BSIM 102.9.6, and as it **increases, overall resistance should decrease** (Our models reflect this)

$$R_{source} = \frac{1}{W_{new}^{WR} \cdot NF} \cdot \left(RSWMIN(T) + \frac{RSW(T)}{1 + PRWG \cdot V_{gs,eff}} \right) + R_{s,geo}$$

$$R_{drain} = \frac{1}{W_{new}^{WR} \cdot NF} \cdot \left(RDWMIN(T) + \frac{RDW(T)}{1 + PRWG \cdot V_{gd,eff}} \right) + R_{d,geo}$$



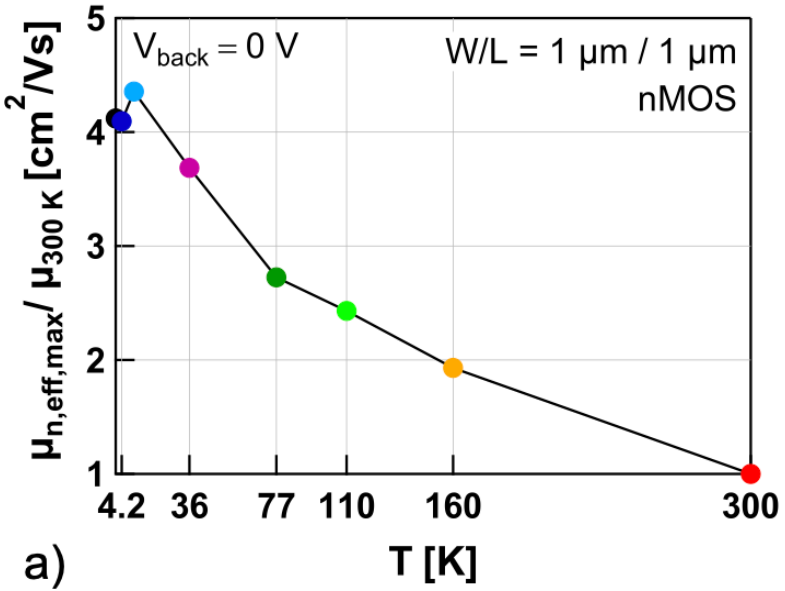
Source/drain series resistance (*R*se, *R*de) improve by 15% at 5.5 K [13]



Reduced resistivity of gate metal contact (NiSi) and poly-Si cause gate resistance (*R*ge) reduction at cryogenic temperature. [13]

Mobility Expectation at Cryogenic Temperatures

- Effective mobility is made of three main components:
  - Lattice vibration-induced scattering
  - Scattering on impurities (Coulomb and phonon scattering)
  - Surface Roughness Scattering
- At cryogenic temperatures Coulomb Scattering becomes more dominant increasing mobility [2]



Effective Mobility Temperature dependence in 28nm FDSOI [3]

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BSIM-IMG Recommended Strategy as a Basis

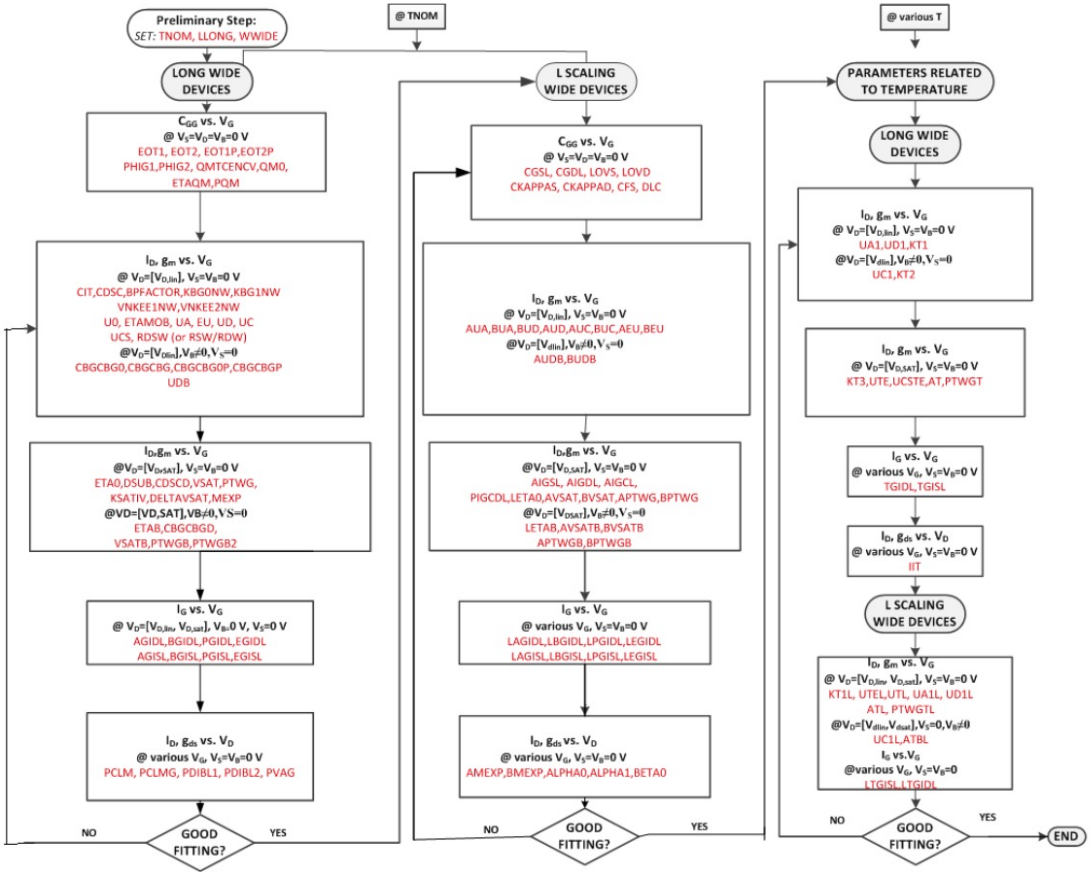

Figure 13: Parameters Extraction Procedure in BSIM-IMG Model.

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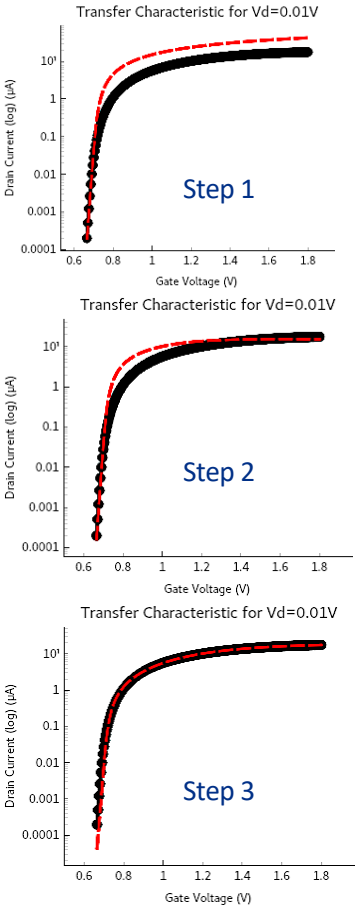
Building an Extraction Strategy

- **Stages:** Contain *groups of isolated parameters* that mainly influence each other
  - **Steps:** Subgroups of parameters that impact v*arious target regions* of the curves within each stage
  - **Loop:** *Repeat Steps* until a good fit is reached

Example: Stage 1
(u0,ua,ud,rdw, rsw, cit, phig1) impact Low Drain Bias curve

Step 1: (phig1, cit) fit to subthreshold region
Step 2: (u0,ua,ud) fit to Ion region
Step 3: (rdw, rsw) fit to threshold voltage region

Loop steps 1-3 until a good fit requirement is met



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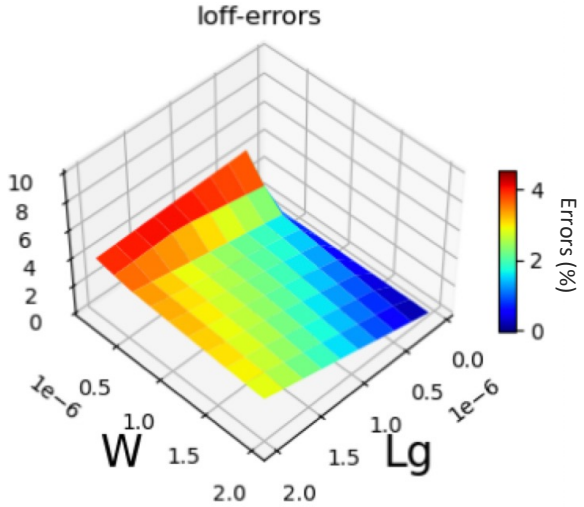
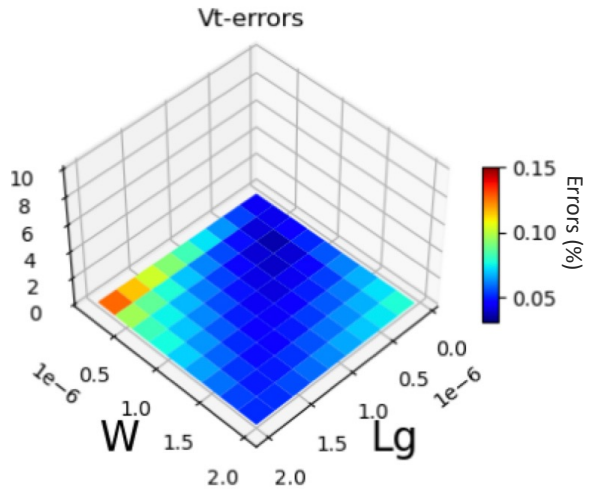
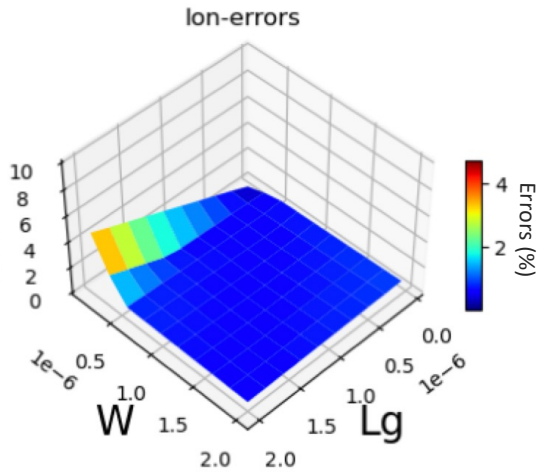
Errors across Figures of Merit for all Lengths and Widths (EG Devices)

Found by taking the percentage error between data simulated using the extracted model and the measurement data (for transfer characteristics):







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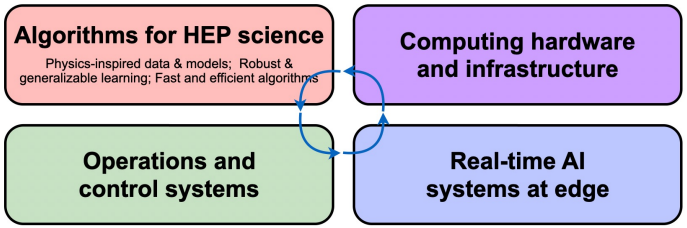
AI/ML Modelling for Extreme Environmen

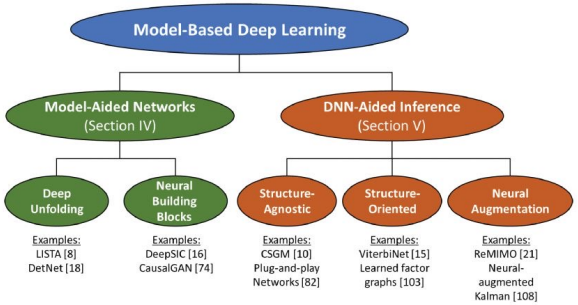
Fermilab has expertise with AI across a wide array of tasks and methods

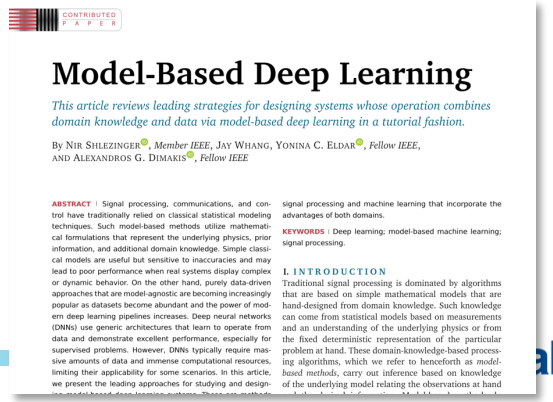
- Develop robust models, adaptable across domains (temperatures)

With are currently considering 3 scenarios:

1. PDK compatible SPICE models using AI/ML extracted parameter values
   - Use AI/ML to enhance specialized tools, ameliorate difficulties for modelling engineers, rapidly develop models for extreme environments
2. Make a data driven model that bypasses compact models all together
   - This is where most of the work in AI/ML based transistor modeling has been done
3. Collaborate with Synopsys to integrate AI/ML in their tools. Expertise with AI across a wide array of tasks and methods







CONTRIBUTED PAPER

Model-Based Deep Learning

This article reviews leading strategies for designing systems whose operation combines domain knowledge and data via model-based deep learning in a tutorial fashion.

By Nir Shlezinger, *Member IEEE*, Jay Whang, Yonina C. Eldar, *Fellow IEEE*, and Alexandros G. Dimakis, *Fellow IEEE*

ABSTRACT | Signal processing, communications, and control have traditionally relied on classical statistical modeling techniques. Such model-based methods utilize mathematical formulations that represent the underlying physics, prior information, and additional domain knowledge. Simple classical models are useful but sensitive to inaccuracies and may lead to poor performance when real systems display complex or dynamic behavior. On the other hand, purely data-driven approaches that are model-agnostic are becoming increasingly popular as datasets become abundant and the power of modern deep learning pipelines increases. Deep neural networks (DNNs) use generic architectures that learn to operate from data and demonstrate excellent performance, especially for supervised problems. However, DNNs typically require massive amounts of data and immense computational resources, limiting their applicability for some scenarios. In this article, we present the leading approaches for studying and design-

signal processing and machine learning that incorporate the advantages of both domains.

KEYWORDS | Deep learning; model-based machine learning; signal processing.

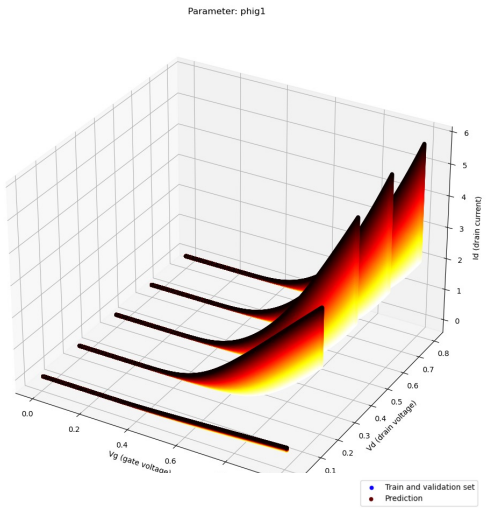
I. Introduction

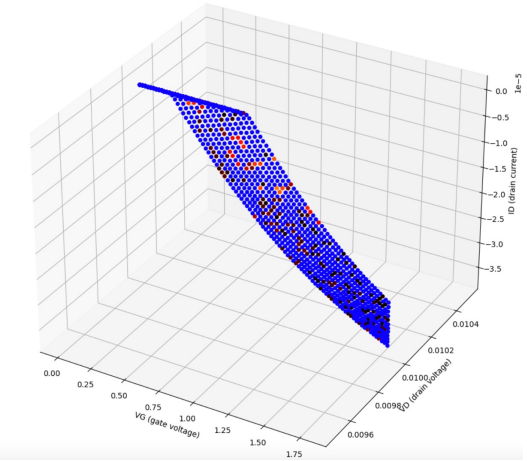
Traditional signal processing is dominated by algorithms that are based on simple mathematical models that are hand-designed from domain knowledge. Such knowledge can come from statistical models based on measurements and an understanding of the underlying physics or from the fixed deterministic representation of the particular problem at hand. These domain-knowledge-based processing algorithms, which we refer to henceforth as *model-based methods*, carry out inference based on knowledge of the underlying model relating the observations at hand

In House ML Algorithm for Cryo-Modeling (In Progress)

Goal: Find optimal value of parameters using machine Learning

- **Inputs:** Drain current that is dependent on gate length (L), width (W), gate voltage (Vg), drain voltage (Vd), and a 45 count parameter set (P)
  - Id = f(L,W,Vg,Vd,P)
- **Outputs:** Optimal values for all 45 parameters that can simulate data using HSPICE as close as possible to the actual measurement data values
- Training the impact of changing a model parameter on drain current. Cadence simulated data from PDK model at 50K
- Starting algorithm that predicts one parameter to the accuracy needed





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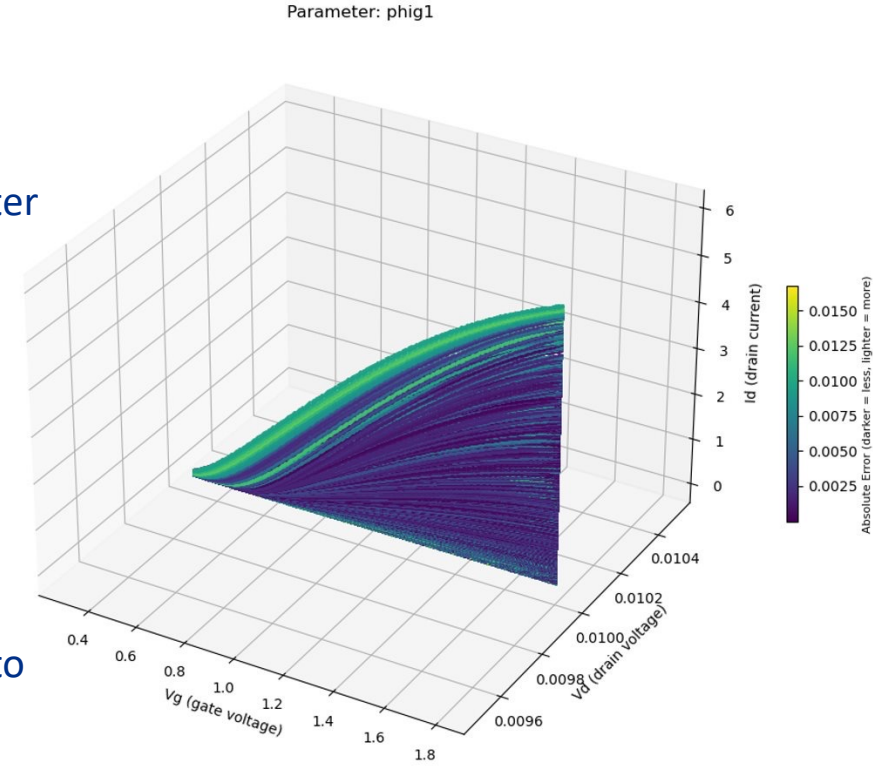
In House ML Algorithm for Cryo-Modeling (In Progress)

ML/AI for Accessible and Efficient PDK development:

Current Status: Developing the algorithm on a 10 parameter subset

Best Result for Single Parameter Estimation: Achieved a Mean Squared error of 0.00002, meeting the accuracy required for our initial test parameter (shown on the right)

Goal: A fully Cadence integrable, open source, model extraction framework, to offer an easier/accessible route to compact model extraction to the community



test_loss	train_loss	train_dropout_rate	train_early_stop_patience	train_batch_size	train_val_split	lr_initial	lr_decay_step	lr_decay_rate	lr_stair_case
0.000027	mean_squared_error	0.000000	50	16	0.200000	0.001000	100	0.960000	False

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Future work

- Develop 4K static **timing libraries** for standard cell library
- Cryogenic **noise measurements**
- **AI/ML** modeling and extraction for cryo-PDK development for extreme environment
- Develop cryo-PDK for **GF 28HV, GF 55BCD, GF 45 SPCLO, GF 9HP**, collaborate with DRD on cryo-PDK for **TSMC 28**

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Works Cited

[1] Lotfi, Nima, et al. “A single-channel 18.5 GS/s 5-bit flash ADC using a body-biased comparator architecture in 22nm FD-soi.” *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019, https://doi.org/10.1109/iscas.2019.8702505.
"A Single-Channel 18.5 GS/s 5-bit Flash ADC using a Body-Biased Comparator Architecture in 22nm FD-SOI""
[2] Tang, Zhidong, et al. “Cryogenic CMOS RF device modeling for Scalable Quantum Computer Design.” *IEEE Journal of the Electron Devices Society*, vol. 10, 2022, pp. 532–539, https://doi.org/10.1109/jeds.2022.3186979.
[3] Beckers, Arnout, Farzan Jazaeri, Heorhii Bohuslavskyi, et al. “Characterization and modeling of 28-NM FDSOI CMOS technology down to cryogenic temperatures.” *Solid-State Electronics*, vol. 159, 2019, pp. 106–115, https://doi.org/10.1016/j.sse.2019.03.033.
[4] Inaba, Takumi, et al. “Importance of source and drain extension design in cryogenic MOSFET operation: Causes of unexpected threshold voltage increases.” *Applied Physics Express*, vol. 15, no. 8, 2022, p. 084004, https://doi.org/10.35848/1882-0786/ac819b.
[5] Hart, P. A. ’t, Babaie, M., Vladimirescu, A., & Sebastiano, F. (2021, June 15). *Characterization and modeling of self-heating in nanometer bulk-CMOS at cryogenic temperatures*. arXiv.org. https://arxiv.org/abs/2106.07982
[6] Importance of source and drain extension design in ... - iopscience. (n.d.-a). https://iopscience.iop.org/article/10.35848/1882-0786/ac819b
[7] Beckers, Arnout, et al. “Cryogenic characterization of 28 nm bulk CMOS technology for quantum computing.” *2017 47th European Solid-State Device Research Conference (ESSDERC)*, 2017, https://doi.org/10.1109/essderc.2017.8066592.
[8]Author links open overlay panelArnout Beckers a, et al. “Characterization and Modeling of 28-NM FDSOI CMOS Technology down to Cryogenic Temperatures.” *Solid-State Electronics*, Pergamon, 21 Mar. 2019, www.sciencedirect.com/science/article/pii/S0038110119301443.
[9] Beckers, Arnout, Farzan Jazaeri, and Christian Enz. “Cryogenic mos transistor model.” *IEEE Transactions on Electron Devices*, vol. 65, no. 9, 2018, pp. 3617–3625, https://doi.org/10.1109/ted.2018.2854701.
[10] Bohuslavskyi, H., et al. “Cryogenic subthreshold swing saturation in FD-soi mosfets described with band broadening.” *IEEE Electron Device Letters*, vol. 40, no. 5, 2019, pp. 784–787, https://doi.org/10.1109/led.2019.2903111.
[11] Chen, Zehua, et al. “Temperature dependences of threshold voltage and drain-induced barrier lowering in 60NM gate length MOS transistors.” *Microelectronics Reliability*, vol. 54, no. 6–7, 2014, pp. 1109–1114, https://doi.org/10.1016/j.microrel.2013.12.005.
[12] Bhardwaj, Anuj, et al. “Narrow-width effects in 28-nm FD-SOI transistors operating at cryogenic temperatures.” *IEEE Journal of the Electron Devices Society*, vol. 11, 2023, pp. 22–29, https://doi.org/10.1109/jeds.2022.3233302.
[13] Chakraborty, Wriddhi, et al. “Characterization and modeling of 22 nm FDSOI Cryogenic RF CMOS.” *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 7, no. 2, 2021, pp. 184–192, https://doi.org/10.1109/jxcdc.2021.3131144.
[14] G. Pahwa, P. Kushwaha, A. Dasgupta, S. Salahuddin, and C. Hu, “Compact modeling of temperature effects in fdsoi and finfet devices down to cryogenic temperatures,” *IEEE*, 2021.
[15] Han, Hung-Chi, et al. “Analytical modeling of source-to-drain tunneling current down to cryogenic temperatures.” *IEEE Electron Device Letters*, vol. 44, no. 5, 2023, pp. 717–720, https://doi.org/10.1109/led.2023.3254592.
[16] Tripathi, S. Pati, et al. "Characterization and modeling of quantum dot behavior in FDSOI devices." *IEEE Journal of the Electron Devices Society* 10 (2022): 600-610 https://doi.org/10.1109/JEDS.2022.3176205
[17] Braga, Davide, Shaorui Li, and Farah Fahim. "Cryogenic electronics development for high-energy physics: An overview of design considerations, benefits, and unique challenges." *IEEE Solid-State Circuits Magazine* 13.2 (2021): 36-45. https://doi.org/10.1109/MSSC.2021.3072804
[18] A. Beckers, F. Jazaeri and C. Enz, "Theoretical Limit of Low Temperature Subthreshold Swing in Field-Effect Transistors," in IEEE Electron Device Letters, vol. 41, no. 2, pp. 276-279, Feb. 2020, doi: 10.1109/LED.2019.2963379.
[19] H. -C. Han, Z. Zhao, S. Lehmann, E. Charbon and C. Enz, "Analytical Modeling of Cryogenic Subthreshold Currents in 22-nm FDSOI Technology," in IEEE Electron Device Letters, vol. 45, no. 1, pp. 92-95, Jan. 2024, doi: 10.1109/LED.2023.3331022.