



## Verification and VIP

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HEPIC

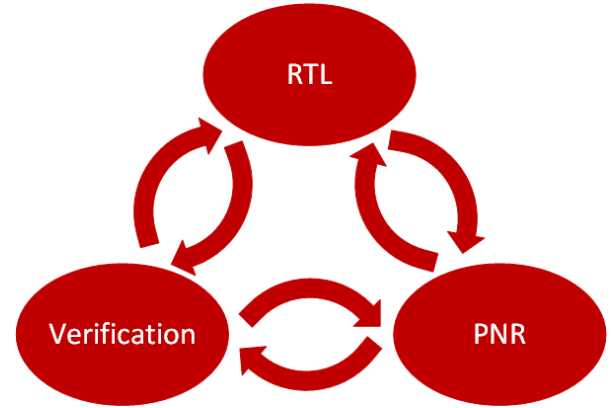
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# Our first and biggest problem (at least from my perspective...)

- According to industry statistics the effort that goes into verification averages to around 70%
- That means that RTL and PNR **COMBINE** to 30%
- Most senior managers stare at you like a deer looking into the headlights when you explain to them that you cannot possibly have a “few simulations” done in a couple of weeks.  
(Directed Tests ≠ Verification)
- We must change the culture. This stuff takes time and **not just a little bit of time**. Verification takes more than twice as much time as everything else combined. We need to **budget** for that, and we need to **schedule** for that.

# Why does it take so much time and effort?

- Verification is a systematic approach to pre-silicon chip testing
- Randomization is constrained by the expectations of the system.
- EVERYTHING is randomized.
- Hundreds of thousands of tests are run
- Each test contributes to coverage
- Verification concludes when coverage is complete (**possibly...maybe...sort of**)



**RTL**

## Coverage

- Toggle Coverage – Design activity; Did a particular bit flip?
- Code Coverage – How much of your RTL Code was tested?
- Functional Coverage – What features were tested?

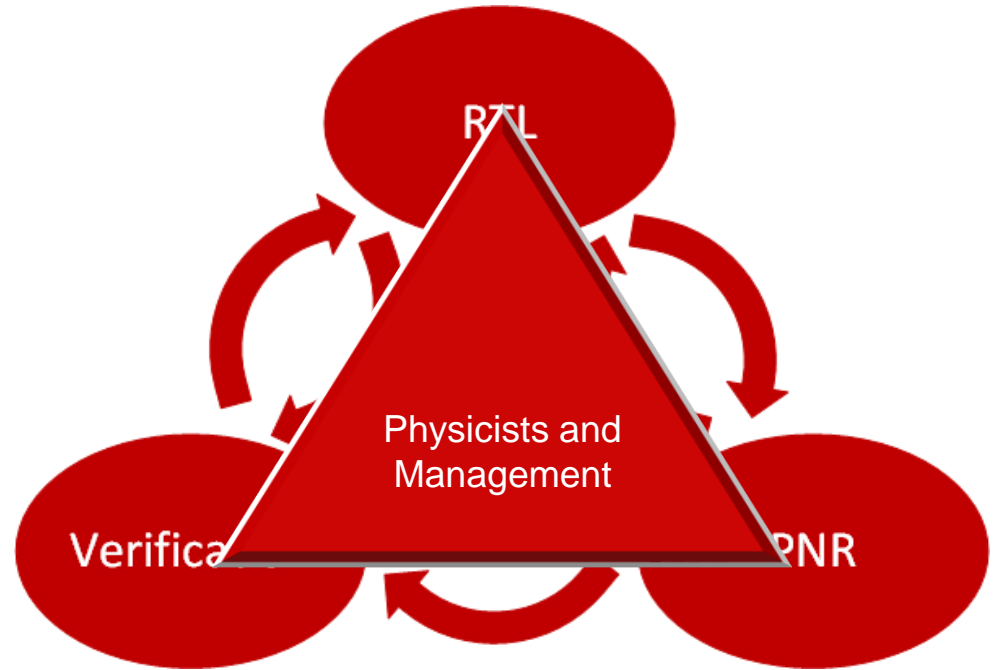
## Constrained Randomization

- Setup Randomization – Number of inputs/outputs
- State Randomization – Start at power up? Start at steady state?
- Data Randomization – Packet contents, etc.
- Upset Randomization – Noise, Radiation, etc.

# Who's involved? Everyone

## How often? Weekly...daily...Hourly

- If you think that you can hand the verification job off to a group of sun-starved cave-dwellers who just happened to like verification, you are grossly mistaken.
- We need detailed specifications on the design, **but don't give us the code!**
- We need regular feedback especially on what qualifies as a failure.



# What are our options in Verification?

- **SystemVerilog out-of-the-box class-based verification**
  - Reuse is poor
  - Development quick (maybe)
- **COCOTB**
  - Reuse is not good, but it isn't bad, either.
  - Coverage metrics are a work-in-progress
  - Development quicker than other methods
  - Easy to drag physics graduate students into the project because they know Python
- **UVM**
  - Industry standard
  - Reuse is good (if you work at it)
  - Coverage is the best there is and EDA tools know how to work with it

## Any other options?

- The dark horse is formal verification
- **Formal Verification** - the act of proving or disproving the correctness of intended algorithms underlying a system with respect to a certain formal specification or property, using formal methods of mathematics
- SEU injection framework for radiation-tolerant ASICs, a formal verification approach
  - Journal of Instrumentation
  - 2023-02-01 | Journal article
  - DOI: 10.1088/1748-0221/18/02/c02023
  - Part of ISSN: 1748-0221
  - CONTRIBUTORS: M. Lupi; A. Pulli

# Reuse?

- Why do we care?

Verification is difficult and time-consuming. Consequently, any time that I can reuse some of your verification code, that is one less piece of code that I must make! That's all to the good, and that's really all the VIP is.

However, to make it work well, VIP requires an almost

**SLAVISH OBSESSION WITH STANDARDS.**

# VIP

- **All VIP must look alike**: They must use the same lintable coding standards.
- **All VIP must act alike**: use the same primary function names, use the same primary configuration variable names, etc. In this way, new users know how to pick them up and place them in their code.
- **All VIP must be well documented**: ESPECIALLY WITHIN THE CODE ITSELF!!! Independent documentation should include timing diagrams (where appropriate) and code examples.
- **All VIP must be “self-standing”**: They should be contained within their own package and include any required constants.



# VIP

- We need a GitHub or GitLab repository for the HEPIC VIP
- It should be fully compatible with VIP used by the CHIPS Group at CERN because we ALL work on both American and European projects. If American VIP is incompatible with European VIP, in the long run, it will not do us a lot of good.
- We should have an understanding about “credit” for developing VIP – co-authorship on papers or acknowledgement in papers or whatever. It just needs to be understood in advance. We might also want to consider some kind of publishing option so that VIP developers get some kind of publishing credit for their efforts.
- Finally, some group of people must be responsible for all this effort.

## One last thing...

- The Fermilab Digital Group just finished a major, 5+ year UVM effort in both the DUNE Cold chips (COLDADC and COLDATA) and CMS ECON chips (ECON-T and ECON-D).
- We have one principal, one senior and one junior engineer with significant UVM experience
- Our COCOTB skills are on the rise
- We have time now if you need verification assistance. Send an email or contact me some other way.
  - Jim Hoff ([jimhoff@fnal.gov](mailto:jimhoff@fnal.gov))
  - Jim Hirschauer ([jhirsch@fnal.gov](mailto:jhirsch@fnal.gov))
  - Farah Fahim ([farah@fnal.gov](mailto:farah@fnal.gov))