Training Program

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Why A HEPIC Design Apprenticeship Program?

Two questions:

- Why does HEP need ICs
  - I think that is easy for those at this conference
- Why do we need a Design Apprenticeship program
  - In 2021 interest in chip design was in decline

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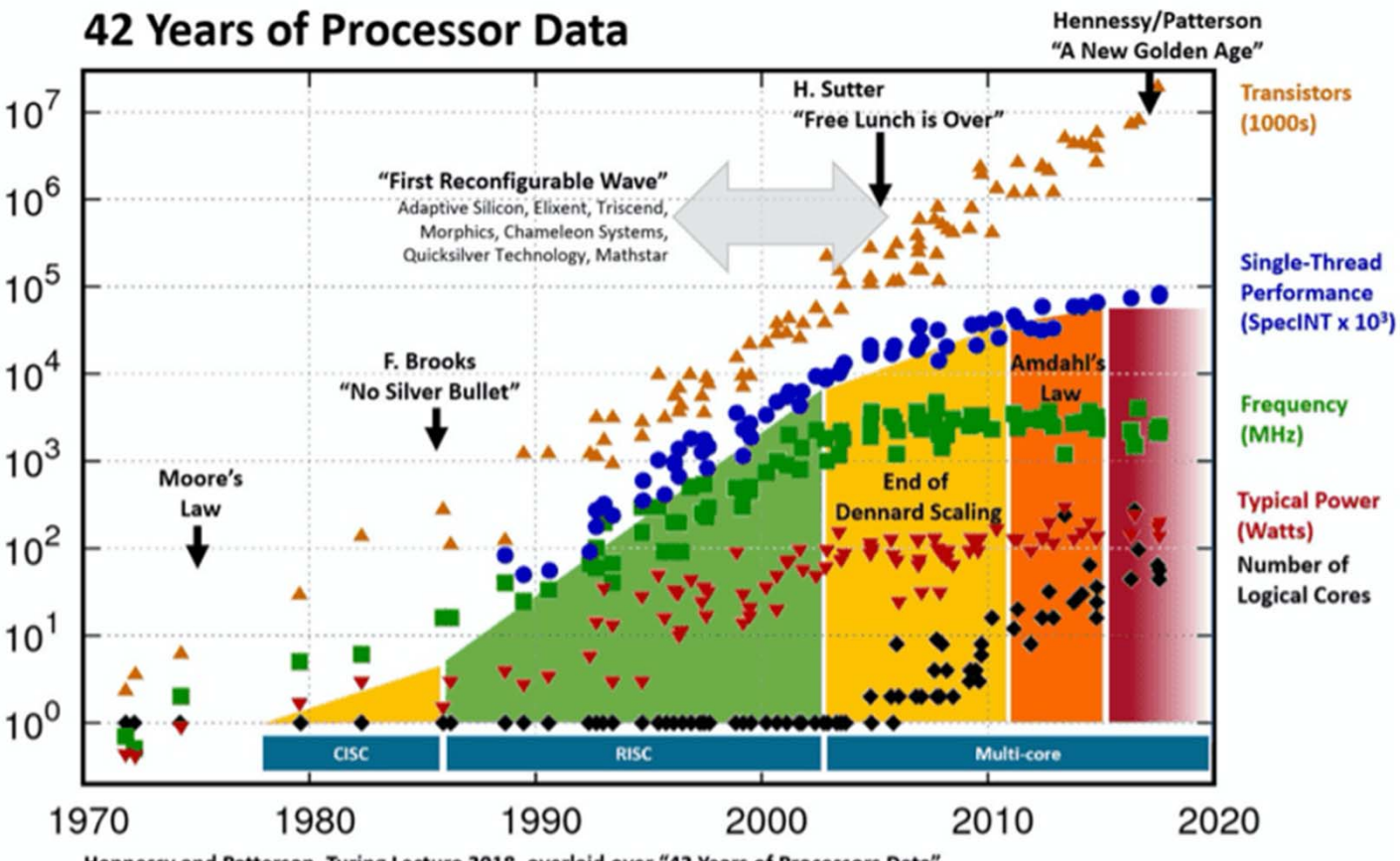
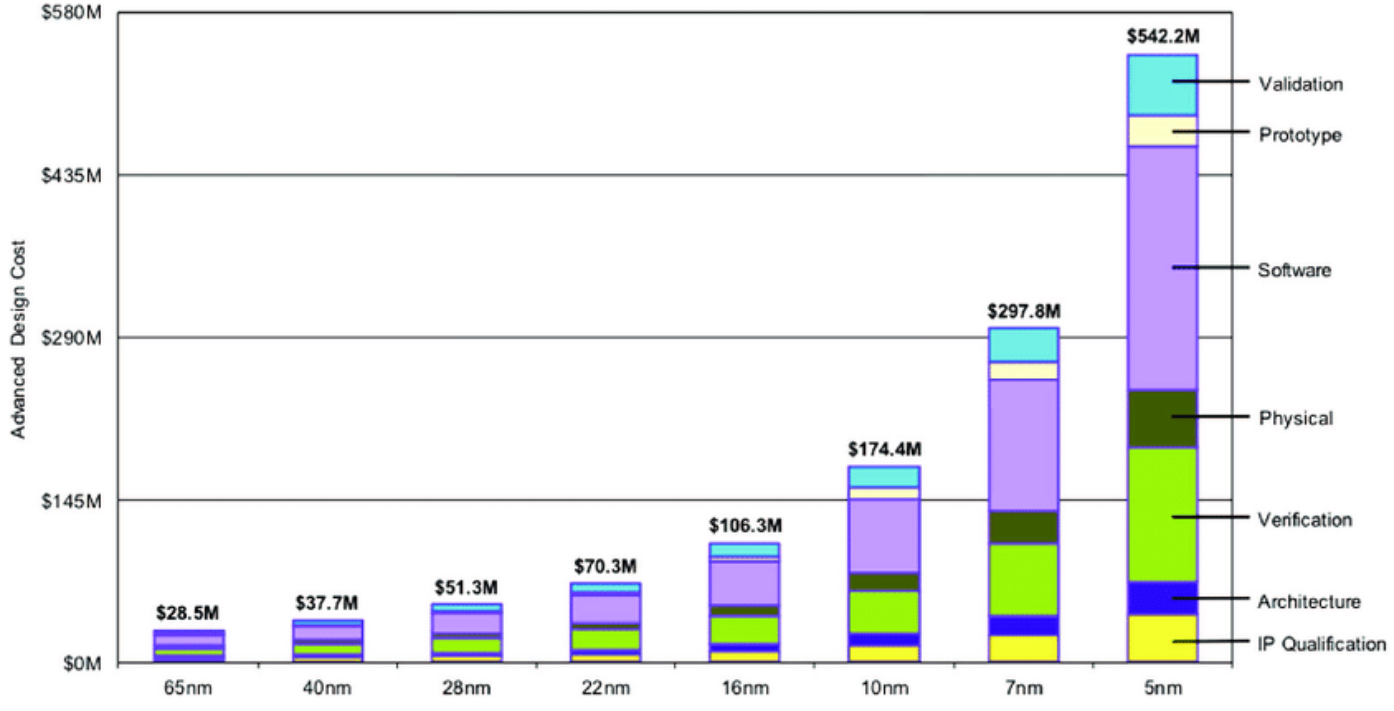
We Are Burdened By Our Own Success



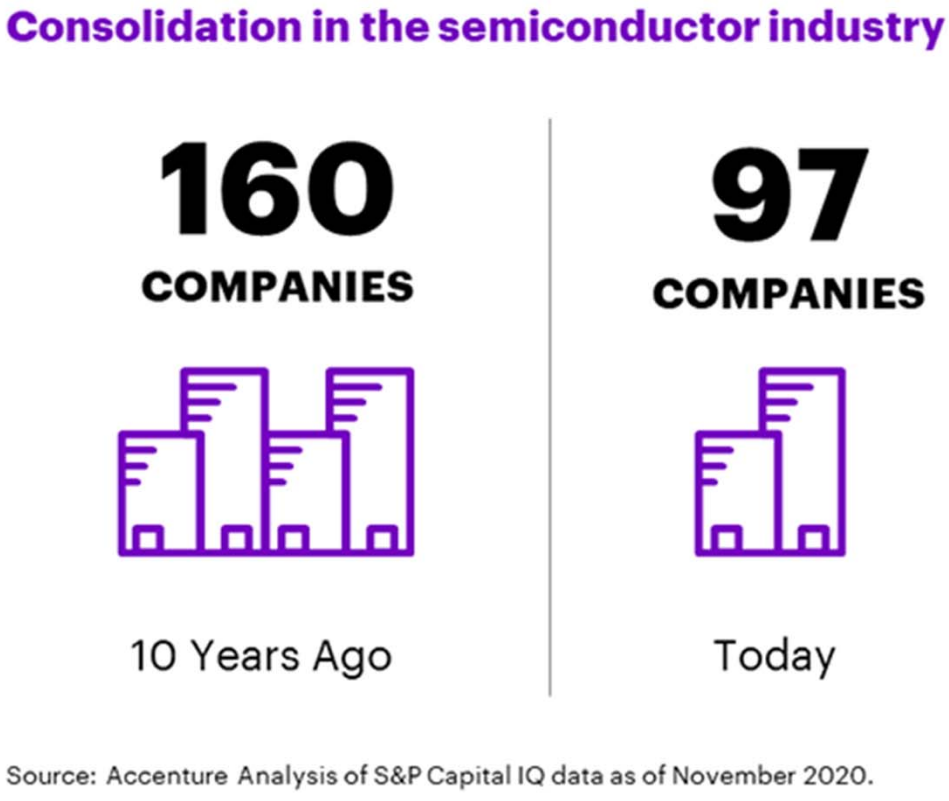
Hennessy and Patterson, Turing Lecture 2018, overlaid over "42 Years of Processors Data"
https://www.karlrupp.net/2018/02/42-years-of-microprocessor-trend-data/;"First Wave" added by Les Wilson, Frank Schirrmeister
Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2017 by K. Rupp

Complex Systems Are Expensive To Design

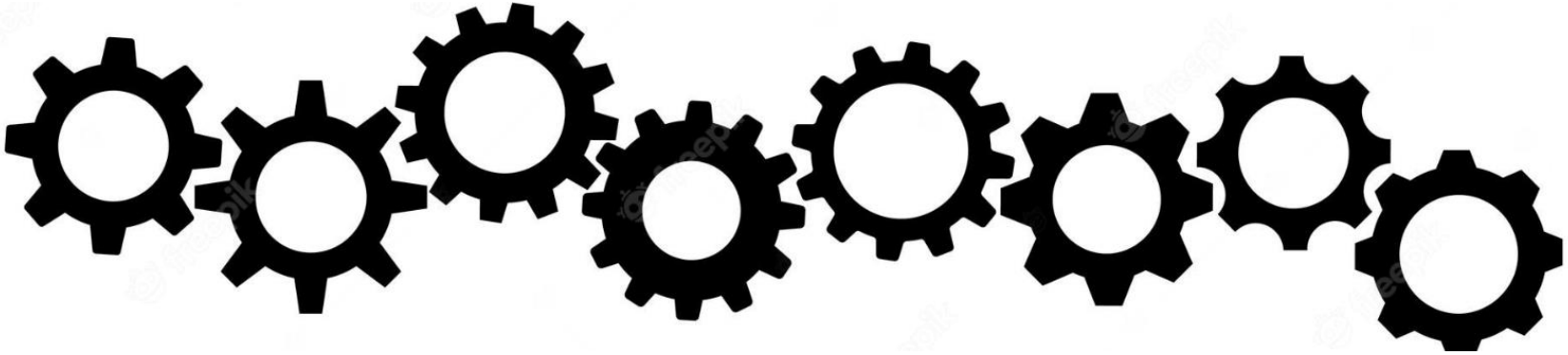


Chip Design and Manufacturing Cost under Different Process Nodes: Data Source from IBS

Leads To Industry Consolidation



And Lower Student Interest In Hardware



And those students interested in IC are snapped up by industry

Solve Two Problems w/ One Program

Using interesting HEP-IC design challenges at National Labs

- To generate interest in IC design
- To introduce students to opportunities in HEP-IC design

Three-Pronged Program

- University classes
- SLAC Summer school
- National Lab projects

Digital

CS107E
Computer Systems from the Ground Up
Chris Gregg

EE108
Digital System Design
Subhasish Mitra

EE180
Digital Systems Architecture
Christos Kozyrakis

EE282
Computer Systems Architecture
Caroline Trippel

EE271
Introduction to VLSI Systems
Priyanka Raina

CS357S
Formal Methods
Caroline Trippel

EE272
Design Projects in VLSI Systems I
Priyanka Raina

EE156/256
Board Level Design
Steve Clark

EE372
Tapeout Class
Design Projects in VLSI Systems II
Priyanka Raina

EE273
Digital Systems Engineering
Mark Horowitz

ENGR 40M
An Intro to Making
Tom Lee

Analog

EE101A
Circuits I
Eric Pop

EE101B
Circuits II
Tom Lee

EE292A
EDA & ML
Raul Camposano

EE207
Neuromorphics: Brains in Silicon
Kwabena Boahen

EE114 / EE214A
Fundamentals of Analog Integrated Circuit Design
Amin Arbabian

EE309A
Semiconductor Memory Devices and Circuit Design
Philip Wong, Priyanka Raina

EE214B
Advanced Integrated Circuit Design
Angelo Dragone

EE309B
Emerging Non-Volatile Memory Devices and Circuit Design
Philip Wong, Priyanka Raina

EE315
Analog-Digital Interface Circuits
TBD

EE314A
RF Integrated Circuit Design
Amin Arbabian

Stanford University

Prof. Amin Arbabian

EE114/214A: Fundamentals of Analog Integrated Circuit Design

Learning Goals:

Specific Analog Circuit Concepts:

CMOS transistor models, biasing, amplifier stages, frequency response, differential and multi-stage amplifiers, circuit non-idealities, feedback, noise, & stability

Intro to Design Methodology *:

- Abstraction
- Modeling
- Analysis
- **Design**
- Verification

* Applies more broadly than analog circuits

Example applications of analog circuits for sensor interfaces:

1) Neural interfaces

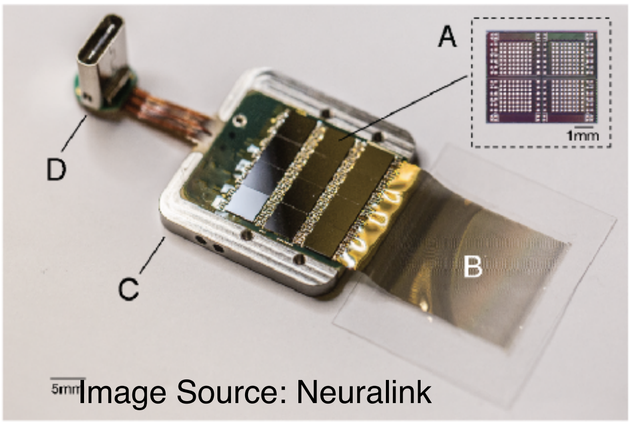


Image Source: Neuralink

2) LiDAR systems for self driving cars

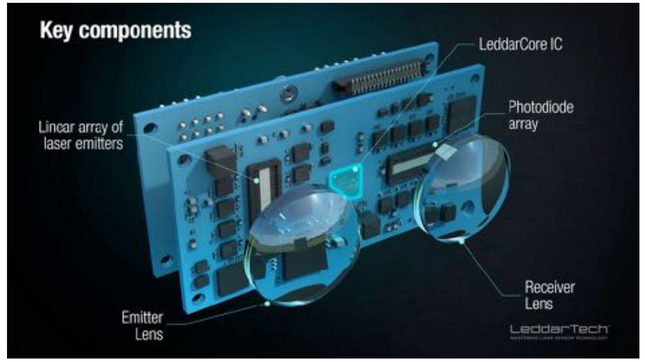
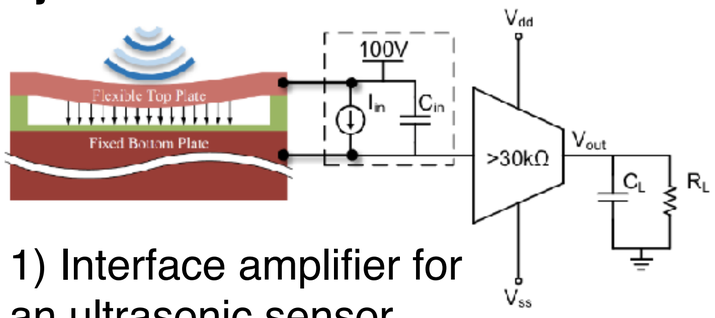
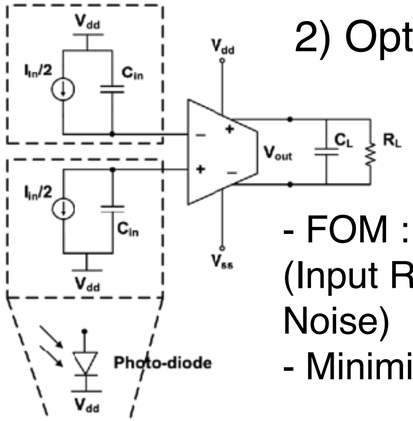


Image Source: LeddarTech Inc.

Example Design Projects:



1) Interface amplifier for an ultrasonic sensor

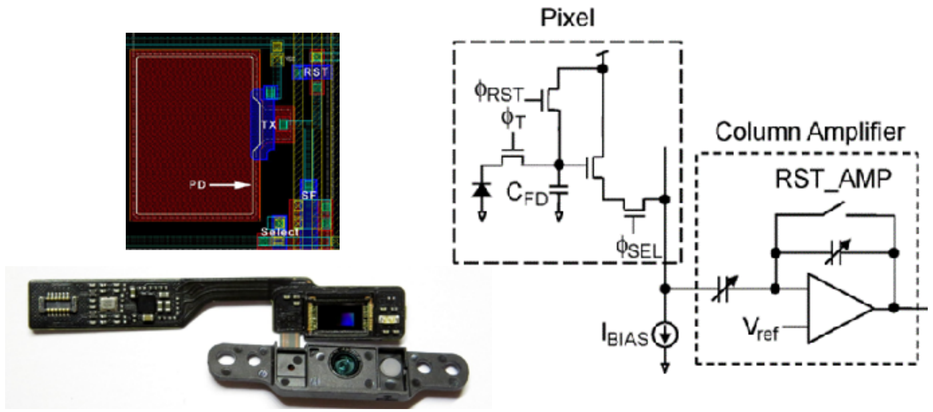


2) Optical sensor circuit

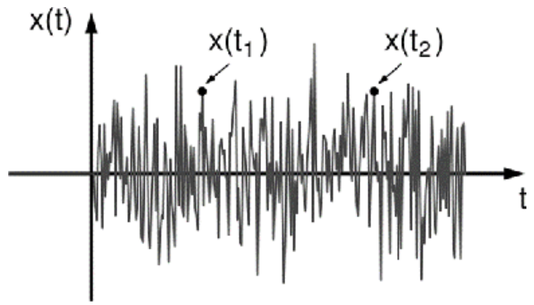
- FOM : (Gain x Bandwidth)/ (Input Referred Differential Noise)
- Minimize power consumption

Prof. Boris Murmann & Prof. Ahmed Sawaby

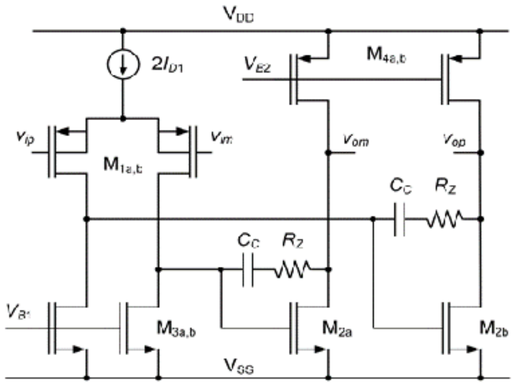
EE214B: Advanced Integrated Circuit Design



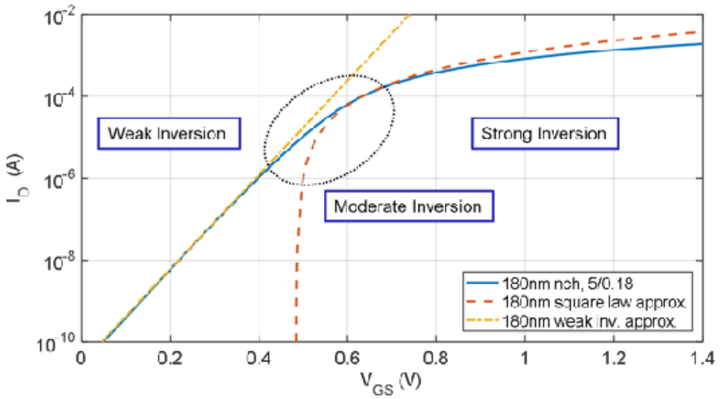
Driver Application: Image sensor



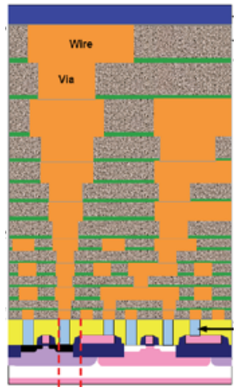
Noise analysis

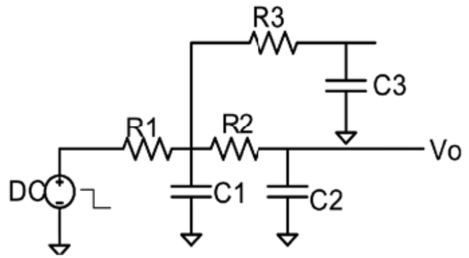


Amplifier design

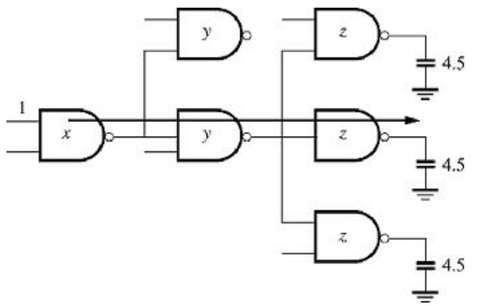


Transistor modeling





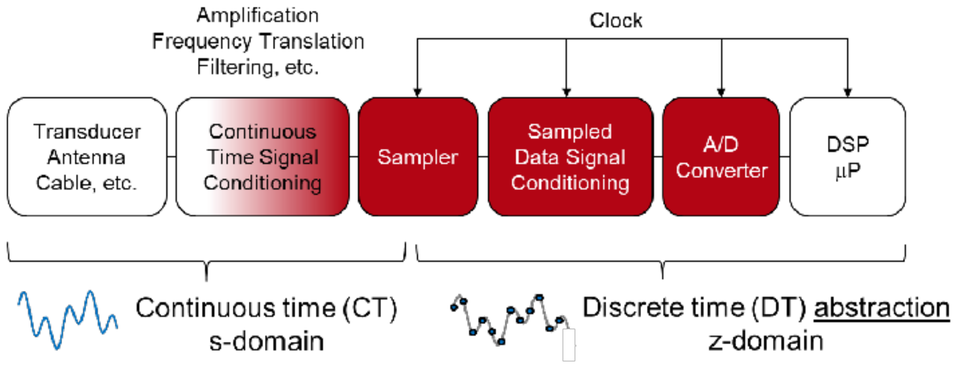
Interconnect modeling

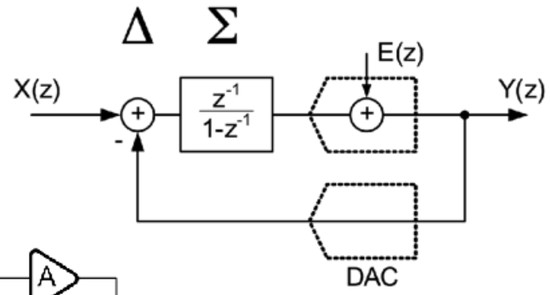


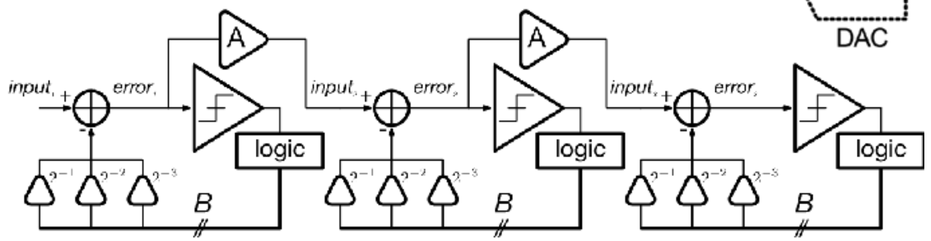
Gate sizing

Prof. Boris Murmann & Prof. Gift Nyikayaramba

EE315: Analog-Digital Interface Circuits

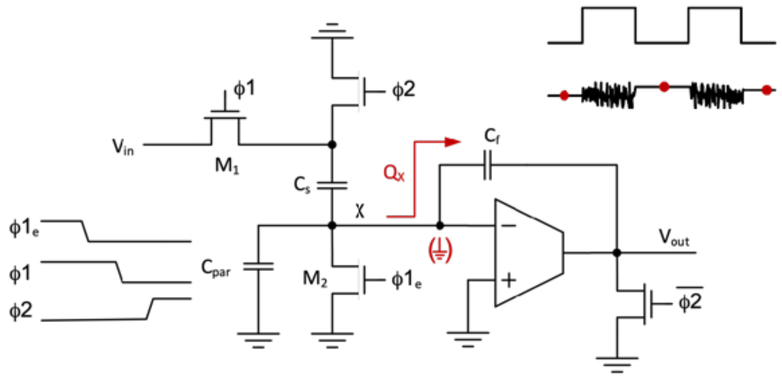


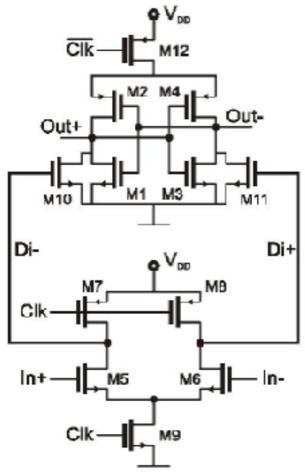


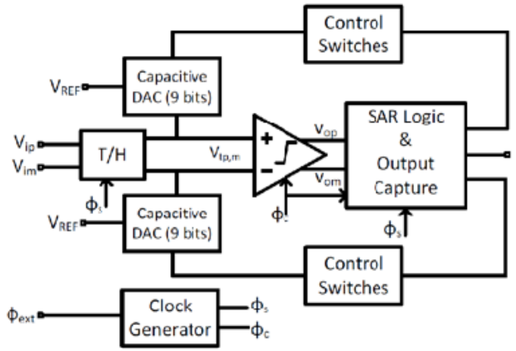


Modeling of A/D and D/A interfaces

A/D and D/A converters







Switched capacitor circuits, filters

Comparators

Project: SAR ADC

VLSI Design Course Sequence

Learn digital design fundamentals

Taken by 1st year PhD and MS students, and co-terms and seniors

Learn the full digital and analog EDA toolchain on an example project (DNN accelerator and PLL)

Write EE372 chip proposal

Use the toolchain to tape out your own chip

Teams of 2

Tapeout complete by end of Spring!

Test and measure your chip

HEPiC Summer Week

- Goals:
- **Aimed at graduate IC design students but open to others at a similar level. This summer week will cover High Energy Physics use cases and unique operating conditions, such as high radiation or deep cryogenic temperature.**
- Program:
- **A mix of lectures and practical design exercises:**
- **Students will attend lectures on HEP topics in the morning and will work together in teams in the afternoons on solving design exercises. The teams will present the results on the last day of the workshop.**
- Lectures over the past years have included:
- Analog front-end design, ADCs, fast timing circuits, digital flow, cryogenic readout circuits, introduction to particle physics, experimental collider physics, cryogenic detectors, and accelerator physics.

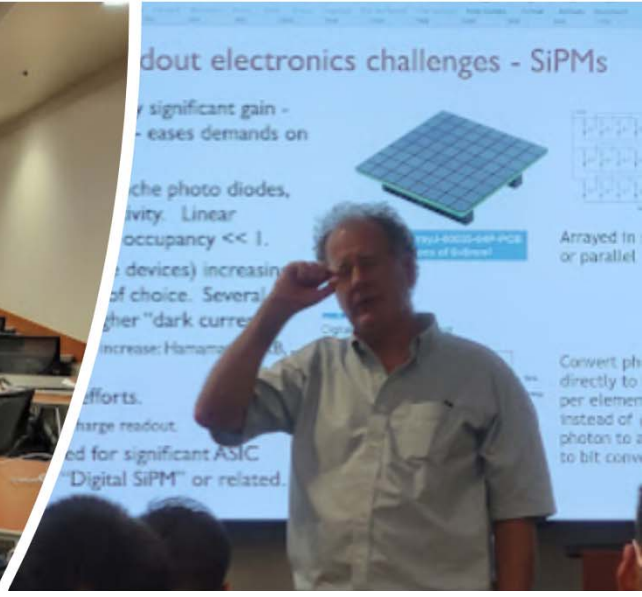
Highlights:

~20 participants (Ma-Postdoc)
4.5 days
4 plenary lectures on high-energy physics
4 plenary lectures on instrumentation
4 afternoons of IC design time
1 student presentation session

SLAC NATIONAL ACCELERATOR LABORATORY

Testimonials and impressions

- *‘I learned a lot in terms of physics of colliders and accelerators and how that physics is translated to hardware design and circuits. As a non-expert in IC, I learned a lot about circuits and their components.’*
- *‘Thank you for this amazing experience, I had a lot of fun and enjoyed meeting the other students.’*
- *‘Before participating in this program, I had very limited knowledge about High Energy Physics detectors. After experiencing the lectures, tours, and working on the design challenge, I am definitely intrigued by the prospect of designing readout ASICs for HEP detectors.’*



Sign-up Now For The Next Edition!

High Energy Physics (HEP) IC Design Traineeship Program

SLAC National Accelerator Laboratory. Menlo Park, California

June 24 - 28, 2024

https://indico.slac.stanford.edu/event/8802/

Final deadline for registration: June 1st. Currently 9/20 slots are filled.

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Program Organization

During Fall Quarter

- Students find out about program during graduate orientation
- They apply to the program, and start taking IC design classes
- PIs review applications and select apprentice

During Winter Quarter

- Lab propose projects
- Virtual meeting where projects are introduced
- Student – lab project matching process

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Program Organization, cont'd

Spring Quarter

- Students continue to take IC design classes
- Start talking with their lab about their project

Summer Quarter

- SLAC summer school
  - Brings all the students together
- Work on their project at their lab.

Following year, they continue working on their degree

- Usually continue some connection with lab

Program Progress

First year had 3 students

- SLAC, Fermi, BNL
  - Two students converted from MS to PhD
  - One is doing his PhD at SLAC

Second year had 5 students

- SLAC, LBL, Fermi

Current year has 7 students

- SLAC, LBL, Fermi, BNL

How Funding Works

Funding is restricted to around $55k

- Direct student support, no overhead
- But smaller than annual cost of student at Stanford

Stanford, UCSC, UCD

- Are on quarter system
- Students are selected fall quarter
- Support students in Winter, Spring, Summer

Conclusion

The program is running well

- Would be better to have a larger pool of students

Please reach out if you are interested in joining