Cross-Institutional Training and Continuous Education in ASIC Design

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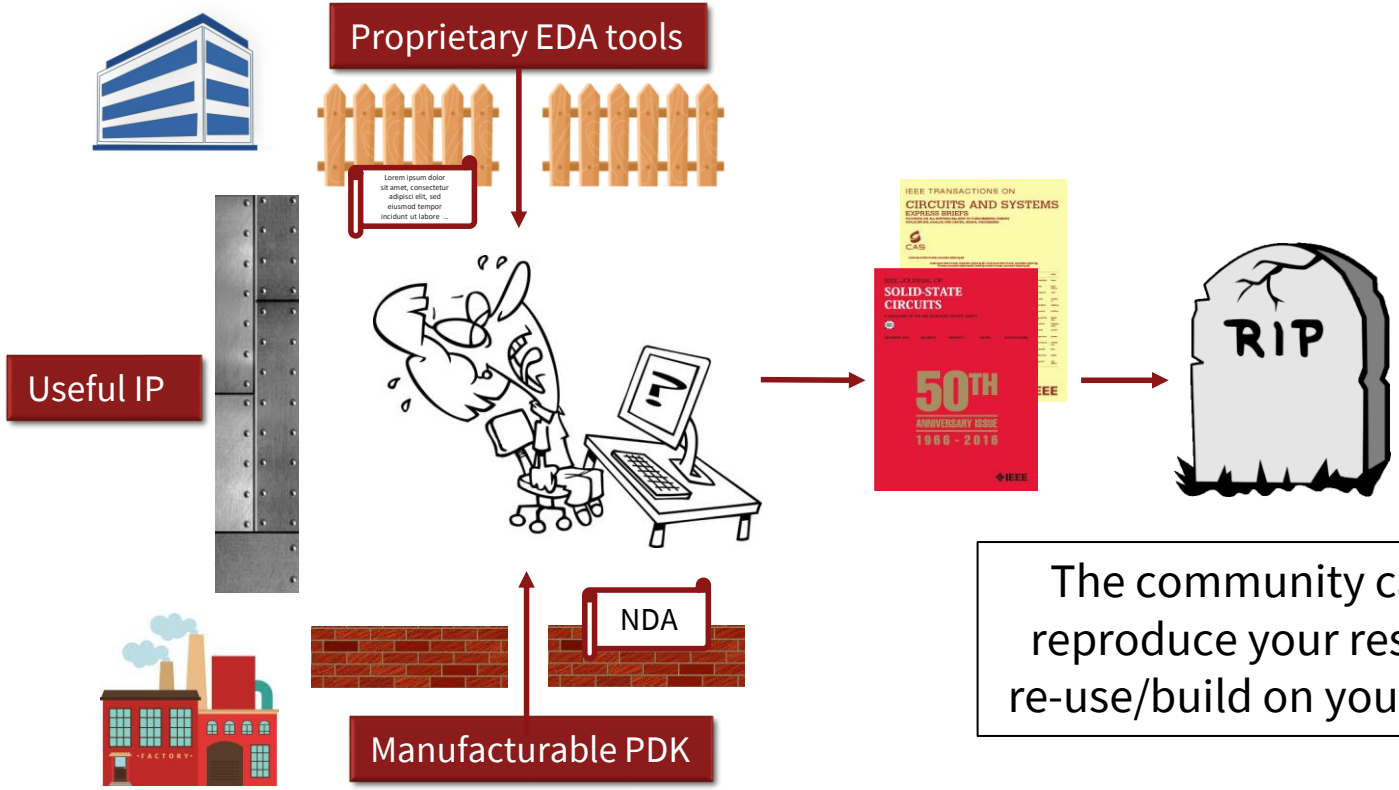
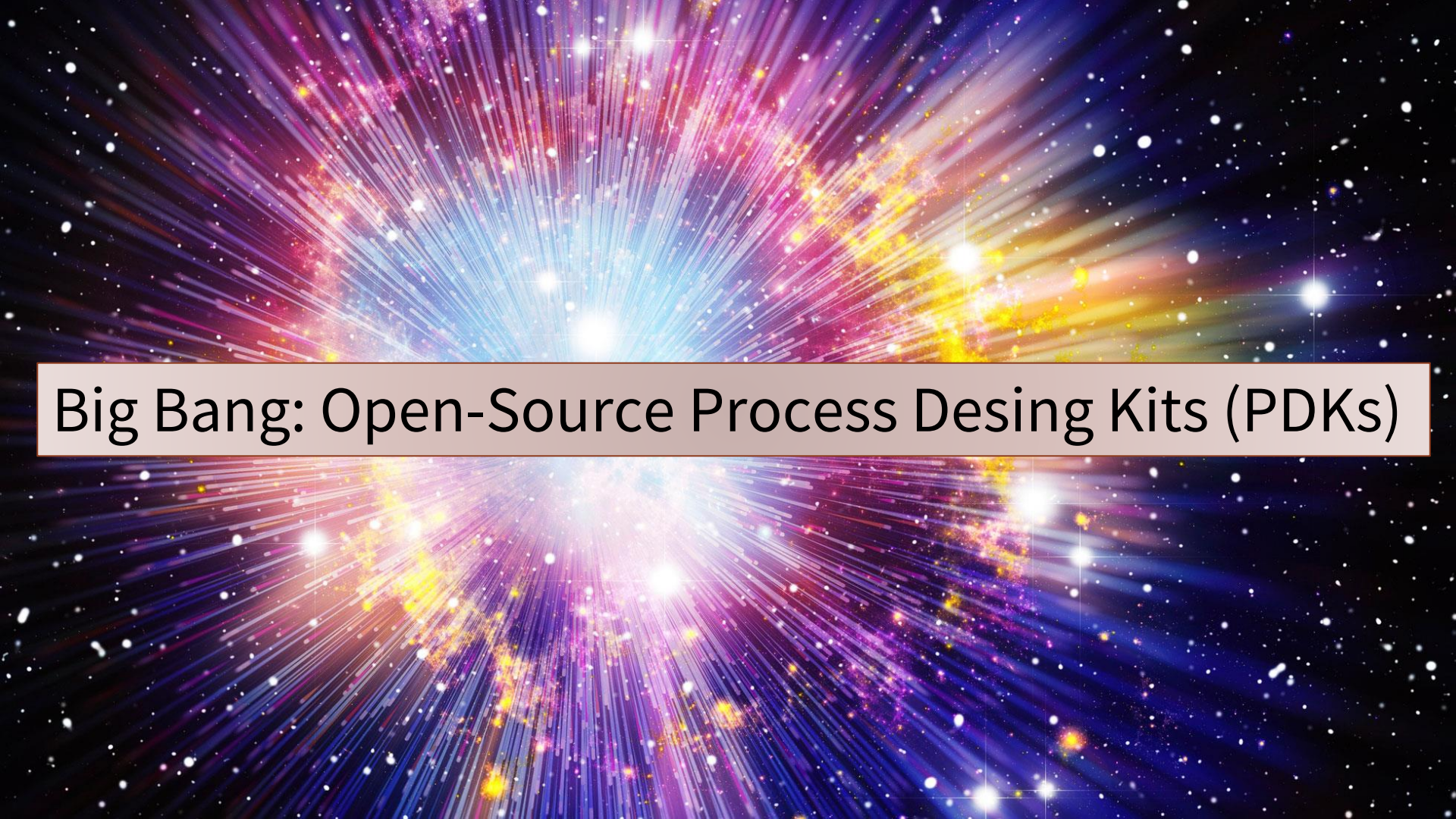
May 2, 2024

Decade-Old Dilemma in IC Research and Education



The community cannot reproduce your results or re-use/build on your design


Big Bang: Open-Source Process Desing Kits (PDKs)

Open-Source PDKs

- First open-source PDK (November 2020)
  - SkyWater 130nm CMOS
  - https://github.com/google/skywater-pdk
- Second open-source PDK (October 2022)
  - GlobalFoundries 180nm MCU
  - https://github.com/google/gf180mcu-pdk
- Third open-source PDK (March 2023)
  - IHP 130nm BiCMOS
  - https://github.com/IHP-GmbH/IHP-Open-PDK
- Permissive Apache 2.0 licensing

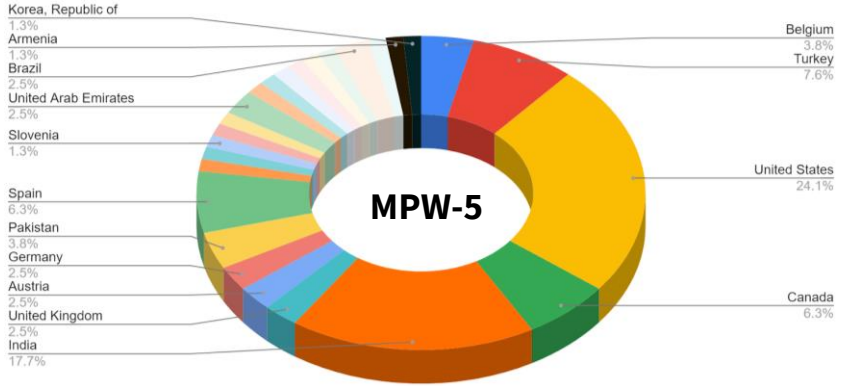
Tim (mithro) Ansell (They/Them) · 1st
Software Engineer at Google

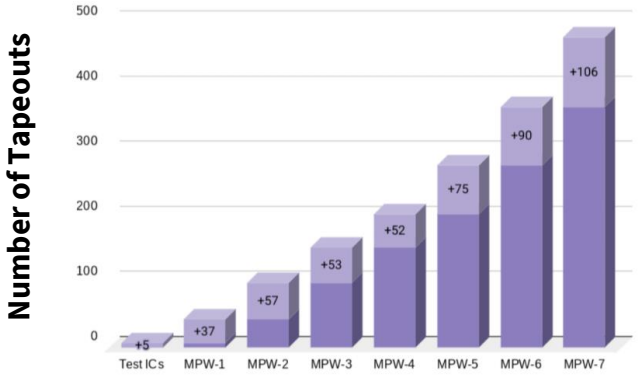
Google + skywater TECHNOLOGY + ihp + GLOBAL FOUNDRIES

Fast Rise Fueled by Google-Sponsored Fabrication Runs

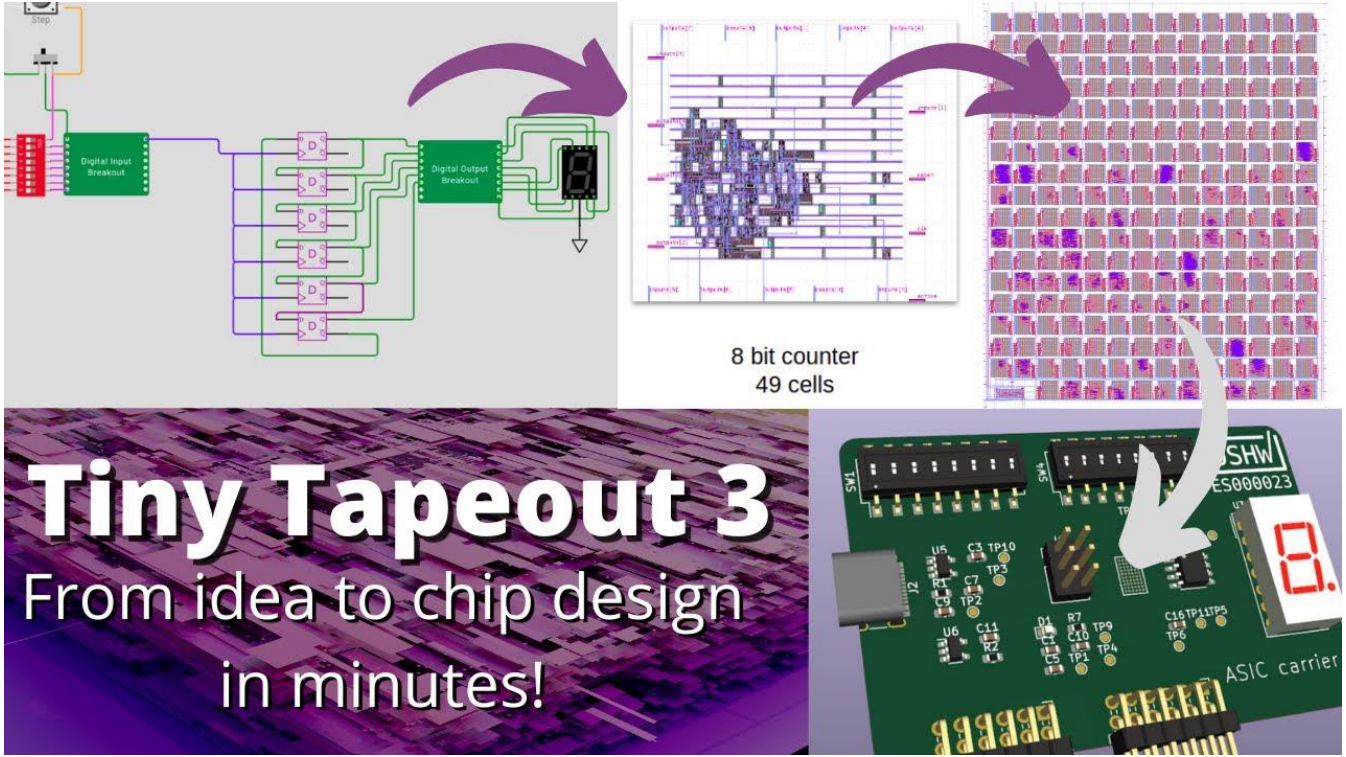
Efabless Caravel “Harness” SoC

efabless.com





Tiny Tapeouts!

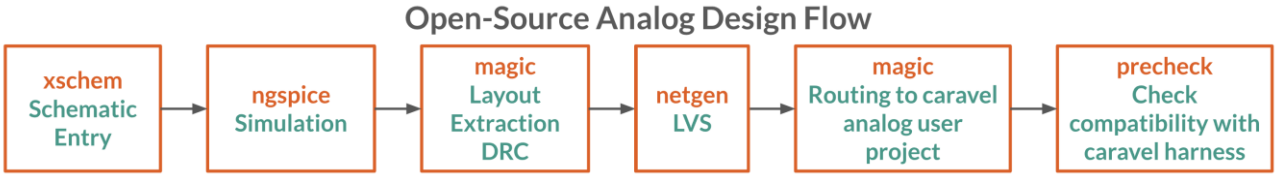


Matt Venn

“Tape-Out” Courses

EE372 - Design Projects in VLSI Systems II

Design and tape out your own digital, analog or mixed-signal chip in an open-source technology!

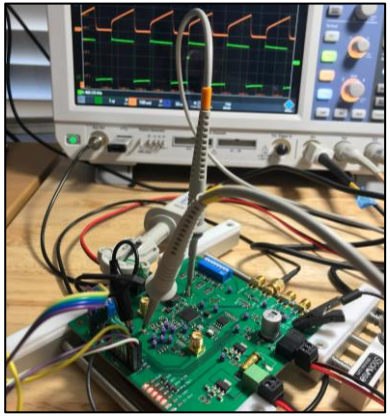


Prof. Priyanka Raina

Weston Braun
@WestonBraun

The Open PMIC works! Still a lot of blocks I need to verify further, but it works! What a relief.

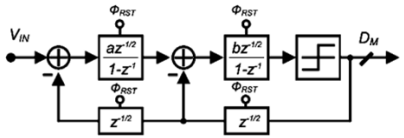
Testing here at a 3.3V to 1.8V step down. It's 90.2% efficient at 0.25W of output power.

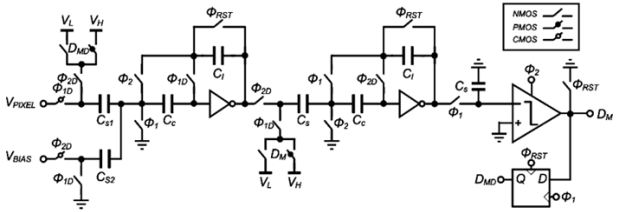


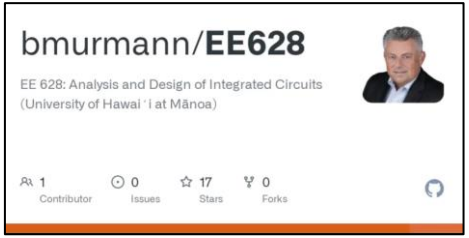
https://priyanka-raina.github.io/ee372-spring2022/

EE 628 at the University of Hawaii

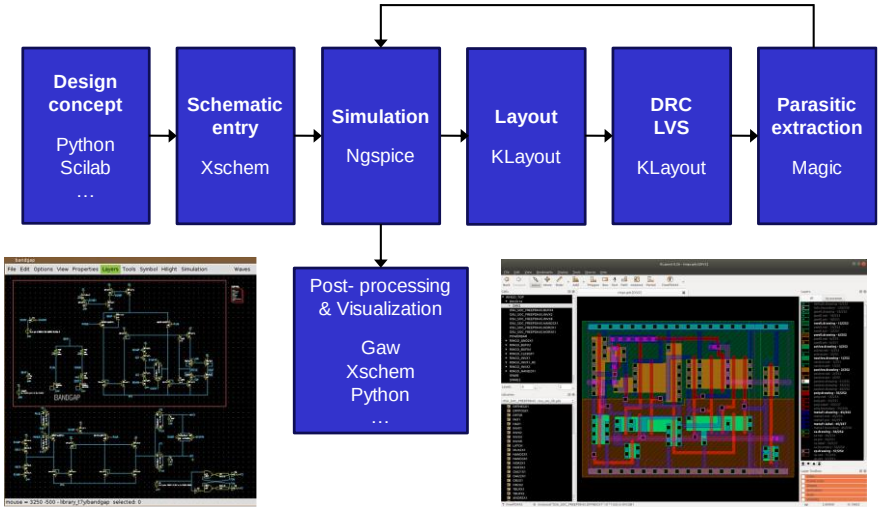
[Chae, JSSC 1/2011]







High-level model → Design and layout of complete transistor-level circuit



Realistic IC Design in the Cloud – For Free

Open in Colab

https://github.com/bmurmann/Ngspice-on-Colab/blob/main/notebooks/SKY130_Track_and_Hold.ipynb

SKY130 Track and Hold Circuit

Tool setup

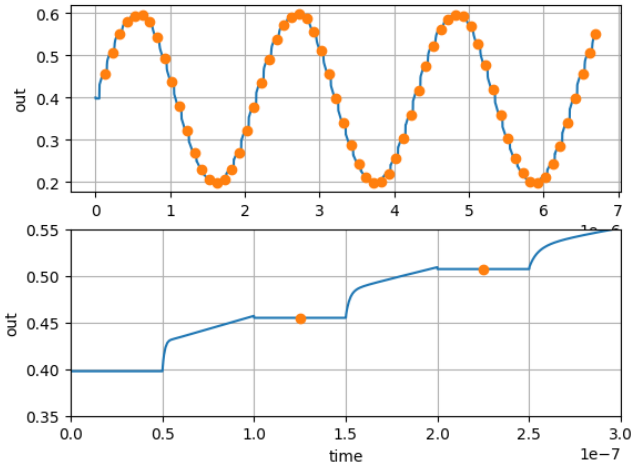
```
import pandas as pd
import matplotlib.pyplot as plt
import numpy as np
import os
CONDA_PREFIX = os.environ.get('CONDA_PREFIX', None)
if not CONDA_PREFIX:
  !python -m pip install condacolab
  import condacolab
  condacolab.install()

# install sky130a
!conda install -c litex-hub open_pdks.sky130a

# install ngspice
!conda install -c litex-hub ngspice
```

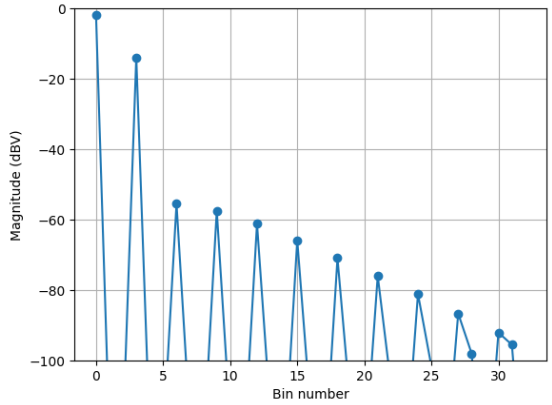
Realistic IC Design in the Cloud – For Free

```
%%writefile netlist.spice
* Track-and-hold circuit using single NMOS
.lib "/usr/local/share/pdk/sky130A/libs.tech/ngspice/sky130.lib.spice" tt
x1 in clk out 0 sky130_fd_pr__nfet_01v8_lvt w=5 l=0.15
cl out 0 100f
vin  in 0 sin (0.4 0.2 {fin})
vclk clk 0 pulse (1.2 0 0 100p 100p {per/2} {per})
.param nfft=64 fclk=10Meg per=1/fclk cycles=3 fin=fclk*cycles/nfft
```

```
df1 = pd.read_csv("output1.txt", delim_whitespace=True)
df1
```

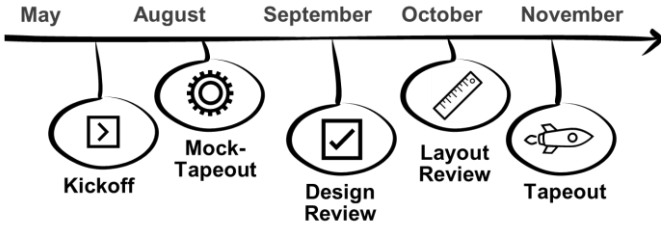
	time	out
0	0.000000e+00	0.400000
1	1.000000e-12	0.399961
2	2.000000e-12	0.399922
3	4.000000e-12	0.399845
4	8.000000e-12	0.399695
...	...	...

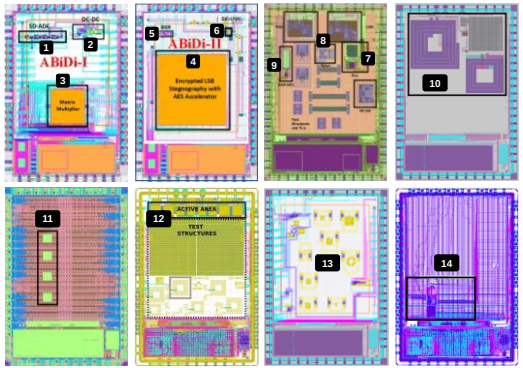




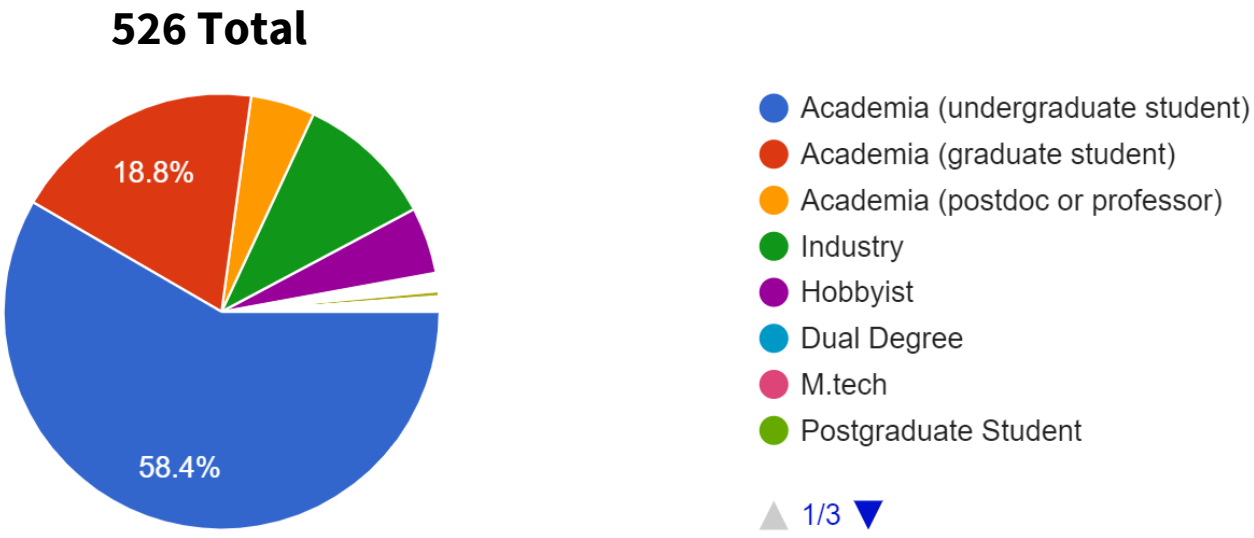
IEEE Activities

- **SSCS Platform for Integrated Circuits Outreach (PICO)**
  - https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-program
  - Annual Chipathon
  - Code-a-Chip Travel Grants
- **Universalization of IC Design from CASS (UNIC-CASS)**
  - Mentoring & tape-out support
  - https://ieee-cas.org/universalization-ic-design-cass-unic-cass
- …





Sign-Ups for 2023 SSCS PICO Chipathon



Outline of 2023 SSCS PICO Chipathon

- Phase 1: Learn layout automation using Python
- Phase 2: Form teams and define larger cells
- Phase 3: Build generators for larger cells
- Phase 4: Integration & test-chip tapeout
- Phase 5: Measurement & documentation

https://sscs.ieee.org/about/tc-ose/sscs-pico-design-contest

Open-Source IC Design Ecosystem

Standardization, shared IP

Advanced tools, open collaboration, repositories

Free tools, open collaboration

“Physics-minded”
talent pool interested ICs

NEW

“Software-minded”
talent pool interested in ICs