



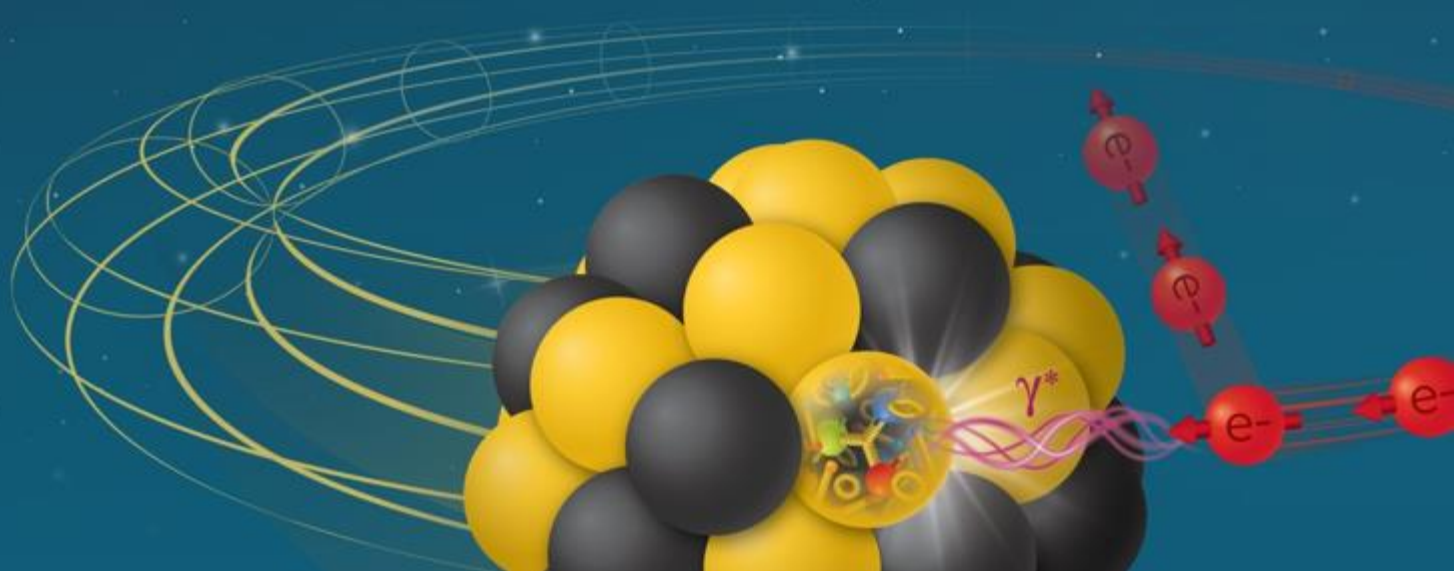
MPGD readout electronics

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Incremental Design and Safety Review
of the EIC Tracking Detectors
March 20-21, 2024

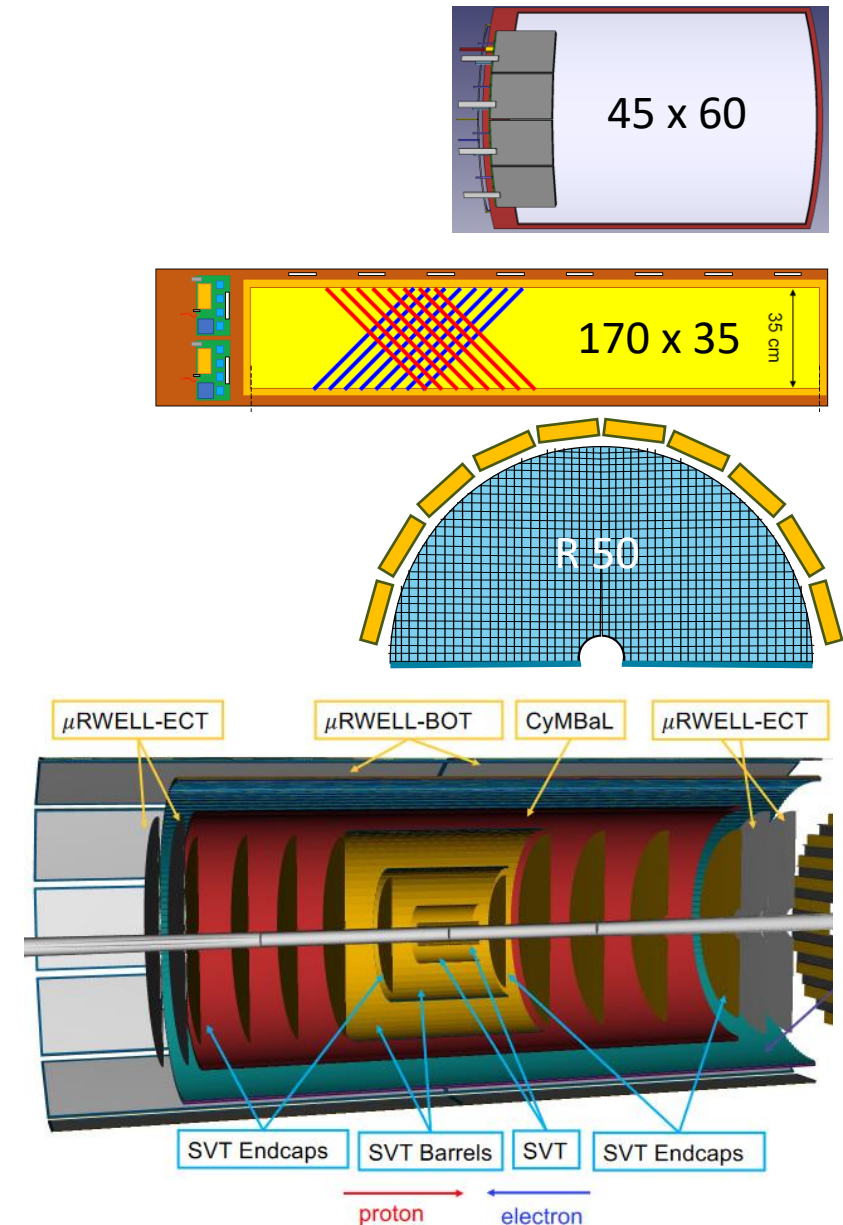
Electron-Ion Collider



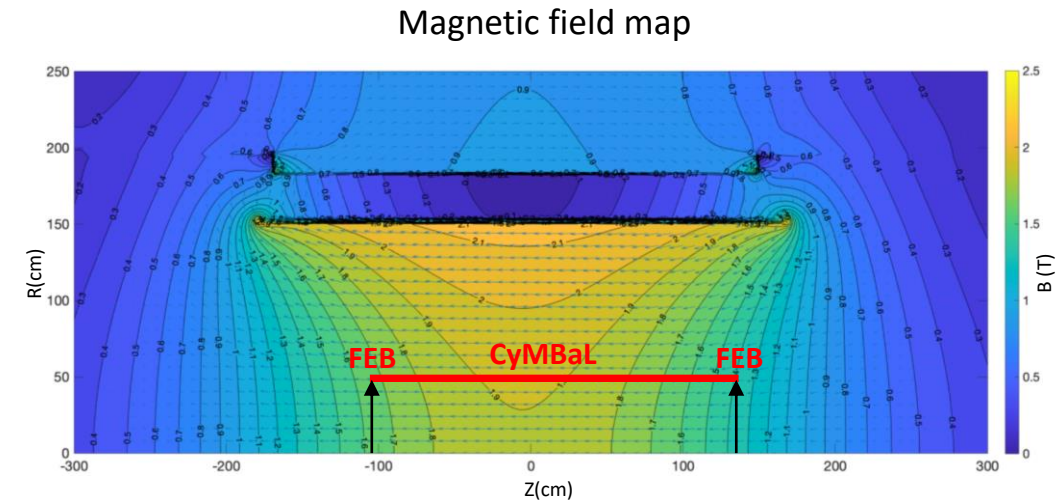
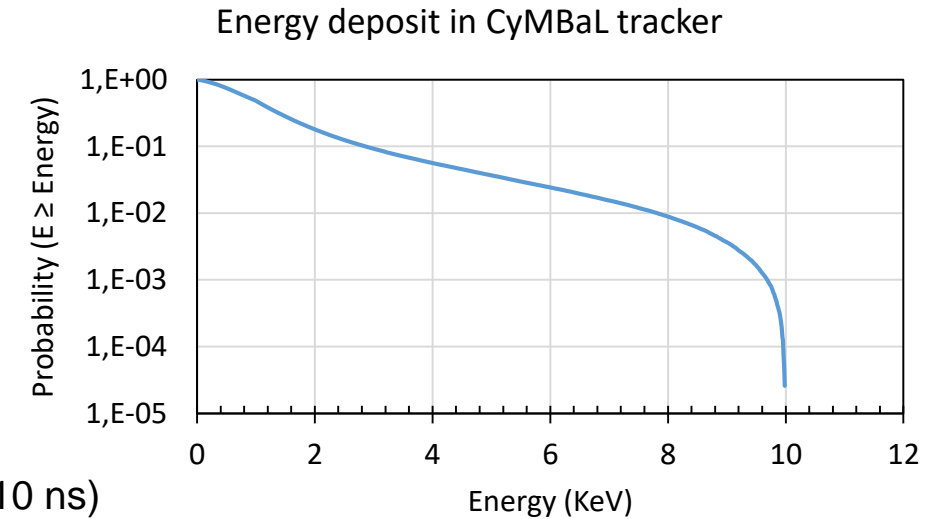
- Requirements
- Readout architecture
 - Salsa ASIC
 - FEB
 - System scale
- Organization
 - Production strategy
 - Planning
 - QA and risk mitigation
- Summary
- References
 - Signal - https://indico.bnl.gov/event/20965/contributions/82420/attachments/50649/86604/231026_IM_CyMBal_ExpectedSignal.pdf
 - Data collection - https://indico.bnl.gov/event/18118/contributions/72179/attachments/45781/77366/221221_MpgdDataCol_IM.pdf
 - Calibration - https://indico.bnl.gov/event/16040/contributions/64090/attachments/41290/69185/220520_MpgdTrack_CalibRates_IM.pdf
 - Salsa - https://indico.bnl.gov/event/22053/contributions/86152/attachments/52272/89395/SALSA_EPIC_electronics_DAQ_20240125.pdf
 - MPGD LV - https://indico.bnl.gov/event/22316/contributions/87363/attachments/52727/90159/240215_IM_MpgdPower.pdf
 - FEB options - https://indico.bnl.gov/event/21104/contributions/83856/attachments/51197/87574/231127_IM_Mpgd_VtrxPlus.pdf
 - Detailed study of FEB organization options and their powering schemes – provided in support material
 - Run control state machine and proposal of synchronous commands – provided in support material
 - Salsa and Prisme PLL IP – proposals, provided in support material

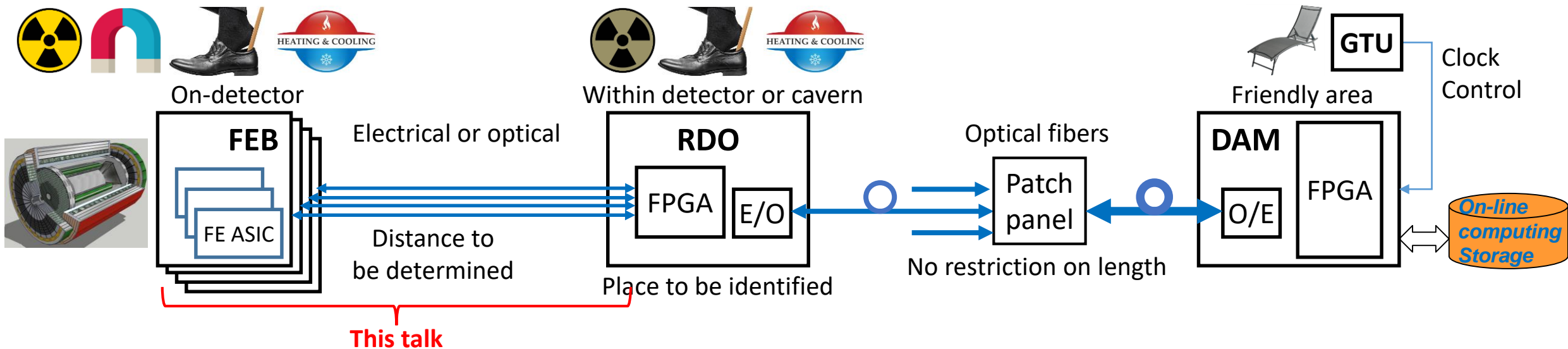
1. Are the technical performance requirements appropriately defined and complete for this stage of the project?
2. Are the plans for achieving detector performance and construction sufficiently developed and documented for the present phase of the project?
3. Are the current designs and plans for detector, electronics readout, and services sufficiently developed to achieve the performance requirements?
4. Are plans in place to mitigate risk of cost increases, schedule delays, and technical problems?
5. Are the fabrication and assembly plans for the various tracking detector systems consistent with the overall project and detector schedule?
6. Are the plans for detector integration in the EIC detector appropriately developed for the present phase of the project?
7. Have ES&H and QA considerations been adequately incorporated into the designs at their present stage?

- Cylindrical Micromegas Barrel Layer : **CyMBaL** : ~30k channels
→ 32 tiles of 1024 channels each
- μ RWELL Barrel Outer Tracker : **μ RWell-BOT** : ~100k channels
→ 24 modules of 4 096 U-V strips each
- μ RWell End Cap Tracker : **μ RWell-ECT** : ~30k channels
→ 8 half-disks of 4 000 X-Y strips each
- ~160k-channel heterogeneous system
→ Micromegas, μ RWell, barrel, endcap, curved, planar, circular
- Common approach to acquire data from different types of ePIC MPGDs
 - Use same frontend ASIC
 - Share frontend design between groups
 - Adapt form factor if needed

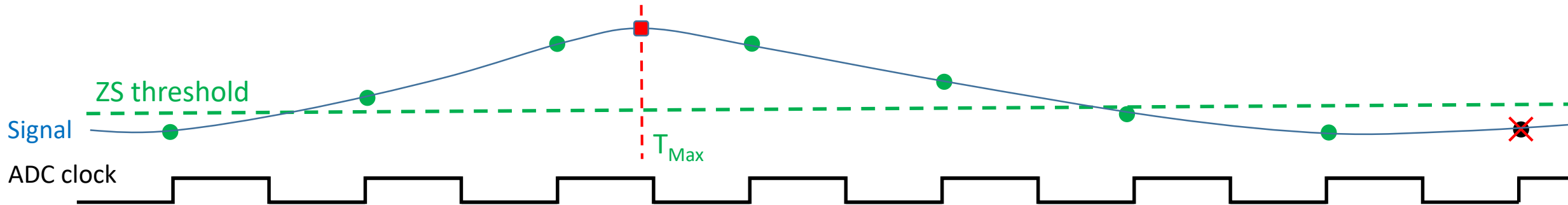


- Typical signal 1-1.5 keV resulting to 15-30 fC per channel
 - Cluster sizes, detector gains, charge collection
- Aimed dynamic range of 10-bits
 - Signal / noise of ~60
 - S/Th ≈ 10 and Th/N ≈ 6
 - Max / signal of ~10
- Timing precision of few ns
 - Low contribution to the aimed overall time measurement accuracy of ~O(10 ns)
- Channel occupancies of ~10 kHz
 - Including factor π of safety margin
- Streaming readout
 - With support of *in-situ* calibration and of on-demand readout
- ~1.8 T magnetic field
- Mild radiation environment
 - TID and neutron fluence after 10 years: 10 krad and $10^{11} \text{ n}_{\text{eq}} / \text{cm}^2$
 - 20 MeV proton flux: 100 particle / cm^2 / s
- Stringent space for detector readout and services



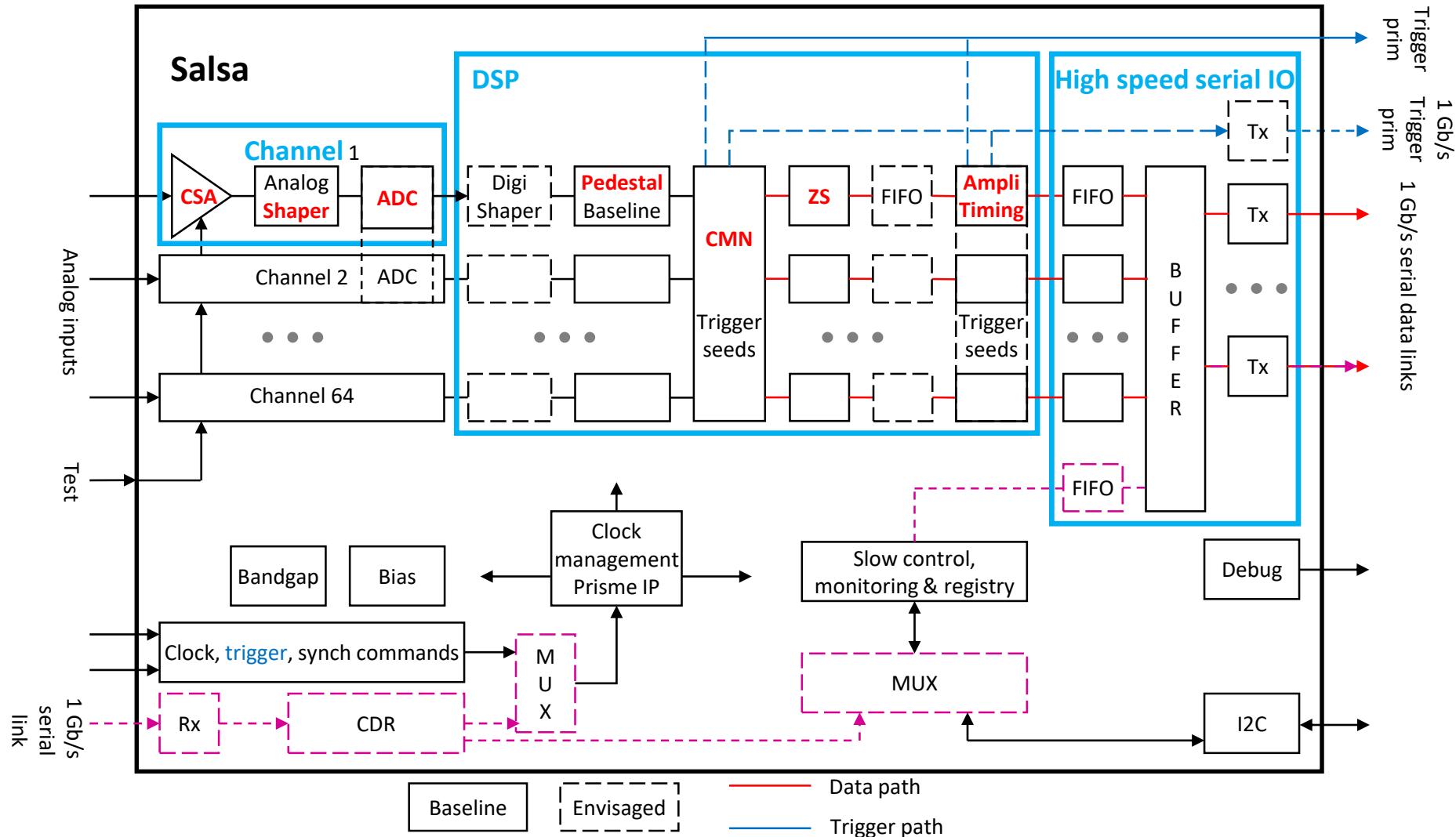


- FEB – frontend board with readout ASICs
 - Sub-detector specific
- RDO – readout module – first stage of FEB data aggregation, last stage to dispatch clock & control
 - Mostly common design framework between sub-detectors, different form factor
- DAM – data aggregation module – interface with computing and global timing and control unit (GTU)
 - Common design for all sub-detectors
- Downstream towards detector : clock, control, monitoring
- Upstream towards storage : physics, calibration, monitoring data



- Signal is continuously sampled with an ADC
- Signal samples above threshold are retained
- Nominal (physics data) readout : signal amplitude and timing is derived
 - Time of max (as on example) or time of arrival (fitting samples on rising edge)
- On-demand readout : signal shapes or raw non-ZS data are provided
 - Calibration, detector studies
- Guarantees best noise immunity and thus best S/N ratio
 - Allows on-line common mode noise (CMN) subtraction before ZS

Salsa : a 64-channel versatile MPGD readout ASIC



- Currently under development by a collaboration of Irfu, CEA Saclay and University of Sao-Paulo
→ Support from Project R&D program for Salsa prototyping including clock management IP Prisme

- Channel features

- 4 dynamic ranges : 50 fC, 250 fC, 500 fC, 5 pC
- 10 peaking times : from 50 ns to 500 ns
- Support for high input capacitances up to 1 nF and beyond
- Both signal polarities
- Rate per channel : up to 100 kHz
- Sampling rate : programmable, up to at least 50 MSPS
- 12-bit ADC with >10-bit ENOB

ePIC MPGD needs

250 fC
100-200 ns
~200 pF
Negative
<10 kHz
50 MSPS
>9.6 bits

- Digital stage programmable features

- Pedestal equalization, common mode noise subtraction, zero suppression
- Baseline tracking
- Signal amplitude and timing extraction

All

Main readout option

- Clock management with Prisme IP :

- Wide range jitter cleaner PLL, 4 clock frequency synthesizer, phase adjustment

100 MHz

- Streaming and triggered readout

- Four 1 Gbit/s serial links
- Non-ZS, signal shape or time-amplitude readout

Single Gbit/s link
All

- Backend

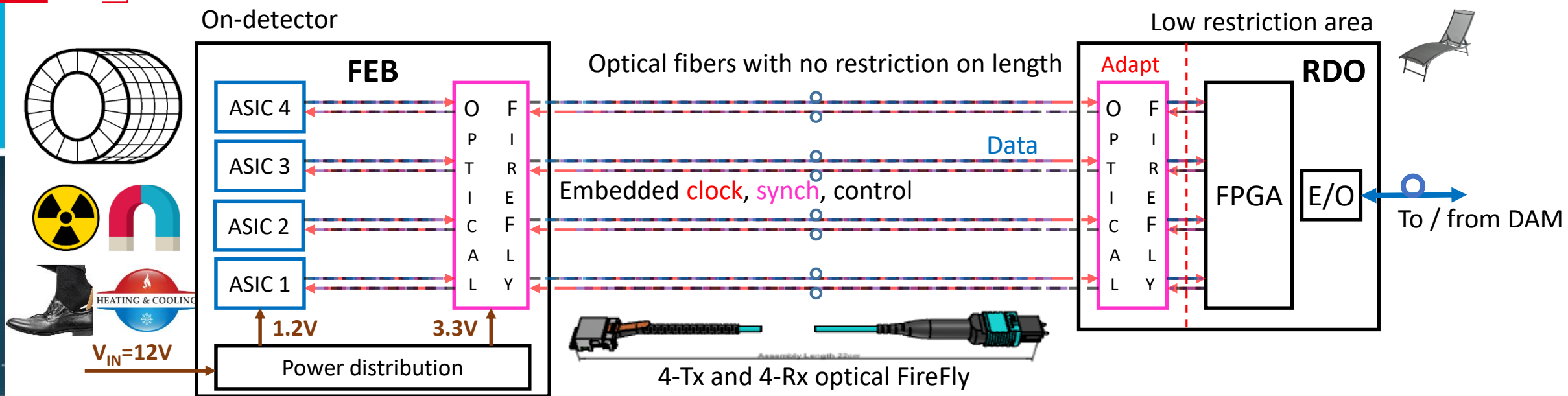
- Traditional interface with separated clock, sync command and control ports
- Innovative unified interface over 1 Gbit/s input link

Baseline

- Implementation

- 65 nm TSMC
- 10-15 mW/ch @ 1.2V
- Radiation hardened : SEU, > 300 Mrad, > 10^{13} n_{eq} / cm²

10 krad, 10^{11} n_{eq} / cm²



• FEB

- ASICs directly connected to 4-lane bidirectional parallel optic FireFly transceivers from Samtec
 - Single 1 Gbit/s Rx line encoding clock, sync run-control and asynchronous slow control and monitoring commands
 - Single 1 Gbit/s Tx line for physics, calibration, control and monitoring data
- Low active component count
 - Easier to adapt to challenging on-detector environment
 - Samtec FireFly : reported to stand TID of 50-100 krad and neutron fluence of at least $5 \times 10^{11} \text{ n}_{\text{eq}} / \text{cm}^2$

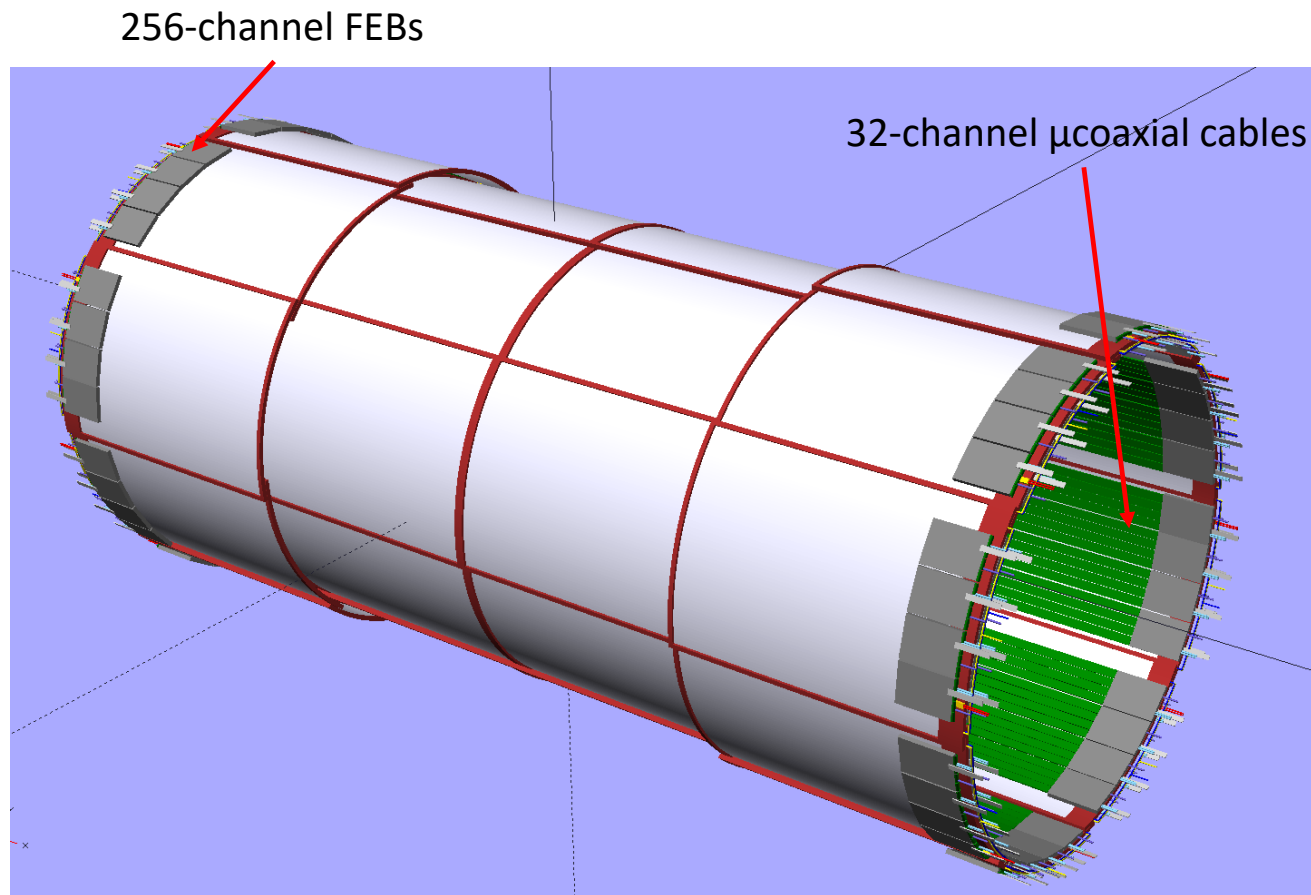
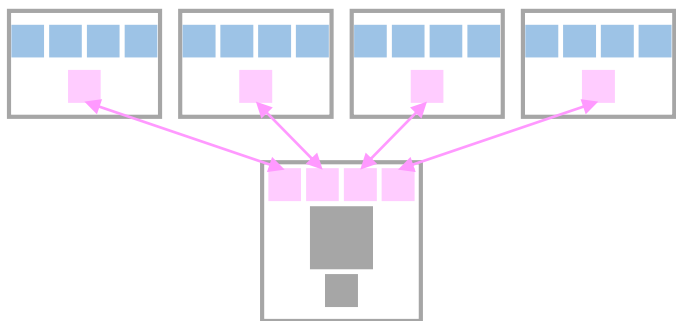
• RDO

- Based on **common ePIC design with minimal adaptation for MPGDs**
- Can be placed anywhere in experimental hall with no particular environmental restrictions

• Optimal tradeoff between complexity of the on-detector electronics and its power consumption

- 32K channels
- 128 256-channel FEBs
→ 4 Salsa ASICs per FEB
- 32 1024-channel RDOs
→ 4 FEBs per RDO

16 Salsa-s, 4 FEBs, 1 RDO = 1024 channels



- Estimates of operational quantities for MPGDs assuming 256-channel FEBs

	CyMBaL		μ RWell-BOT		μ RWell-ECT		Total
	Tile	Sub-detector	Module	Sub-detector	$\frac{1}{2}$ disk	Sub-detector	MPGDs
FEB	4	128	16	384	16	128	640
Salsa	16	512	64	1 536	64	512	2 536
RDO	1	32	4	96	4	32	160

- Production quantities
 - Including prototyping, test-bench and quality assurance needs

→ 750 FEBs
 → 4 000 Salsa-s
 → 200 RDOs

- Work in progress to understand impact of mechanical constraints on FEB design
 - Possibility to use the same form factor and ASIC integration level for all MPGDs

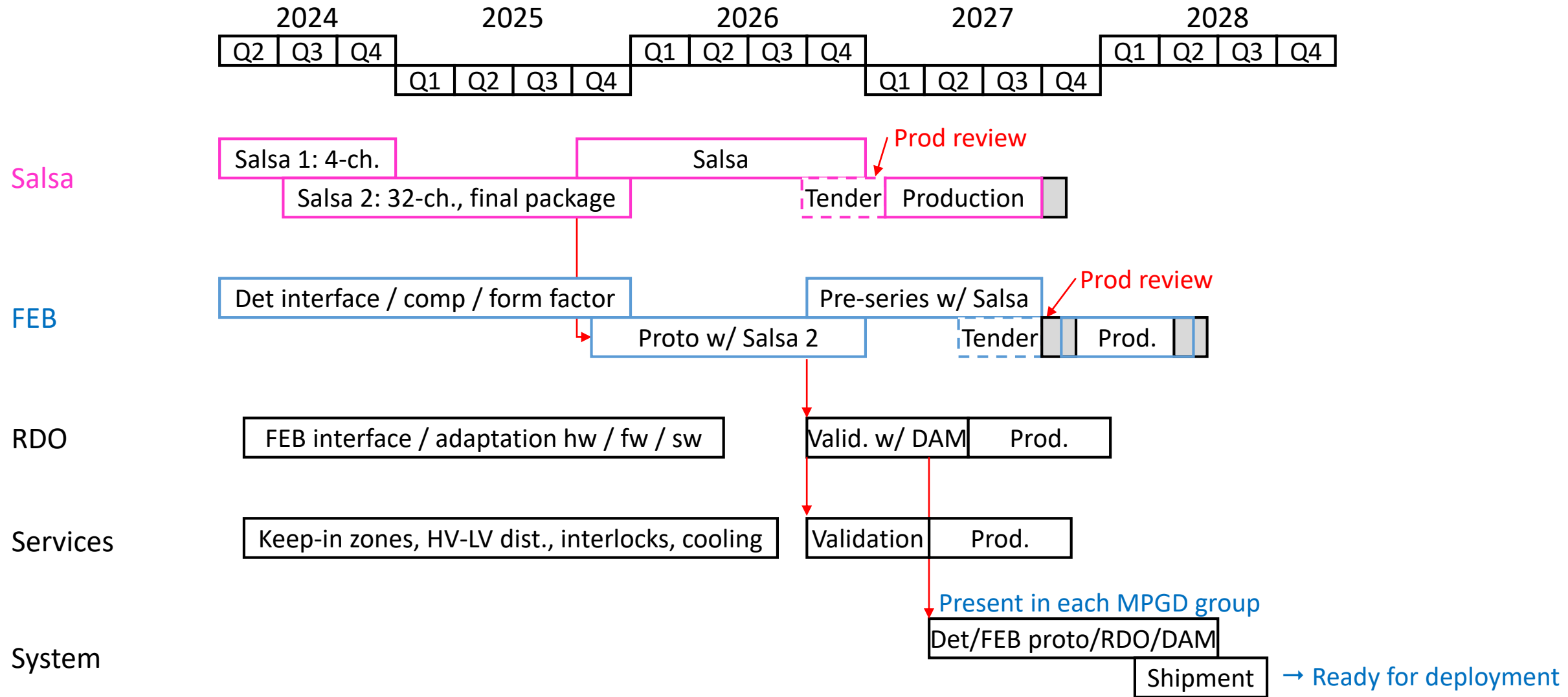
- Salsa and clock management Prisme IP prototypes developed
 - Analog channel and clock synthesizer validated
- Several alternative FEB options have been evaluated
 - Passive electrical RDO interface, VTRX+ optical RDO interface, merged FEB/RDO
- Data collection and calibration protocols elaborated
 - Physics and calibration data throughput estimated
 - On-line periodic calibration is possible
 - FEB – RDO link occupancy is ~30 % : comfortable safety margin
- LV power requirements estimated and power distribution schemes compared
 - e.g. Baseline FEB with FireFly optical interface requires : ~9W or 35 mW / channel
- Detector – FEB connectivity studies on-going
 - Compact and low-cost micro-coaxial cable assemblies from KEL under evaluation
- R&D on Samtec FireFly optical transceivers
 - In close contact with Samtec optical division
 - Bilateral NDA between Samtec and Irfu, CEA Saclay renewed

More info in links on Outlook page
and in backup slides



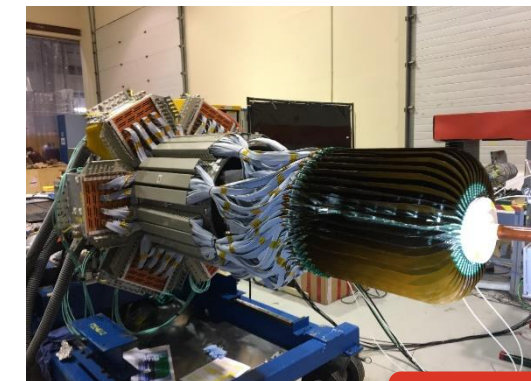
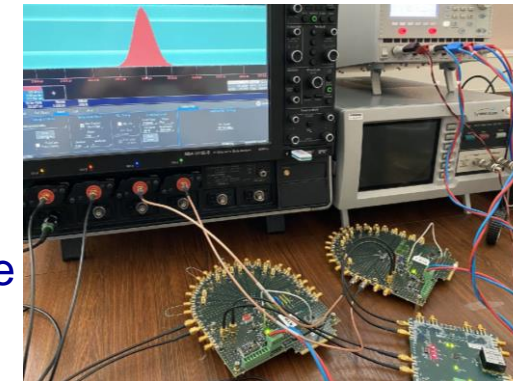
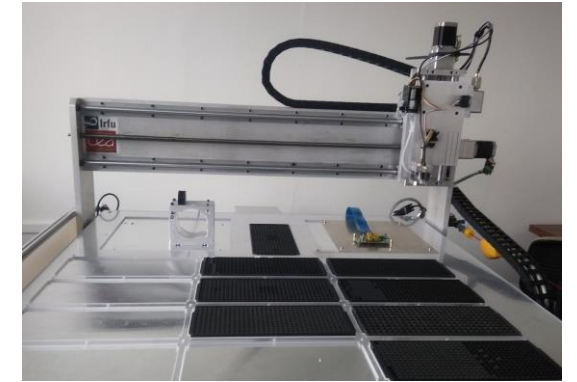
- Salsa will be produced and tested in quantities that will cover the needs of all ePIC MPGDs
- The FEB design will be shared with all MPGD groups
 - If needed, FEB design adaptation for a particular geometry will be under sub-detector responsibility
- Common effort to adapt RDO-s and DAM-s to MPGD readout
 - Firmware and Software
 - And partially RDO hardware
- Common effort on services
 - LV and HV distribution, interlock, slow control and cooling
 - Common concern of several sub-detector systems in magnetic field
- FEB and RDO production and qualification tests will be shared between several sites
 - Faster completion track
 - Especially in case of different FEB form factors
 - Lower risk associated with procurement and task execution delays

Planning



- Tight schedule mainly driven by Salsa development phases
→ With ~6-9-month contingency

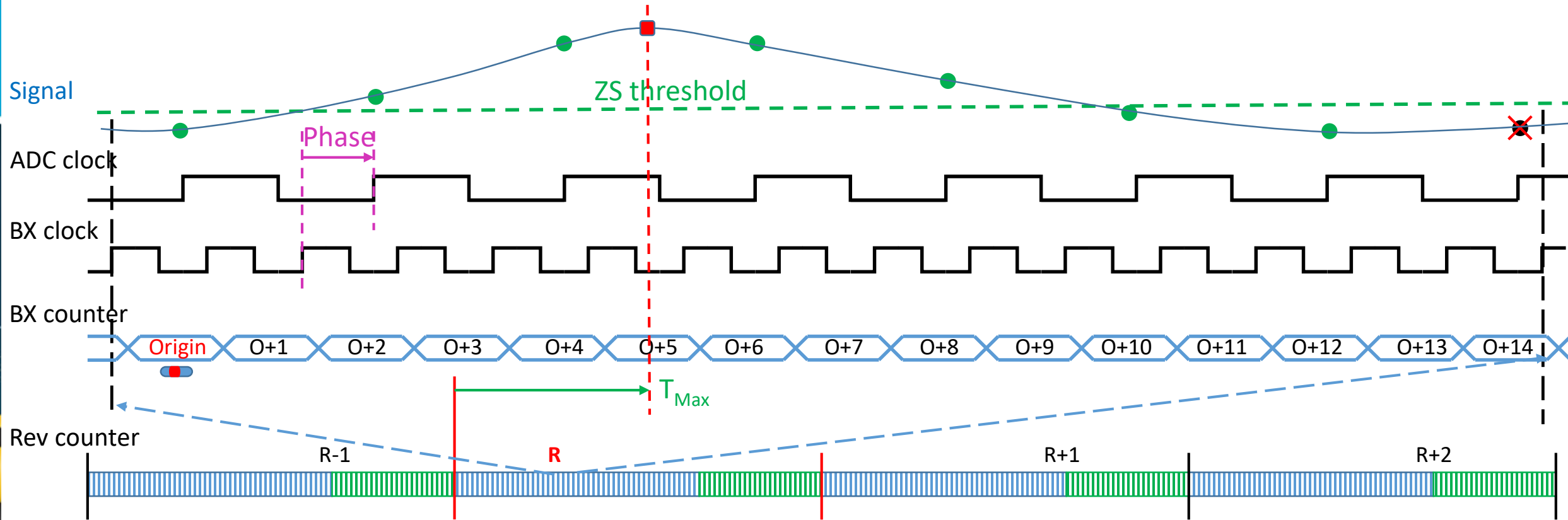
- Expertise at Saclay in large scale production of ASICs and frontend boards
 - In-house : automated ASIC tester robots and FE production test benches
 - In industry : providing turn-key test benches
 - Ex: 40 000 Rafael and 80 000 Catia ASICs for CMS Ph2 upgrade
 - Ex: 700 Alice Solar, 170 LTDB Atlas, 150 Clas12 FEU boards
- Rich set of equipment for Salsa and FEB test benches
 - High-end LeCroy and Tectronix oscilloscopes
 - High performance phase noise analyzer
 - Low jitter precision clock sources
 - Climate chamber
 - Bonding machines
- Expertise in system-level design, production, commissioning, maintenance
 - Detector – readout electronics – acquisition software – analysis
 - Clas12 MVT, T2K TPCs, Asacusa tracker, ...
 - Respecting ES&H regulations of host labs (BNL, CERN, JLab, J-PARC)
- Expertise in radiation hard ASIC design and validation techniques
 - Access to CERN, French and European radiation source facilities
- Access to high magnetic field facilities
 - At CERN and at Saclay



- Unexpected Salsa behavior or performances issues
 - Diagnostic-correction-production-validation cycle may require 1 year
- Delays in mass-production of FEBs and RDOs
 - At least two production and validation sites
- Component procurement delays
 - Usual practice of anticipated acquisition of long lead time components of choice
 - Establishing privileged partnership with manufacturers
 - e.g. Irfu CEA Saclay has renewed bilateral NDA with Samtec optical division
- Radiation impact on COTS components
 - Use of components from the list of components proven for radiation tolerance
 - Validation of components in radiation facilities for ePIC-like ionization doses and particle fluxes
 - SEU : implementing error detection and recovery mechanisms adopted by ePIC collaboration
- Noise impact on data volume
 - On-line coherent noise subtraction
 - Enough bandwidth to readout signal shapes and apply more sophisticated discrimination algorithms on-line

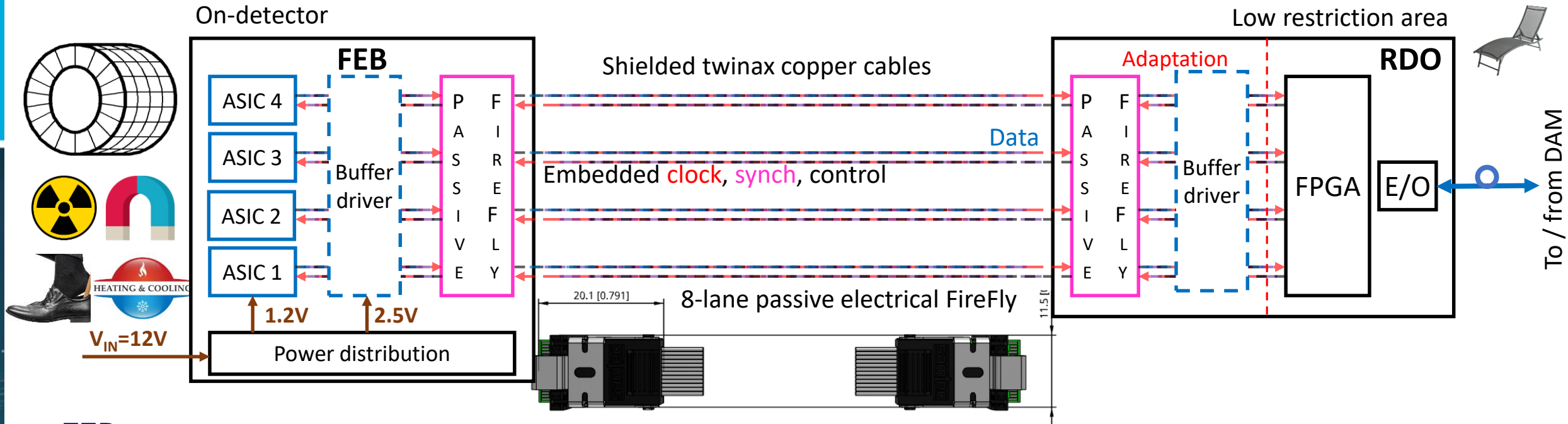
- Envisaged solutions for the ePIC MPGD readout are viable and cover performance requirements
- Engaged groups have necessary experience for large scale system design, production and commissioning
- R&Ds are on-going
 - Detector – FEB connectivity
 - Integrated ASIC interface
 - COTS components validation for ePIC environment
- Design of Salsa ASIC drives current planning
- Closely following and contributing to collaboration-wide efforts
 - Precise identification of keep-in-out zones between the sub-detectors
 - Efficient low form factor magnetic-field tolerant powering means
 - Defining of run-control state machine and set of rules that detector partitions need to obey
 - Error detection and recovery strategy
- Pursuing discussions within the MPGD DSC to identify second site for FEB design and production
 - In addition to Irfu, CEA Saclay
- Planning is compatible with the overall ePIC installation schedule

Backup



- ADC clock is derived from bunch crossing clock and is its (sub)multiple (e.g. ~50 MHz)
 - Known frequency and phase relationship exists between the two clocks
- Signal above threshold is tagged by a timestamp relative to revolution tick
 - Max (as on example) or time of arrival (fitting samples on rising edge)
 - Timing association with data from other sources possible

Backup option: 256-channel FEB with electrical interface



• FEB

- ASICs directly connected to 4-lane bidirectional parallel optic FireFly transceivers from Samtec
 - Single 1 Gbit/s Rx line encoding clock, sync run-control and asynchronous slow control and monitoring commands
 - Single 1 Gbit/s Tx line for physics, calibration, control and monitoring data
- Low active component count
 - Easier to adapt to challenging on-detector environment
 - Samtec electrical FireFly : drop-in compatibility with optical counterpart

• RDO

- Based on **common ePIC design with minimal adaptation for MPGDs**
- Possibly can be placed in a low restriction area

- Attention must be payed for ground loops and noise pickup over long distance

- Physics: support two zero suppression modes

- Nominal : peak finding readout

- 12-bit amplitude, 12-bit time of max, 8-bit ToT

- On-demand : full signal shape readout

- All samples (12-bit) above threshold (typically 15-25)

Estimated CyMBaL **physics** data bandwidth per Salsa ASIC

Channel rate kHz	Peak finding Mbit/s	Signal shape Mbit/s
10 (5 x safety)	40	265

- On-line calibration : on demand readout

- Programmable number of non-ZS samples

- Signal shape for calibration pulse

Estimated **calibration** data bandwidth per ASIC ~6 Mbit/s

- FEB – RDO link occupancy : ~30 %

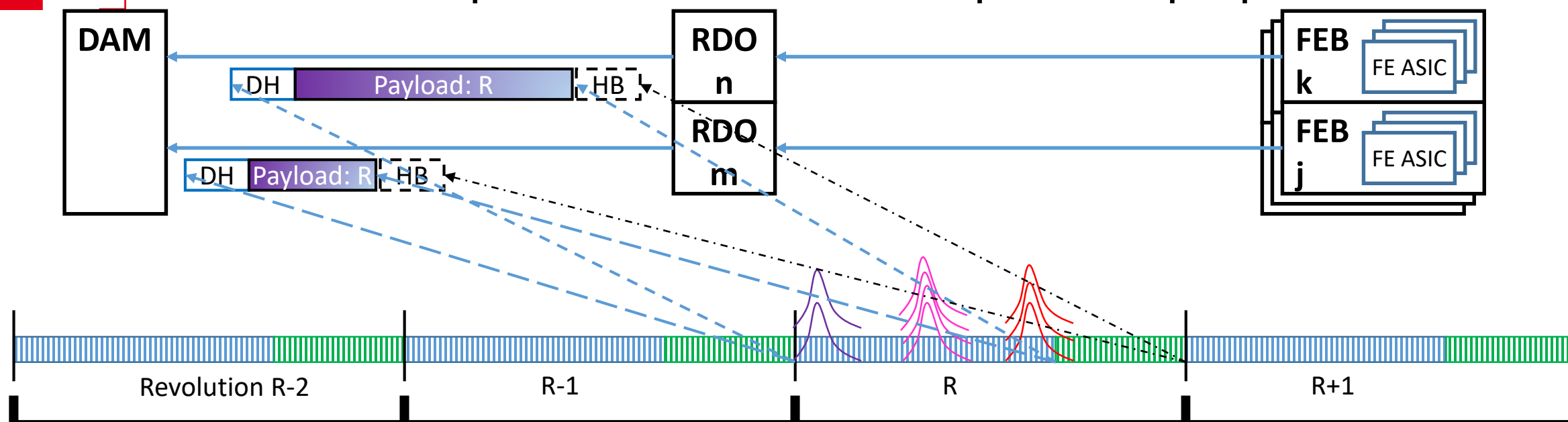
- Comfortable safety margin, even for on-demand signal shape readout

- Overall physics frontend data of MPGDs

- Accurate estimates still to be done

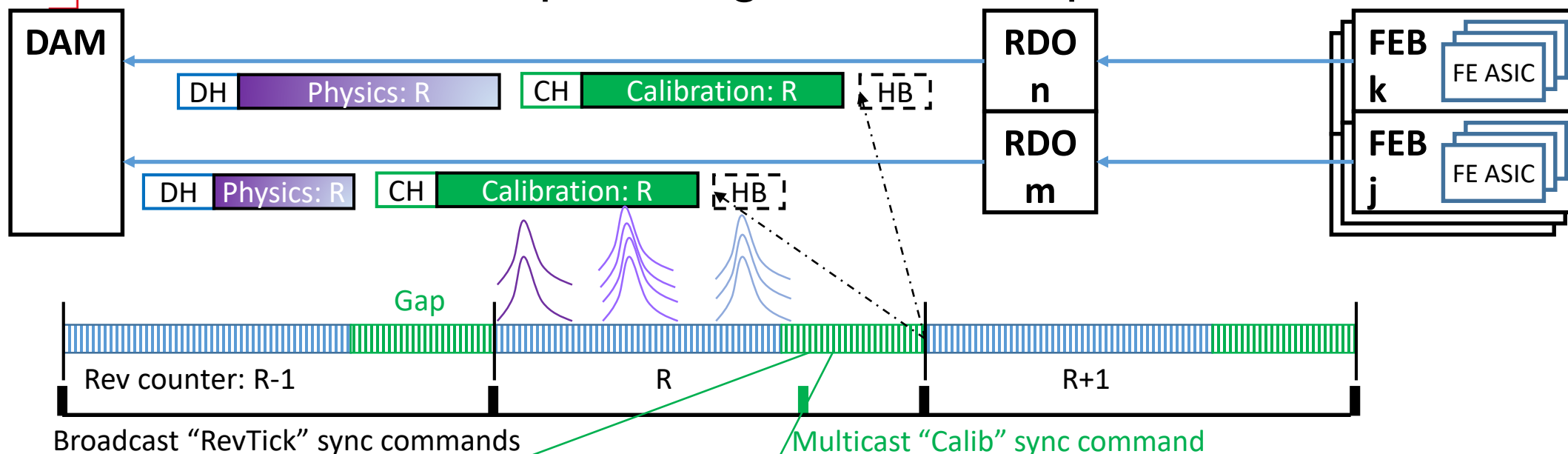
	CyMBaL	μRWell-BOT	μRWell-ECT	Total
Data (Gbit/s)	35	100	35	170

- NB: in nominal operation, the bulk of the physics frontend data will be further processed before being archived
 - e.g. clustering

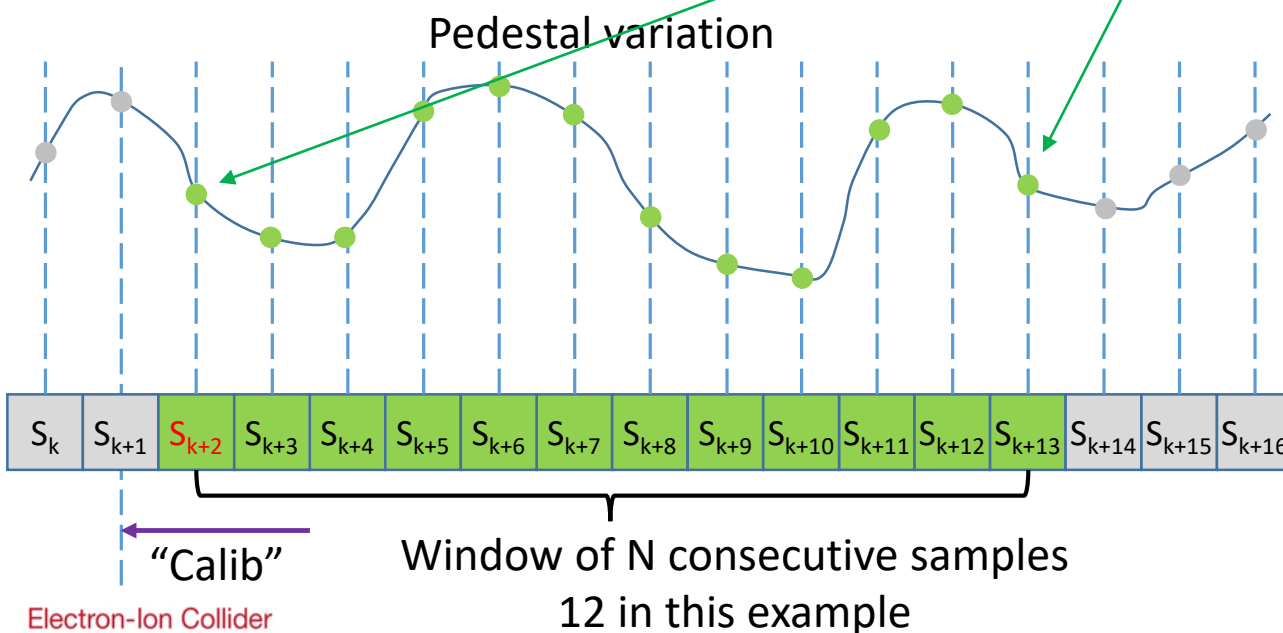


Broadcast "RevTick" sync commands

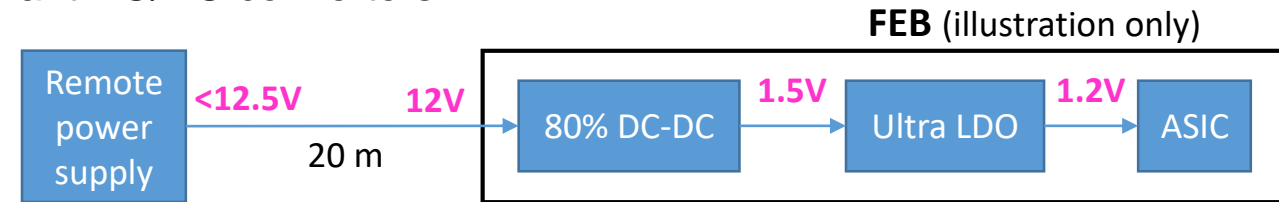
- **Combine FEB (ASIC) data belonging to the same revolution**
 - If needed, heartbeat (RevTick) acknowledgement is sent after the last data belonging to the same revolution
 - Revolution-level granularity might be handy for fragment building in RDO and in DAM
 - A compromise between memory requirement and aggregation
 - If too long, data fragments can be sent in a succession of packets
- **DAM performs revolution record building based on revolution numbers embedded in data**
 - Heartbeat packet can be used as indication that no more data is expected from RDO or FEB for this revolution
- **In other words, consider the RevTick as a 78.195 kHz constant rate trigger**
 - Do classical event building in RDO and DAM with a readout window of $\sim 12.7886 \mu\text{s}$



- A “Calib” request results in a window readout
 - N consecutive samples
 - Full readout of non-ZS data
 - All channels of all ASICs in concerned FEBs
 - Window size programmable
- “Calib” command distributed in barrel shifter mode
 - Only to a predefined FEBs to avoid data congestion
- A special “TestPulse” command to fire on FEB pulser
 - Read ASIC response to know charge



- Powering fronted electronics in ~ 2 T magnetic field is a challenge task
 - Efficient scheme requires on-board magnetic field tolerant DC/DC converters
 - Coupled with ultra low drop-out (LDO) linear regulators
 - Avoids significant power dissipation in LV cables



- 256-channel FEB with a bidirectional 4-lane FireFly optical interface : 9 W or 35 mW / channel
 - LV wire cross-section : 1 mm²
 - NB : In absence of DC-DC converters, LDO-based power distribution will require 5.5 mm² wires

- Estimates of MPGD sub-detector power needs

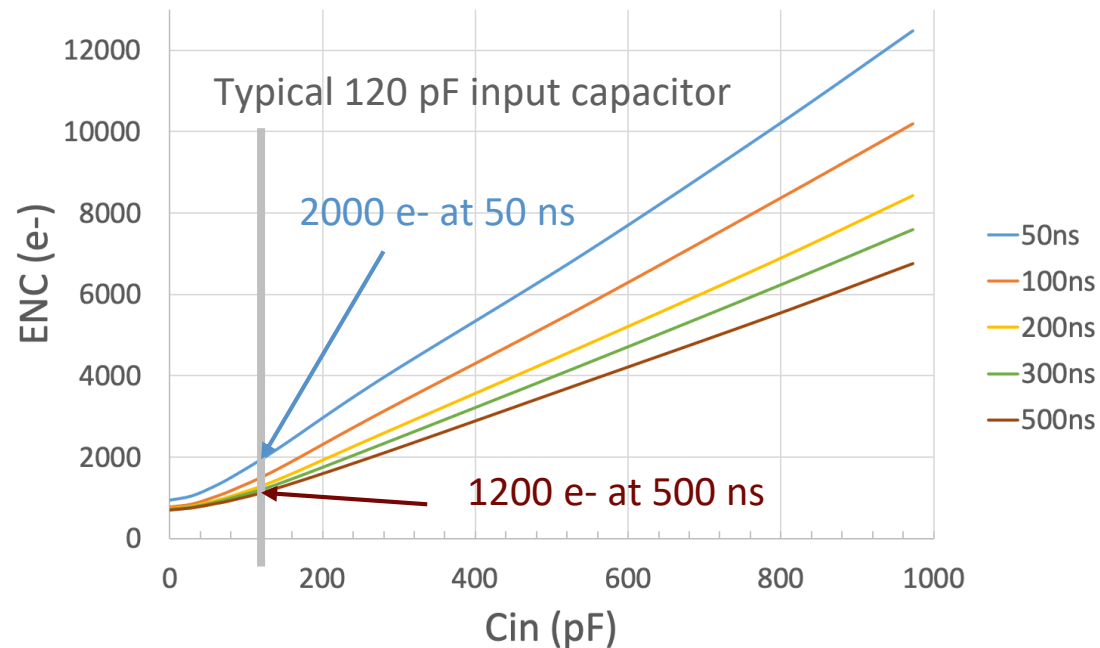
	CyMBaL		μ RWell-BOT		μ RWell-ECT		Total
	Tile	Sub-detector	Module	Sub-detector	$\frac{1}{2}$ disk	Sub-detector	MPGDs
Power(W)	36	1.2k	144	3.5k	144	1.2k	6k

- Engaging common intra- and extra-MPGD efforts to devise power distribution and cooling infrastructure
 - Profit from expertise available within the Project in small form factor magnetic field tolerant DC-DC converters

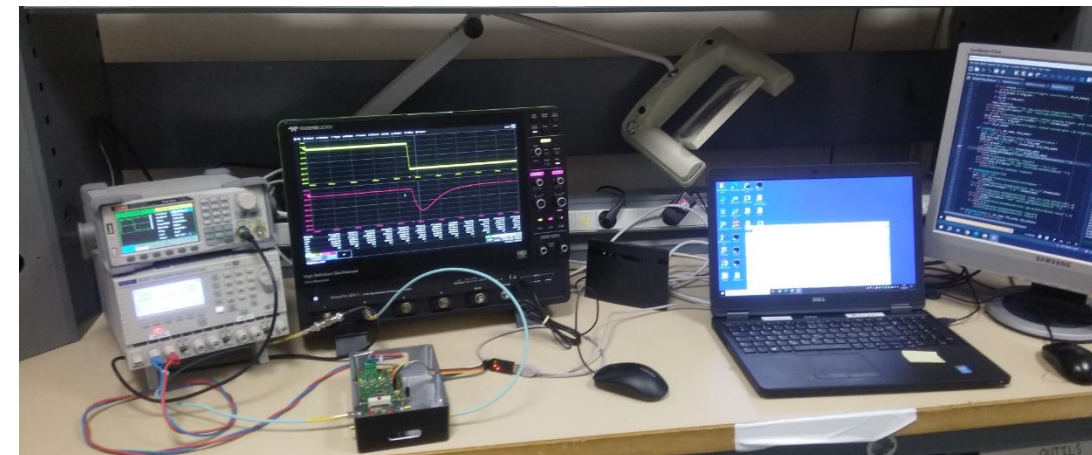
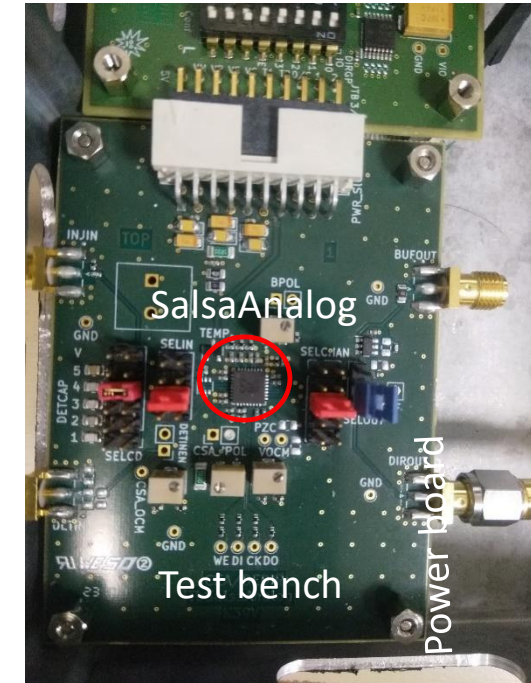
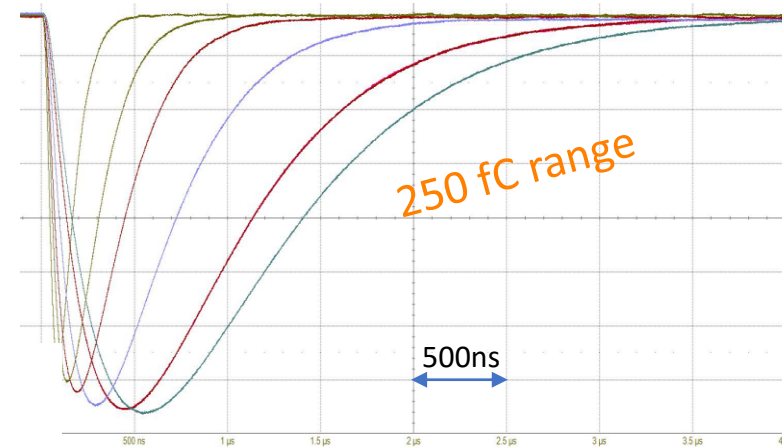
- Prototype ASIC with 4 channels

- 4 dynamic ranges : 50 fC, 250 fC, 500 fC, 5 pC
- 10 peaking times : from 50 ns to 500 ns
- Support for high input capacitances
- Both signal polarities

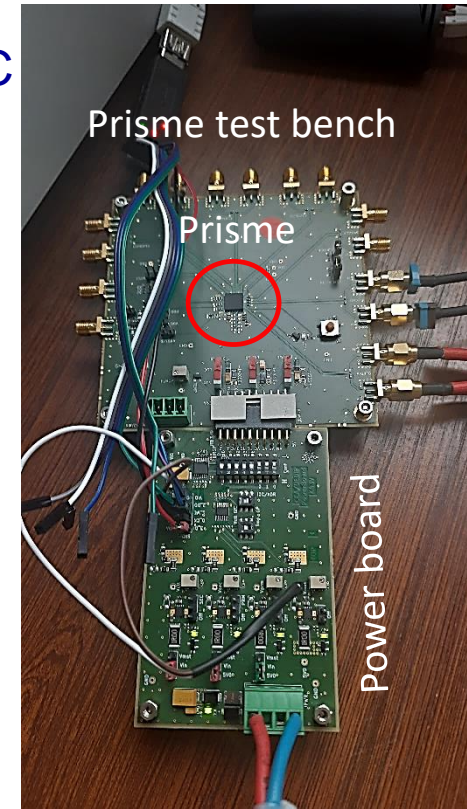
Equivalent Noise Charge in 250 fC range



Programmable Peaking time 50 ns to 500 ns



- Prisme prototype to test a new 65 nm hybrid PLL IP for Salsa and high fidelity fan-out ASIC
 - Large input frequency range
 - 4 clock outputs with programmable frequencies and phase
- Test boards arrived end of February
 - Test bench completed clock generator, high-end 80 GS/S scope and phase noise analyzer
- Preliminary results
 - Power consumption nominal
 - I2C working to read and write registers
 - Low voltage differential (CLPS) receivers and transmitters operational
 - Digital branch of PLL operational
 - Allows to find the right frequency range for the analog branch
 - Internal oscillator reaches nominal 3.2 GHz
 - Locks occur for 40 MHz and 100 MHz input
 - All for outputs tested with programmable frequencies
 - Ongoing tests on jitter characterization and optimization



- Salsa

- 2024 : Salsa1
 - Several fully instrumented channels including analog very fronted and 12-bit MSPS ADC
 - Clock management circuitry based on Prisme IP
- 2025 : Salsa2
 - A 32-channel prototype with main DSP functionalities and serial link interfaces targeting final packaging
 - Prototyping of unified backend interface based on a serial link
- 2026 : Salsa pre-series
 - A 64-channel fully functional prototype
- 2027 : Mass production

- FEB

- 2024-2025 : small prototype developments
 - Assessment of COTS components – e.g. power and monitoring solutions for radiation and magnetic field environment
 - R&D on detector – FEB interface connectors
 - FEB form factor and Salsa integration studies for different MPGDs
 - Validation of unified interface with ASICs
- 2026 : advanced prototype development
 - Based on Salsa2
- 2027 : Pre-series production
 - Based on pre-series Salsa
- 2028 : Mass production

- RDO

- 2024 – 2025 : FEB – RDO interface specification and validation, plus adaptation hardware design
- 2026 : FEB-RDO communication validation based on Salsa2 prototype systems
- 2027 : RDO production

- Services

- 2024 : Identify clearly keep-in-out zones
- 2025 : Validate LV distribution & come out with cooling scheme, plus interlocks
 - Profit from rich expertise within the ePIC groups on magnetic field tolerant DC/DC regulators
- 2026-2027 : production

- System

- 2027 : Fully instrumented slice for every group
 - including FEB prototypes, at least two RDOs and a DAM
- 2028 : Full system chain validation
 - Including slow control and monitoring