

On the use of VTRX+ in ePIC CYMBAL tracker

Cylindric Micromegas Barrel Layer

Irakli Mandjavidze

*Irfu, CEA Saclay
Gif-sur-Yvette, 91191
France*

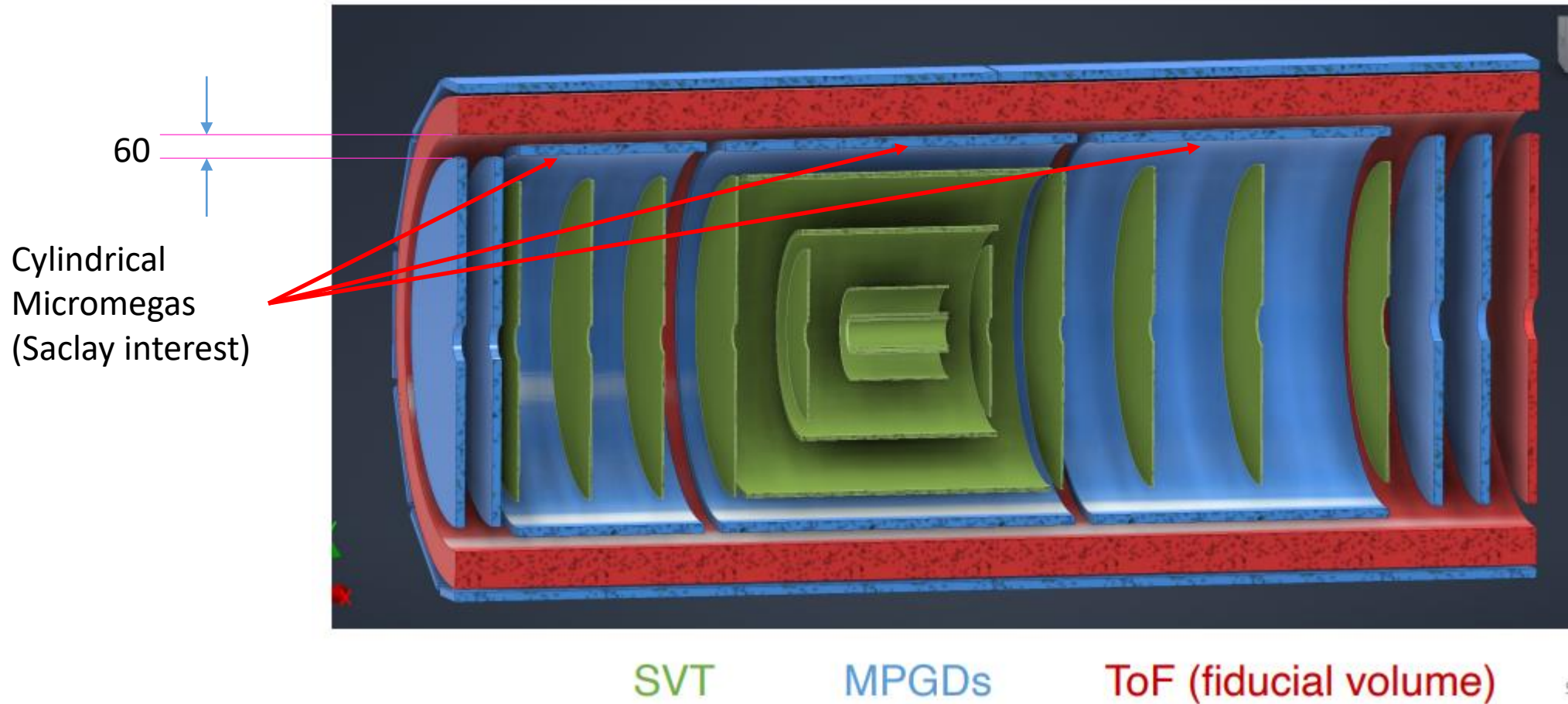
9/Oct/2023

- CyMBaL tracker VTRX+ needs based on the principle “Everybody ran, so I ran too”
 - 170 units
 - ~130 active parts in FEBs deployed on detector
 - ~40 extras for prototyping, pre-series, spares (QA provision)
 - Fragile
- The use of VTRX+ CyMBaL tracker based on system considerations approach
 - Bandwidth considerations
 - Mechanical constraints
 - Functional considerations
 - Power constraints
- In fact, 3 frontend options are studied and compared
 - FEB with electrical RDO interface
 - FEB with VTRX+ optical RDO interface
 - FEB with an “alternative” FireFly optical RDO interface

 - FEB complexity, radiation tolerance and power distribution are considered

Reminder

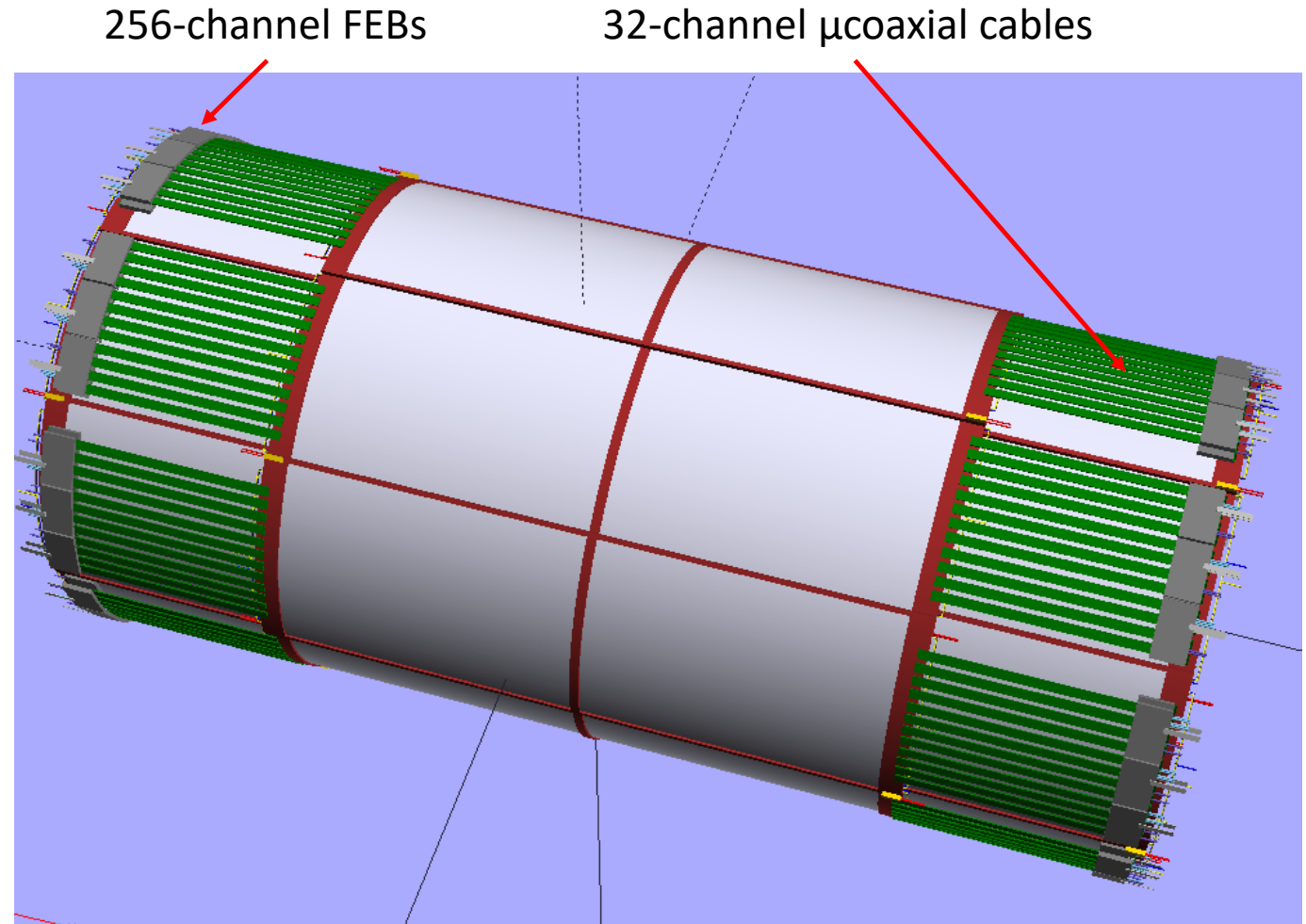
- Space is stringent: 6 cm
→ Detectors, gas pipes, HV cables



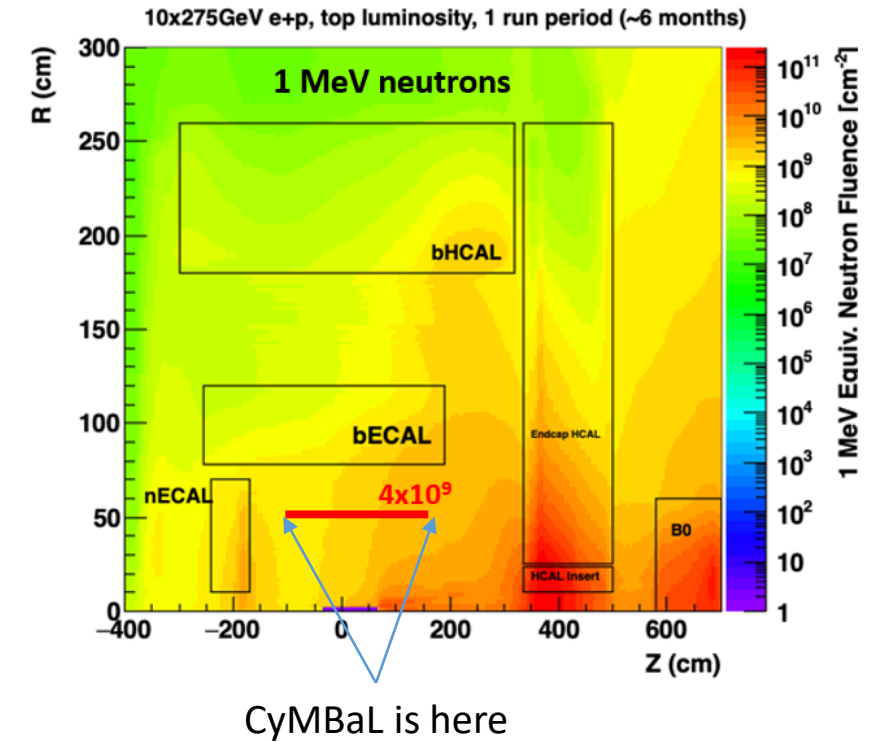
- On detector frontend electronics
→ FEBs + LV distribution + RDO interface cabling + cooling

One of the possible configurations currently under study

- Still under torment of optimization
→ Just a snapshot to give an idea
- 32K channels
- 128 256-channel FEBs
→ Only central detector FEBs visible
 - Peripheral FEBs in a row below
 - Or in a second row
- 32 1024-channel RDOs
- Where to place RDOs not really clear
→ Electrical FEB-RDO interface : 5-6 m
 - 16 on either side of Barrel
→ Optical FEB-RDO interface : no limit
 - Attractive option
- This presentation: impact of optical interface
→ Especially under the pressure to decide on the use of VTRX+



- Stringent space
- Restricted material budget including for cooling
- Magnetic field
- Radiation
- Example of CyMBaL tracker environment
 - TID after 10 years : 10 krad
 - Neutron fluence after 10 years: $10^{11} \text{ n}_{\text{eq}} / \text{cm}^2$
 - 20 MeV proton flux: 100 particle / cm^2 / s
 - Magnetic field: 1.9 T



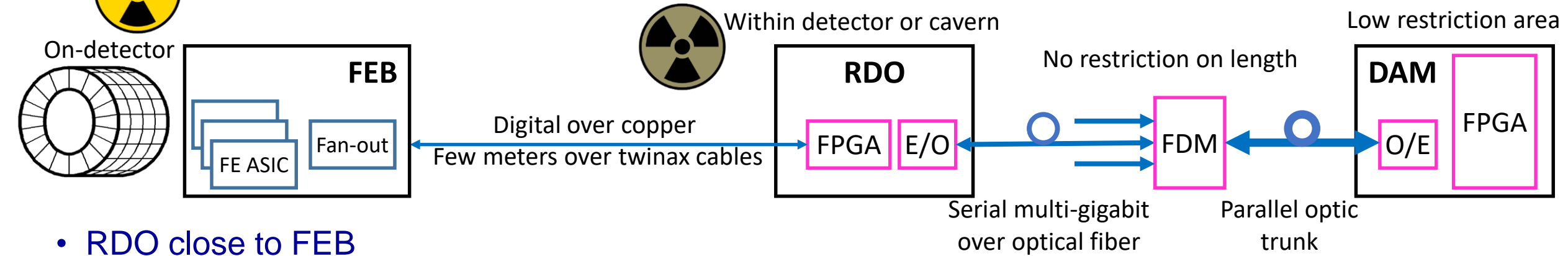
Would be good to have a table with radiation and magnetic field environment of other inner (MPGD) detector frontends

Part 1:

FEB with electrical RDO interface and no on-board intelligence



FEB with no on-board intelligence and electrical interface



- **RDO close to FEB**

→ Moderate radiation environment, space & power stringent

- **RDO ↔ FEB**

- Clock & synch commands – on FEB fan-out or multi-drop
- I2C – daisy chain
- Data – single or several uplinks per ASIC

- **FEB**

- No on-board intelligence, no board-level data aggregation
- High fidelity fan-out candidates: Rafael ASIC or a development based on EICGENR&D_2022_06 [65nm PLL](#)
 - Used solely for clocks and commands; not for I2C

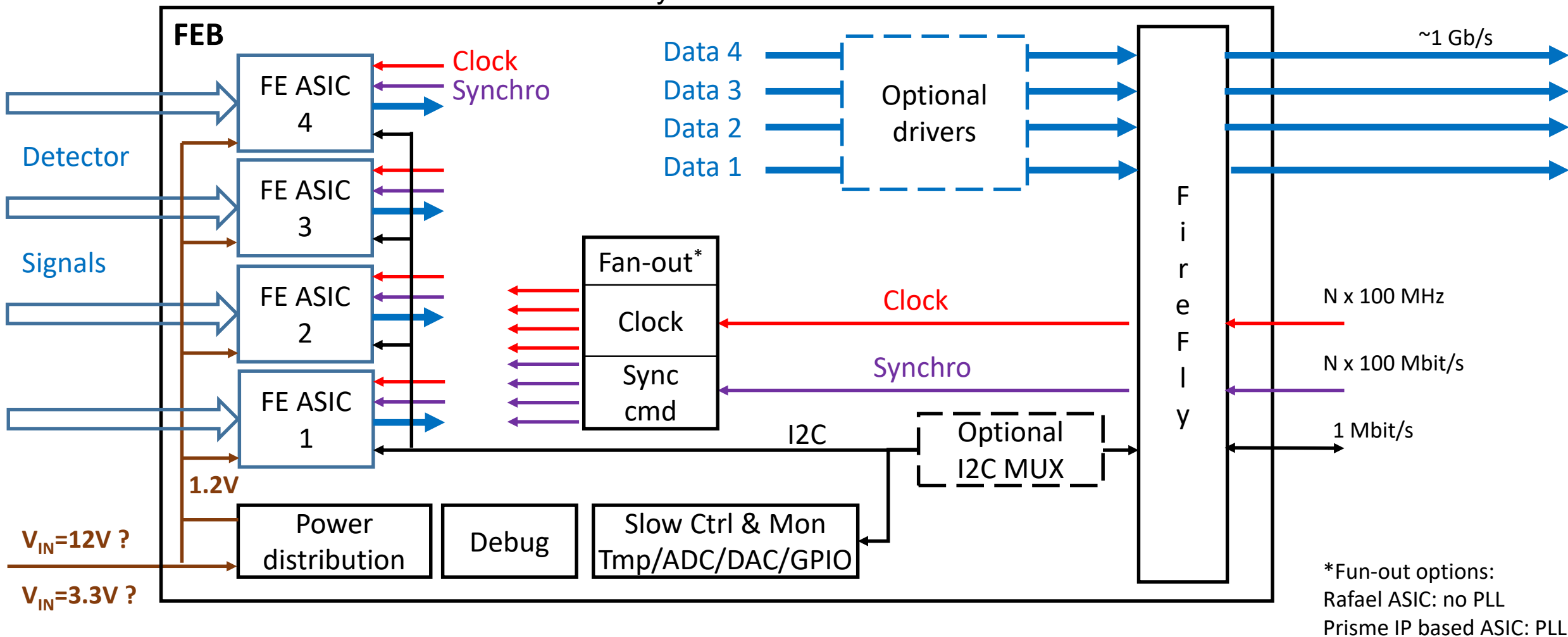


- **On detector FEB: best option for S/N**

→ Difficult for all the rest

- Number of ASICs per FEB can be adapted according to detector modularity and space constraints

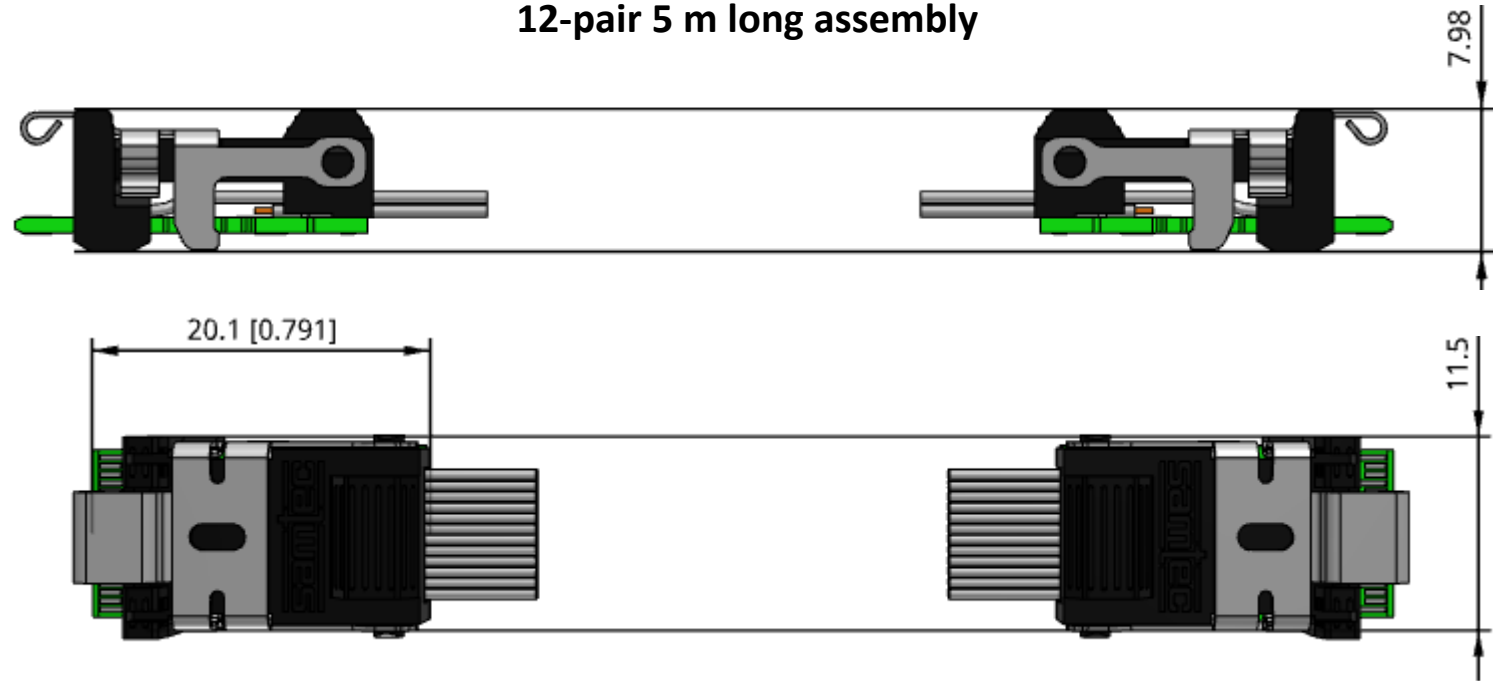
→ As well as lanes of the electrical FireFly interface



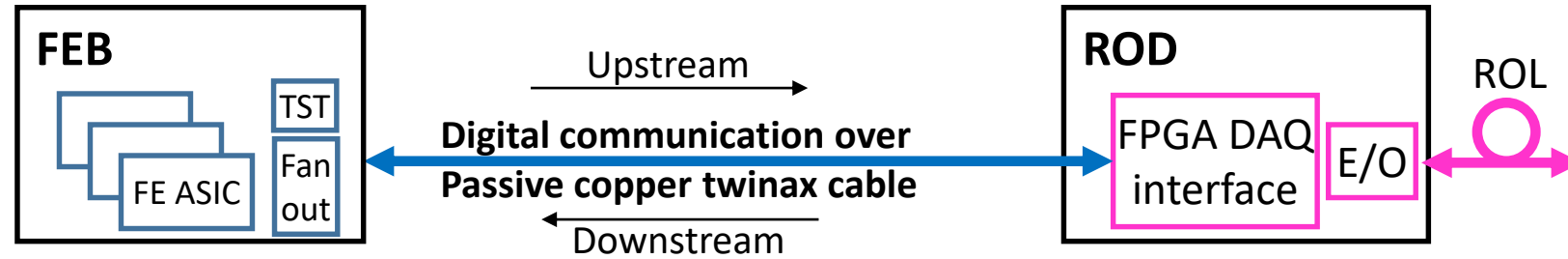
- FEB to RDO distance limited to 5-6 m : where to place RDOs in this range?

- <https://www.samtec.com/products/ecue>
→ https://suddendocs.samtec.com/catalog_english/ecue.pdf
- **Configurable assembly**
 - 8 or 12 pairs
 - up to 10 m
 - Low profile fits stringent space
 - Only 8 mm high
- **Impressive signal integrity figures**
 - Qualified for 10-50 Gbit/s speeds
- **Max length for O(1 Gbit/s) speed?**
 - Are extra drivers needed?
 - Alice MFT: 1Gbit/s over 7-8m
- **Rigidity, weight?**
- **Flammability?**
 - In contact with Samtec technical service
 - R&D on data transmission and on clock / synchronous command distribution?
 - Intention to validate with the PRISME test bench

Example of configured part number: ECUE-12-500-T1-FF-01-1
12-pair 5 m long assembly



FEB-RDO link MPGD example



- 256-channel on-detector FEB

- 4 64-channel FE ASICs (e.g. future SALSA) with
 - 1 Gbit/s output data link
 - Unique system clock line
 - On-board 1-to-4 fan-out
 - Synchronous command line encoding trigger
 - On-board 1-to-4 fan-out
- Bi-directional I2C SDA + unidirectional I2C SDC
 - Chained
- Common on-onboard test pulse logic

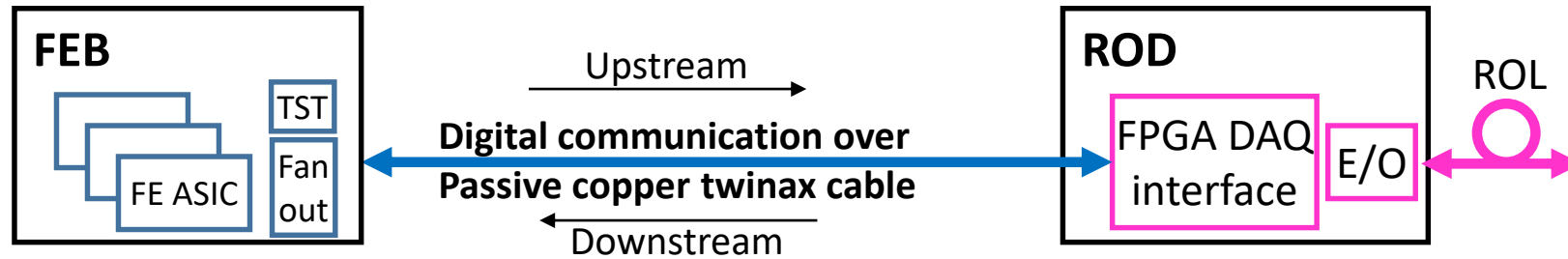
- Off-detector on-detector interface

- 3 downstream lines:
 - Clock, command, I2C SDC
- 1 bi-directional I2C SDA line
- 4 upstream lines
 - 4 data links
- Fits single 8-pair Samtec FireFly copper cable
 - Test sequence may be initiated by I2C over GPIO

- The FEB size (number of channels) to be adapted according to detector segmentation, available space ...

- Example of 512-channel FEB: use 12-lane FireFly
- For other channel counts, some lanes may be ignored

Quick assessment of number of FireFly links for CyMBaL



- 256-channel on-detector FEB
 - 4 64-channel FE ASICs (e.g. future SALSA) with
 - 1 Gbit/s output data link
 - Unique system clock line
 - On-board 1-to-4 fan-out
 - Synchronous command line encoding trigger
 - On-board 1-to-4 fan-out
 - Bi-directional I2C SDA + unidirectional I2C SDC
 - Chained
 - Common on-onboard test pulse logic
- Off-detector on-detector interface
 - 3 downstream lines:
 - Clock, command, I2C SDC
 - 1 bi-directional I2C SDA line
 - 4 upstream lines
 - 4 data links
 - Fits single 8-pair Samtec FireFly copper cable
 - Test sequence may be initiated by I2C over GPIO
- Assume CyMBaL of $4 \eta \times 8 \phi = 32$ detectors of 1024 channels each
- Assume 256-channel FEB : 128 FEBs in total
- Requirement: 128 8-laine 10 mm wide FireFly cables
 - 64 cables distributed over 3 m perimeter on each side of the tracker
 - 1 cm cable every 4.7 cm : kind of fits

- Rafael - Radiation-hArD Fan-out ASIC for Experiments at LHC - developed at Irfu, CEA Saclay

- 3 inputs and 13 outputs

- CLPS signaling

- CM voltage: 0.6 V
- Differential swing: 200-400 mV
- Programmable drive and emphasis

- Single buffer: any input to 13 outputs

- Double buffer

- Input 1 to 6 outputs
- Input 2 to 7 outputs

- Up to 400 MHz and beyond

- Low additive jitter : < 2 ps

- Propagation delay : ~1 ns

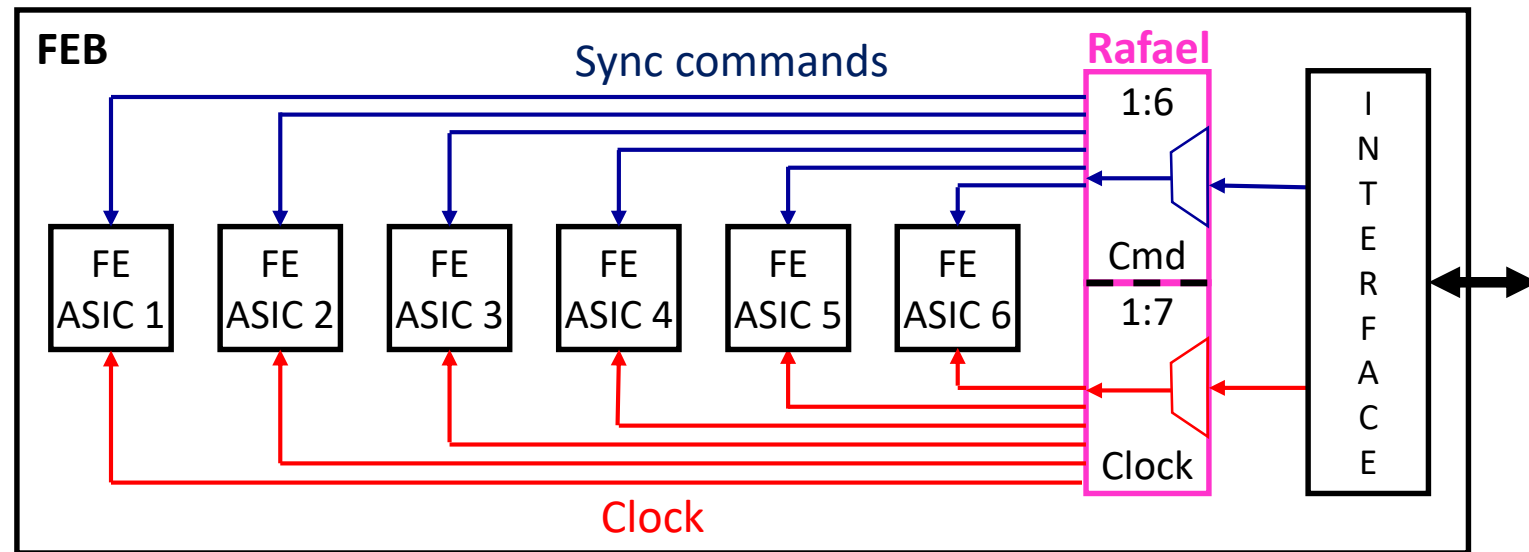
- C2C and P2P skew : < 300 ps

- 130 nm technology

- LHC-level TID, neutron, SEU & latch-up



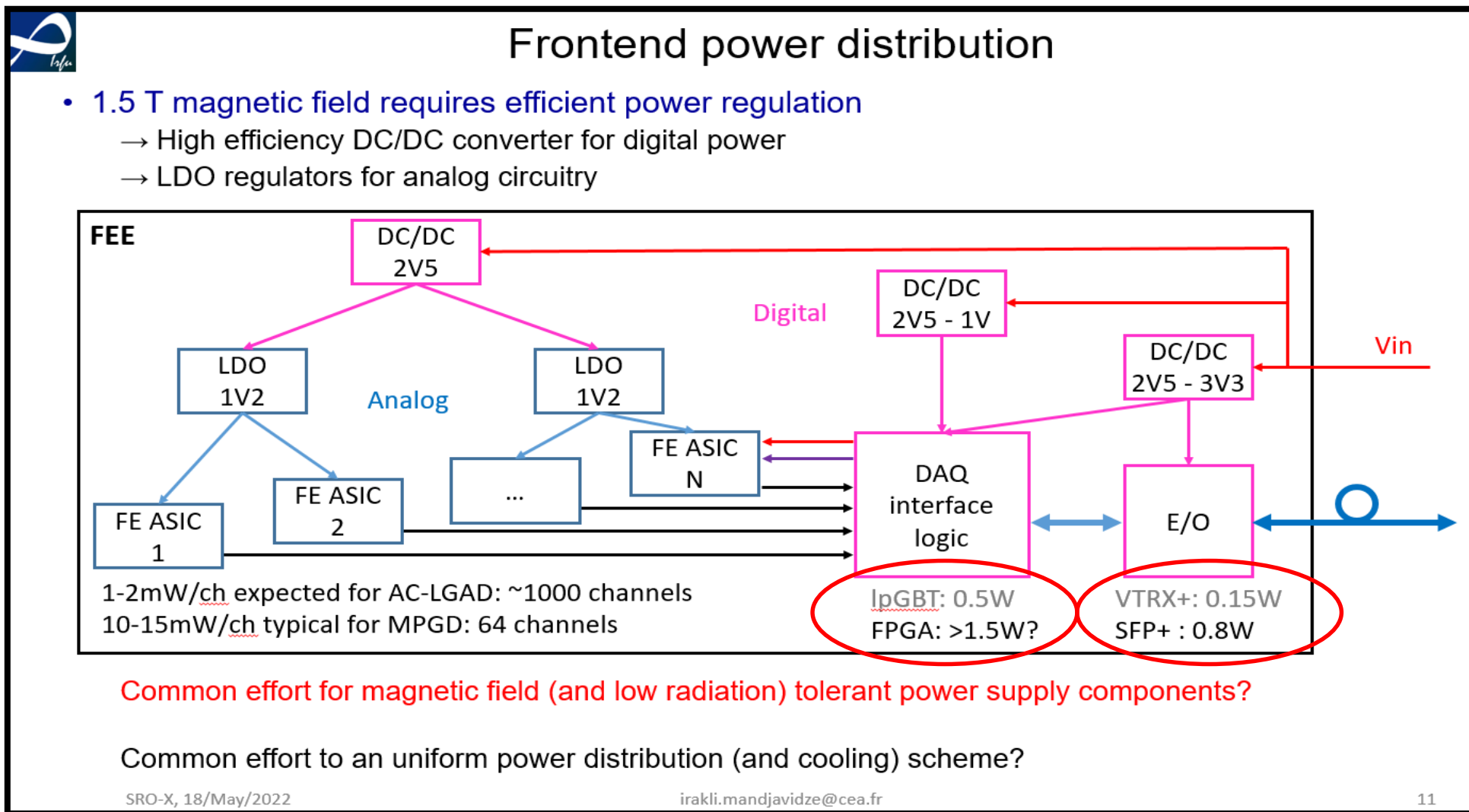
[Rafael](#)



Power distribution: a reminder from the past

- Just for fun: presented on 18 may, 2022, during SRO-X workshop

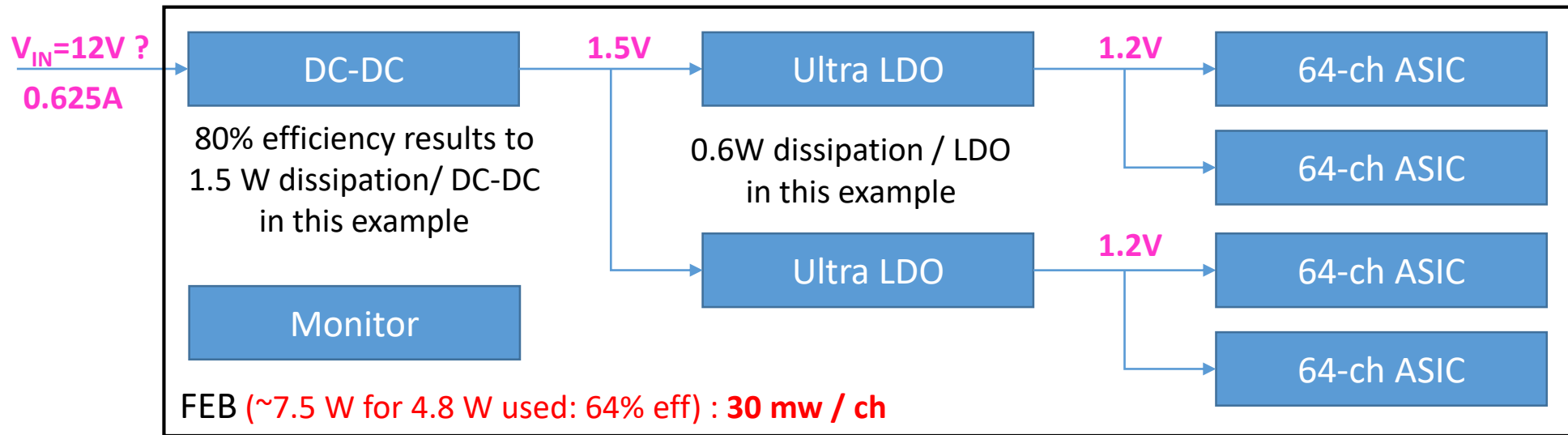
→ https://indico.jlab.org/event/519/contributions/9563/attachments/7748/10855/220518_SroX_FrontEnd_IM.pdf



Powering within magnetic field

- Assuming 64-channel Salsa with ~ 1 W power consumption @ 1.2 V
 - For simplicity, 1 A per ASIC
- Clean power will require a radiation tolerant ultra LDO linear regulator
 - e.g. commercial TPS7H1101A-SP from TI - <https://www.ti.com/product/TPS7H1101A-SP> - space grade
 - e.g. community LDO used for CMS HgCal frontends - <https://cds.cern.ch/record/2797683> - HL LHC grade
 - Or whatever proposed by other subsystems
- Power distribution may require magnetic field tolerant high efficiency DC/DC regulators
 - e.g. community bPOL12V from CERN – HL LHC grade and 4T tolerance
 - [Microsoft Word - bPOL12V V6 datasheet V1.6.docx \(cern.ch\)](#)

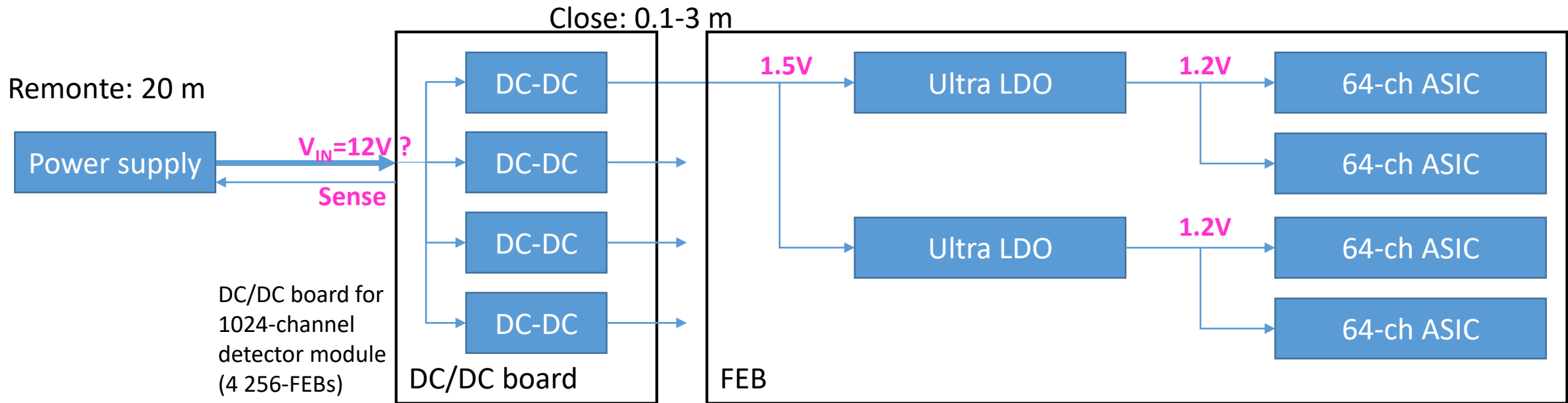
\$1700



- Question: is there a common effort for LV distribution?
 - A centralized group taking care to provide V_{IN} in a “uniform” way wherever possible
 - And in case CERN components will be the choice, for their inventory and procurement

Power distribution: about DC/DC regulators

- The use of magnetic field tolerant DC/DC converters is attractive for efficient powering
- However, they might be bulky
 - One of the designs integrating bPOL12V from CERN requires $\varnothing 12$ mm and H 3mm coils
- And they might be a source of EMC noise requiring a special shielding
 - Extra material budget in the vicinity of trackers if DC/DC converters sit directly on FEBs
- Shall they be placed on dedicated boards not too far from FEBs?

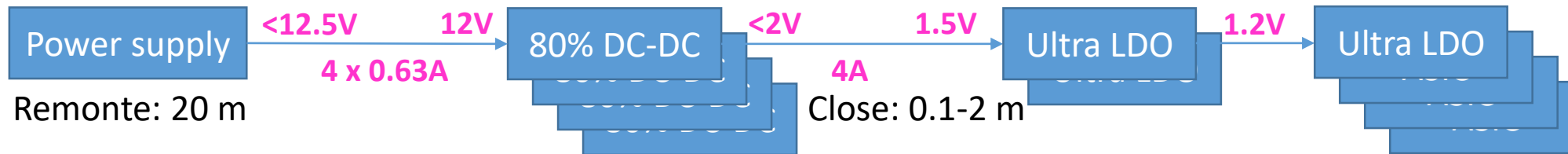


- Next page

- A 256-channel FEB with passive electrical RDO interface consumes 7.5 W

→ With on-board or close-to-board DC-DC converters

- 12V is distributed to DC-DC converters to produce 1.5V for LDOs to produce 1.2V for ASICs



→ Assume DC/DC – LDO connection induces no more than 0.5V drop: DC/DC output set @ 2V

- Power dissipation in wires: $\max 0.5 \times 4 = 2 \text{ W}$: what should be the wire cross-section for a given length?

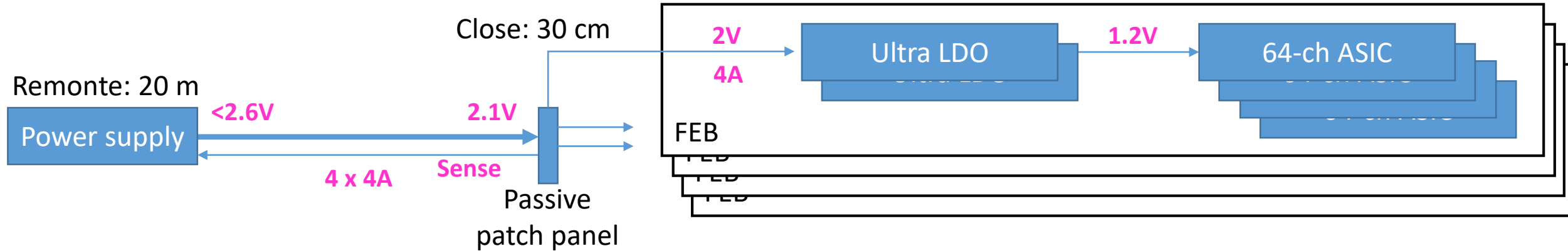
DC-DC to LDO Distance m	Wire cross section mm ²	Comment
0.3	0.1	Not clear if there is a place for DC/DC power board
1	0.3	Noise pickup on 1 m long cables
2	0.6	Not reasonable: usually needs active regulation

- A 1024-channel Module consumes 30W

→ Assume PS – DC/DC connection induces no more than 0.5V drop: PS output set @ 12.5V

→ If PS is 20 m away the cross section of the power wires should be 2 x 3.5 mm²

- If DC-DC converters cannot be placed on FEBs or in a close vicinity, can they be dropped off at all?
→ Low voltage is distributed directly from remote power supply?



- A 256-channel FEB with passive electrical RDO interface consumes 8.4W
→ With DC-DC converter dropped
 - 2.1V is distributed to LDOs to produce 1.2V for ASICs
 - 1.5V distribution with sense wire regulation on a long distance might be problematic; increased to 2.1V
- A 1024-channel detector module consumes 33W
- Assume PS – LDO connection should not induce more than 0.5V drop: PS output set @ 2.6V
→ If PS is 20 m away the cross section of the power wires should be
 - $2 \times 5.5 \text{ mm}^2$ if FEBs are individually powered
 - $2 \times 22 \text{ mm}^2$ if a common power is delivered to a 1024-channel detector module

- Low active component count: minimal power consumption
- Clock and synchronous command distribution via a high fidelity radiation hardened fan-out
 - Rafael : no internal PLL; Exists
 - Prisme : internal PLL with phase adjustment; Under development
- No on board aggregation: ASIC data links interfaced directly with the RDO receivers
- FEB to RDO distance limited to 5-6m
 - Active driver-repeater-buffers can be used to increase the distance
 - Attention should be paid to ground-power return passes and pickup noise
- Expected power consumption of a 256-channel FEB
 - 7.5 W with on-board or closely coupled DC/DC : 30 mW / channel
 - 3.5 mm² wires would be appropriate to distribute required power to entire 1024-channel detector module
 - Location of the magnetic field tolerant bulky DC/DC converters will most probably be problematic
 - 8.4 W without DC/DC regulators : 33 mW / channel
 - !!! 5.5 mm² if FEBs are individually powered
 - !!! 22 mm² if a common power is delivered to a 1024-channel detector module

Part 2: FEB with VRTX+ optical RDO interface

Bandwidth considerations

- Physics: zero suppression

- Case 1: Sampling readout

- 500 ns readout window when signal is above threshold
 - 50 MSPS
 - 12-bits per sample, 50 MSPS, 25 samples

- Case 2: Peak-finding readout

- 12-bit amplitude, 12-bit time of max, 8-bit ToT

- Calibration : on demand non ZS readout

- Possible scenario

- Calibration data requested every 100 Hz
 - 50 consecutive sample readout
 - 50 x 1000 samples per channel

- Data volume determined by physics

- Calibration can even be done regularly on-line

- Still background generated data has to be taken into account

- Hens safety factor of 5

Estimated **physics** data bandwidth per ASIC

Channel rate kHz		Sampling Mbit/s	Amplitude - Time Mbit/s
2	(physics)	53	8.2
10	(safety)	264	41
50	(Clas12)	1 318	205

Estimated **calibration** data bandwidth per ASIC
~6 Mbit/s

A 256-channel FEB data

- Estimated physics data bandwidth per 256-channel FEB
- Data volume determined by physics
 - Calibration can even be done regularly on-line
- Background generated data has to be taken into account
 - Hens safety factor of 5

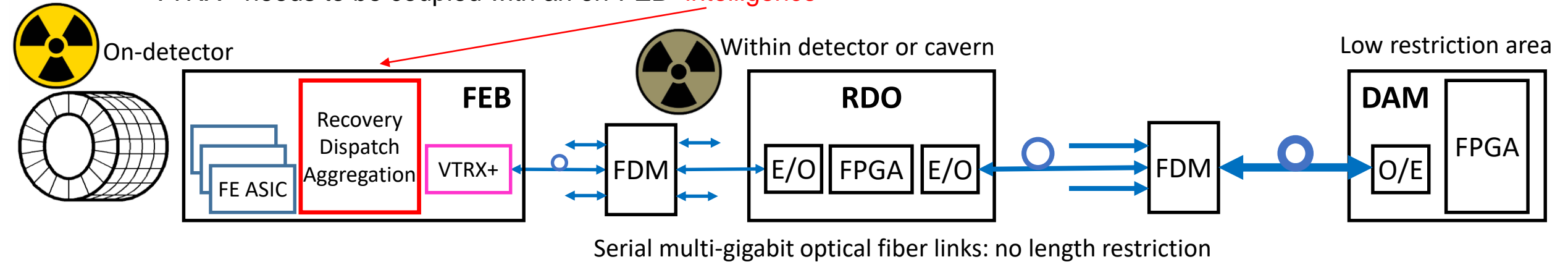
Channel rate kHz		Sampling Mbit/s	Amplitude - Time Mbit/s
2	(physics)	200	40
10	(safety)	1 200	200
50	(Clas12)	5 500	900

- VTRX+:
 - Single 5-10 Gbit/s Tx link seems to be enough
 - Others might be used for commodity
 - see later
 - The 2.5 Gbit/s Rx link is more than enough to
 - Recover good quality clock
 - Pass synchronous commands
 - Pass slow control I2C asynchronous commands
- In term of data bandwidth the use of VTRX+ in CyMBaL application seems to be an overkill
 - One needs to aggregate 66.6 64-channel ASICs (4k channels) to load VTRX+ at 50% (20 Gbit/s): simply impractical
 - 1 VTRX = 1/8 of the entire CyMBaL
 - The low profile and radiation hardness are the driving pros
 - Low consumption is certainly compelling but needs to be considered from system point of view

Some mechanical constraints

- Off-detector RDO

- VTRX+ is on FEB; COTS optical transceiver on RDO
- VTRX+ needs to be coupled with an on-FEB “intelligence”



- On-FEB local “intelligence”

- Recover clock
- Separate downstream data in synchronous and asynchronous commands
 - Clock synchronous commands for run control
 - Asynchronous commands for slow control and monitoring – e.g. I2C
- Dispatch downstream data to FE ASICs
- Aggregate data from FE ASICs
 - Physics, control, monitoring

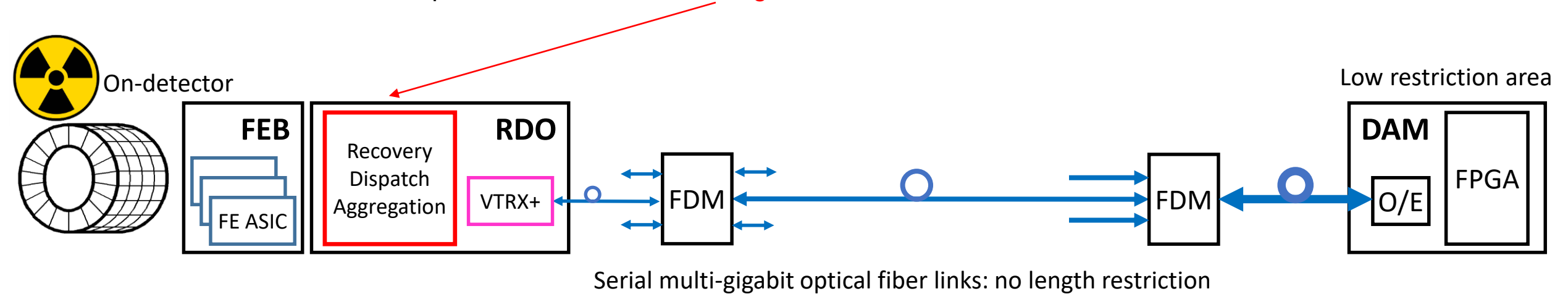
FDM – fiber distribution module
(patch panels, etc.)

- IpGBT@CERN: radiation hard, low power, low price and common to all subsystems

What is or can be EIC/ePIC substitution for IpGBT?

Potential use of VTRX+: on RDO

- On-detector RDO or close to detector RDO in a radiation vicinity
 - VTRX+ is on RDO; COTS optical transceiver on DAM
 - VTRX+ needs to be coupled with an on-RDO “intelligence”



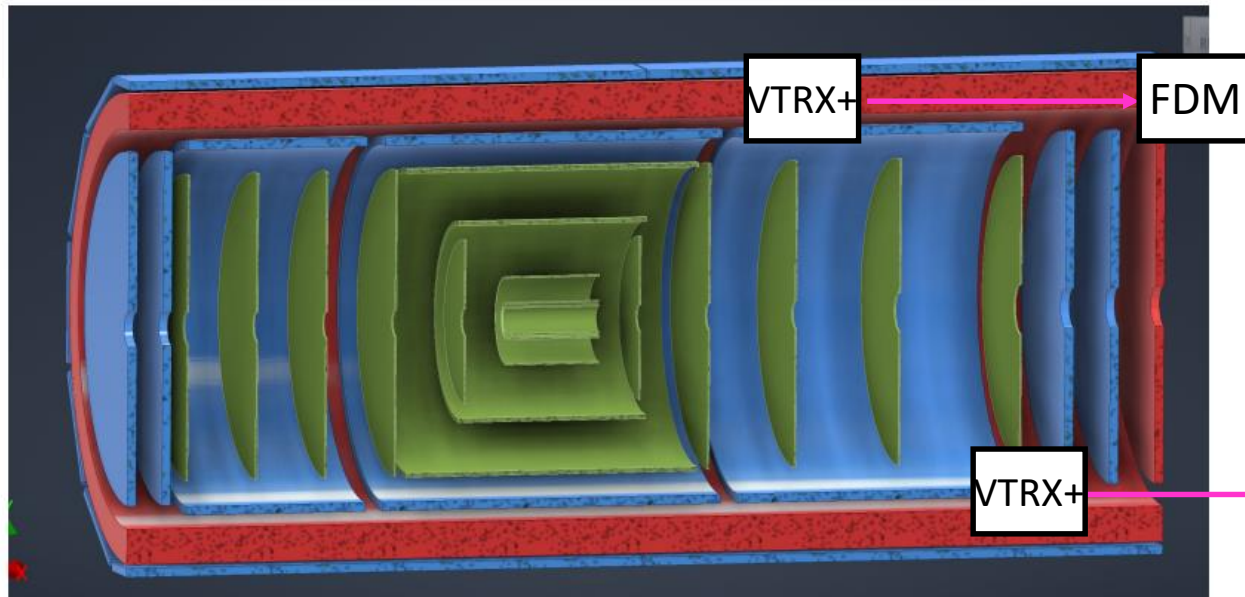
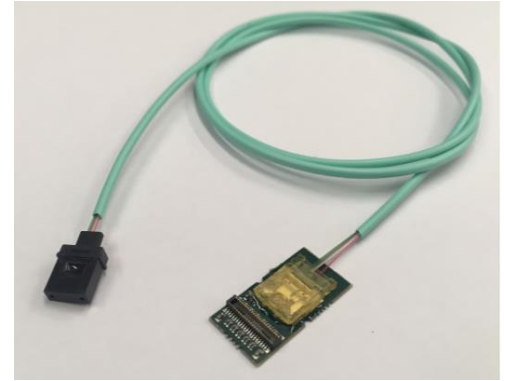
- On RDO local “intelligence”
 - Exactly the same functionality: recover, dispatch, aggregate

- And the same question

What is or can be EIC/ePIC substitution for IpGBT?

FDM – fiber distribution module
(patch panels, etc.)

- VTRX+ comes with a fiber optic pigtail
 - Limited to 20 cm – 1 m range
 - From 5 to 10 discrete lengths yet to be defined
- The first optical patch panel has to be close to FEB/RDO,
 - One needs to understand if the CERN “standard” VTRX+ pigtail lengths are suitable
 - Or if it can be produced with a special “EIC length”
 - And if the reshuffling (or jumper) devices can fit sub-detector space constraints



How bulky the **Fiber Distribution Module** can be?
Just a passive pass-through ?



In quantities, even low profile devices may fill quite some space

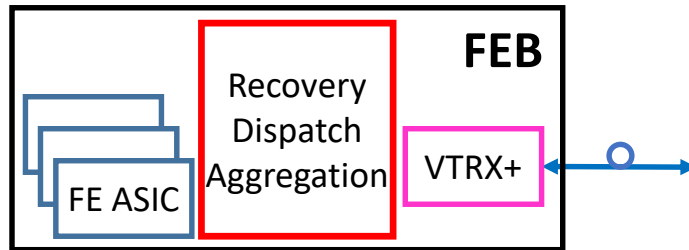
A reshuffle to regroup RXs and TXs?



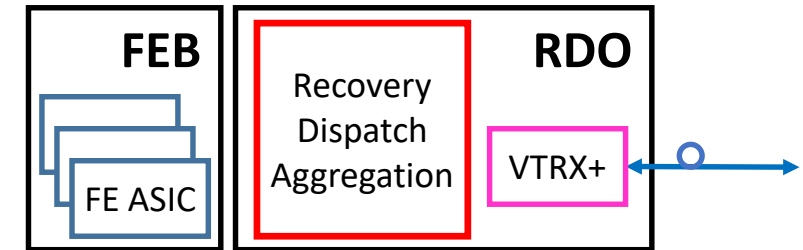
- Need to understand mechanical constraints to decide on pigtail length
 - To stuff extra length of fiber may take surprisingly big volume, especially with a bending radius to respect

Functional constraints

On-detector FEB / Remote RDO option



On-detector FEB / RDO option



- VTRX+ requires an on-board intelligence
- CyMBaL frontends may need, at most, space grade radiation tolerant components
 - Prices may be 10-100 time higher compared to COTS equivalents
- CyMBaL frontends operate in a high magnetic field
 - Can be an obstacle for efficient powering
- Assume IpGBT equivalent functionality is implemented on a radiation tolerant FPGA
 - What will be the consequences of coupling of VTRX+ with a radiation hardened FPGA ?

Does CyMBaL tracker need a rad tolerant FPGA ?

- Remainder of radiation environment

- TID after 10 years : 10 krad ✓ - no problem
- Neutron fluence after 10 years: $10^{11} \text{ n}_{\text{eq}} / \text{cm}^2$? - SEU
 - Flux: $300 \text{ n}_{\text{eq}} / \text{cm}^2 / \text{s}$
- 20 MeV proton flux: 100 particle / cm^2 / s ? – Latch-up

- Xilinx SEU estimator

→ Pretend results for Artix UltraScale+ AU10P are valid for AU7P device (smallest device in the family)

SEU type	1 device	128 devices
	Hours / error	Minutes / error
25 Mbit config RAM	68	30
100% of block RAMs	128	60
All	44	20

→ Uncertainty from estimator : 10-40 min between errors for 128 devices of CyMBaL

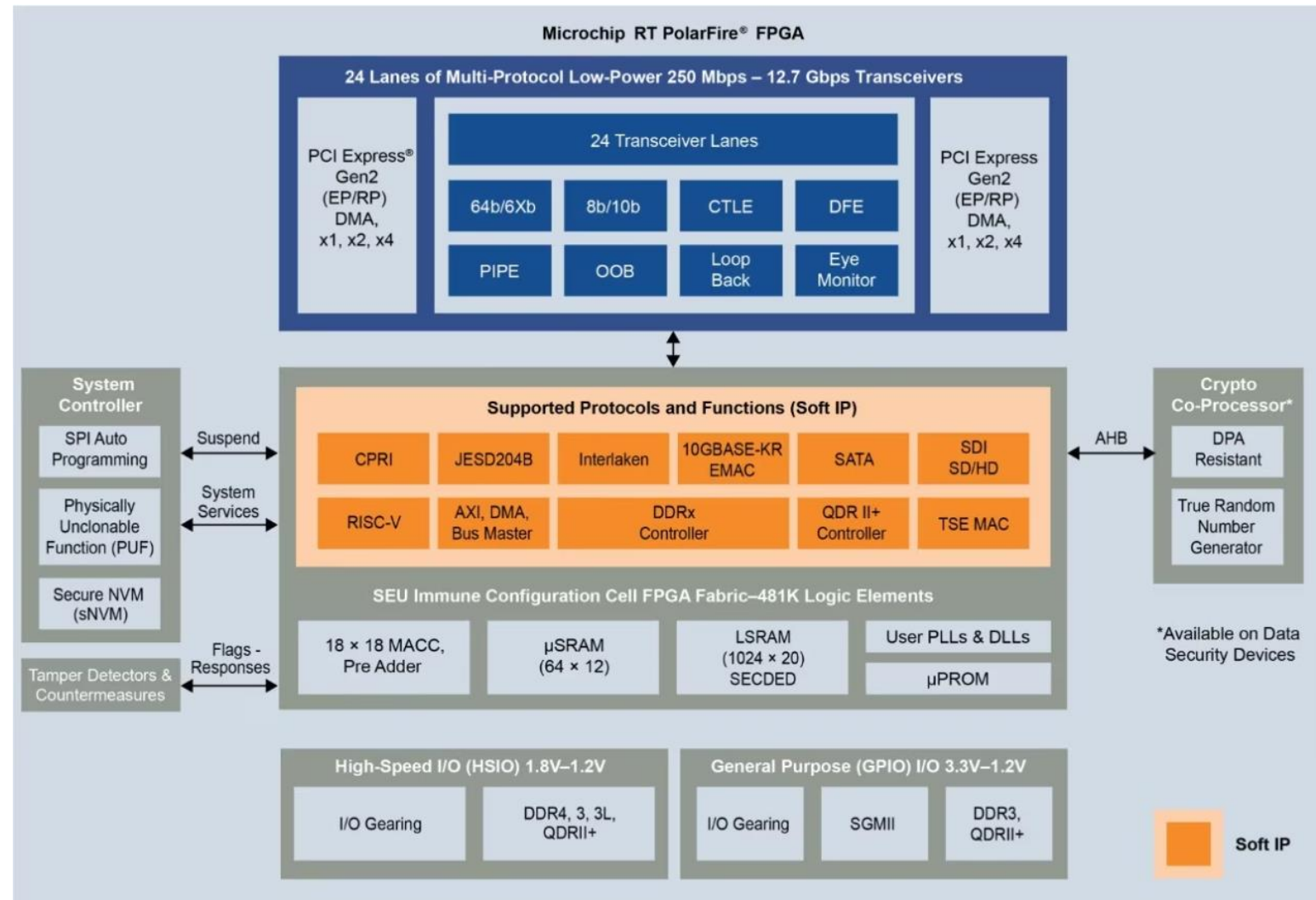
→ MTBF seems low

- What can be mitigated to increase MTBF ?
- What about other sub-detectors ?

- Assume IpGBT equivalent functionality is implemented on a radiation tolerant FPGA
 - What will be the consequences of coupling of VTRX+ with a radiation hardened FPGA ?
- Candidate : RT PolarFire® FPGAs from Microchip
 - Radiation tolerant device type RTPF500Txx in the family
 - 100 Krad
 - Single-Event Latch-Up > 60 MeV.cm²/mg
 - No configuration upsets
 - Data upset rate better than 10⁻¹⁰ errors/bit-day with fault-tolerant design techniques
 - Presumably the reference to be used is **RTPF500TL** – low static power variant

- A middle to high-end FPGA with considerable capabilities

- 481 000 LEs
- 33 Mb embedded SRAM
- 1 480 multipliers
- 632 user IOs
- 24 10 Gb/s transceivers
 - Cost !
- 40 mm x 40 mm 1500-ball package
 - Complexity of board !
- What will be the unit cost ?
 - Its weight on frontend cost ?
 - One will need to pay for
- Need to get an offer
 - To compare with say Artix US+ AU7P : \$200
- Meanwhile one can guess :
 - Development kit for \$20 000 !

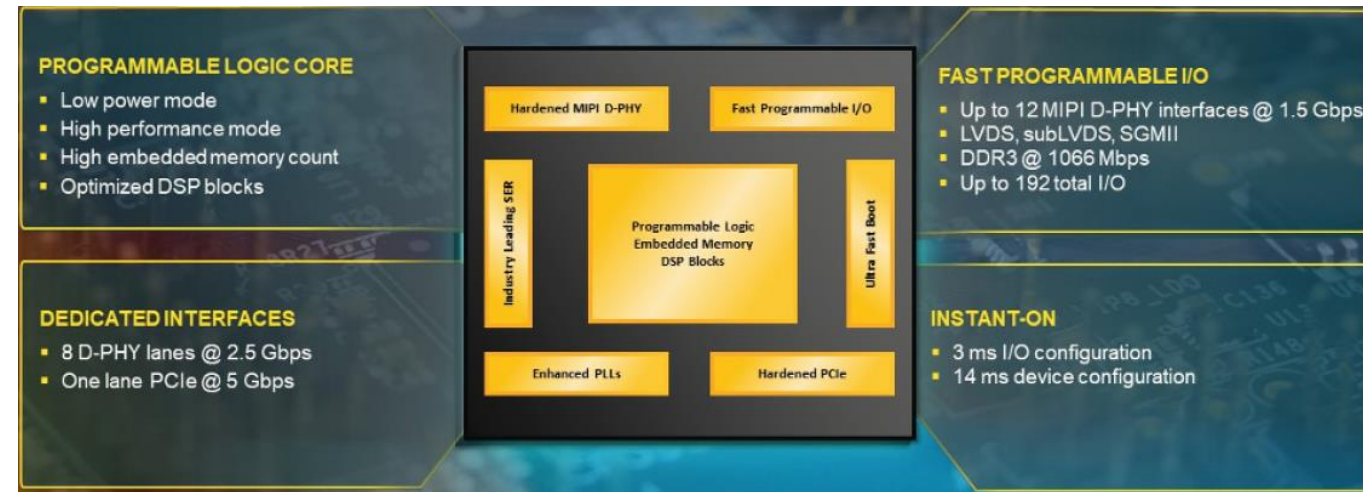


Kind of a “Monster” FPGA compared to frontend needs

- A frontend based on MPF300T PolarFire® FPGA has been reported (equivalent of RDO)
 - https://cds.cern.ch/record/2797780/files/CR2019_207.pdf
 - 16 W for 240 channel : **66 mW / ch**
 - Certainly due to the (forced?) use of LDO regulators
 - €380 in CyMBaL quantities and €210 in quantities above 1000 units
- Smaller brother MPF50TL device – low power grade
 - €120 in CyMBaL quantities and €70 in quantities above 1000 units
 - 48K logic elements
 - Total RAM 3.6 Mbits
 - DLL/PLL 8
 - 4 SERDES lanes
 - 2 PCIe endpoints
 - 176 User I/O
 - 11 mm x 14.5 mm package
 - **Unfortunately not in the datasheet !**
- One may check MPF100TL
 - €230 in CyMBaL quantities and €130 in quantities above 1000 units
- Are they radiation tolerant ?
 - **Excellent recent radiation study:**
 - https://indico.cern.ch/event/1127562/contributions/5028230/attachments/2513165/4320151/DT_twepp_CHARM.pdf
 - To be understood for CyMBaL environment but should certainly be OK

- Radiation hardened LIFCL-40-9BGA400 device from CrossLink-NX family

- 39 000 LEs
- 2.5 Mb embedded SRAM
- 56 multipliers
- 191 user IOs
 - Supports 1.2V
- 2 built-in ADCs
 - Monitoring
- 8 lanes of 2.5 Gb/s hard PHYs
 - Can be set as either transmitter or receiver
- 1 lane of 5 Gbit/s
- 17 mm x 17 mm 400-ball package
 - Compact
- Cost **\$65**
 - Development kit **\$120**



Raw SEU rates with no correction in CyMBaL radiation environment

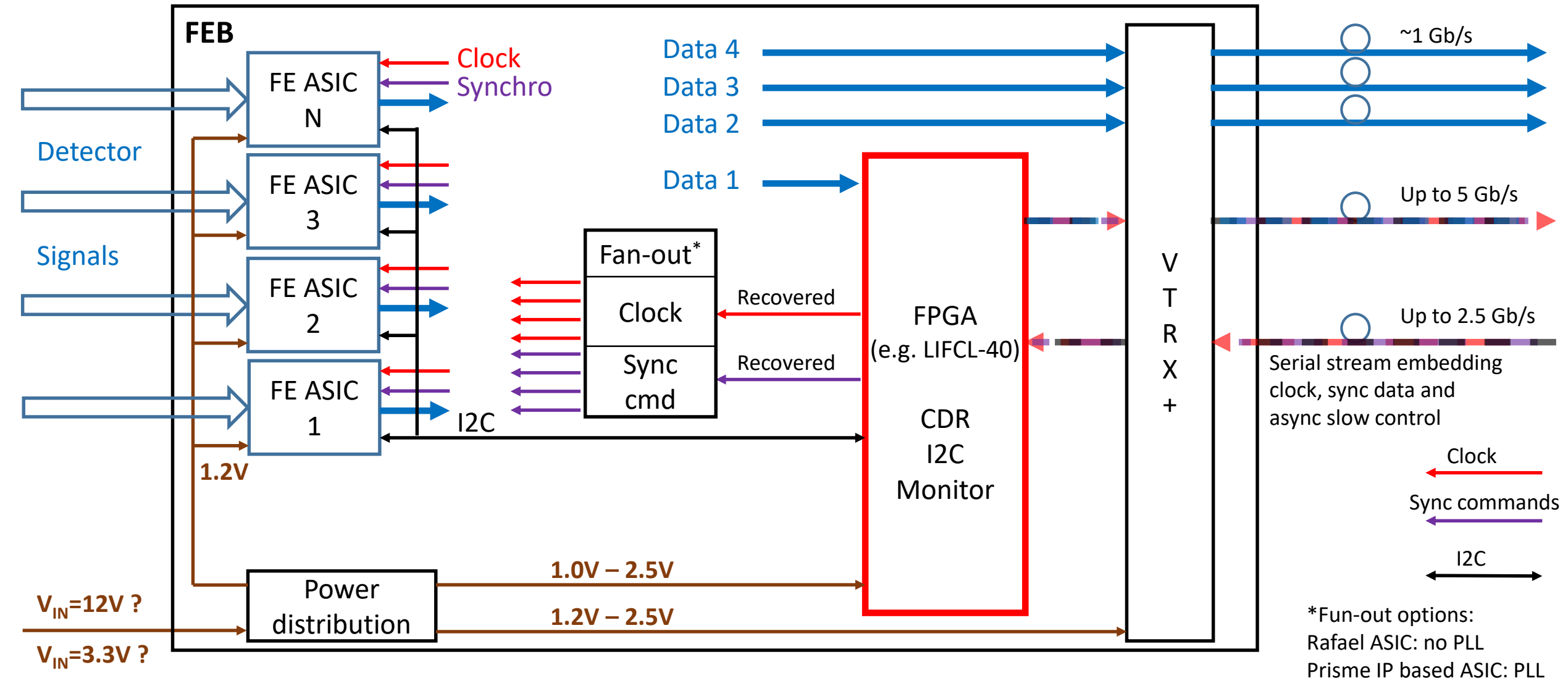
SEU type	1 device	128 devices
	Day / error	Hour / error
6.3 Mbit config RAM	20	3h 35m
1.5 Mb RAMs	40	7h 17m
All	13	2h 25m

MTBF of a 128-device system with embedded SEU corrections:
8h 15m

A pale copy of IpGBT with a low cost rad hard FPGA ?

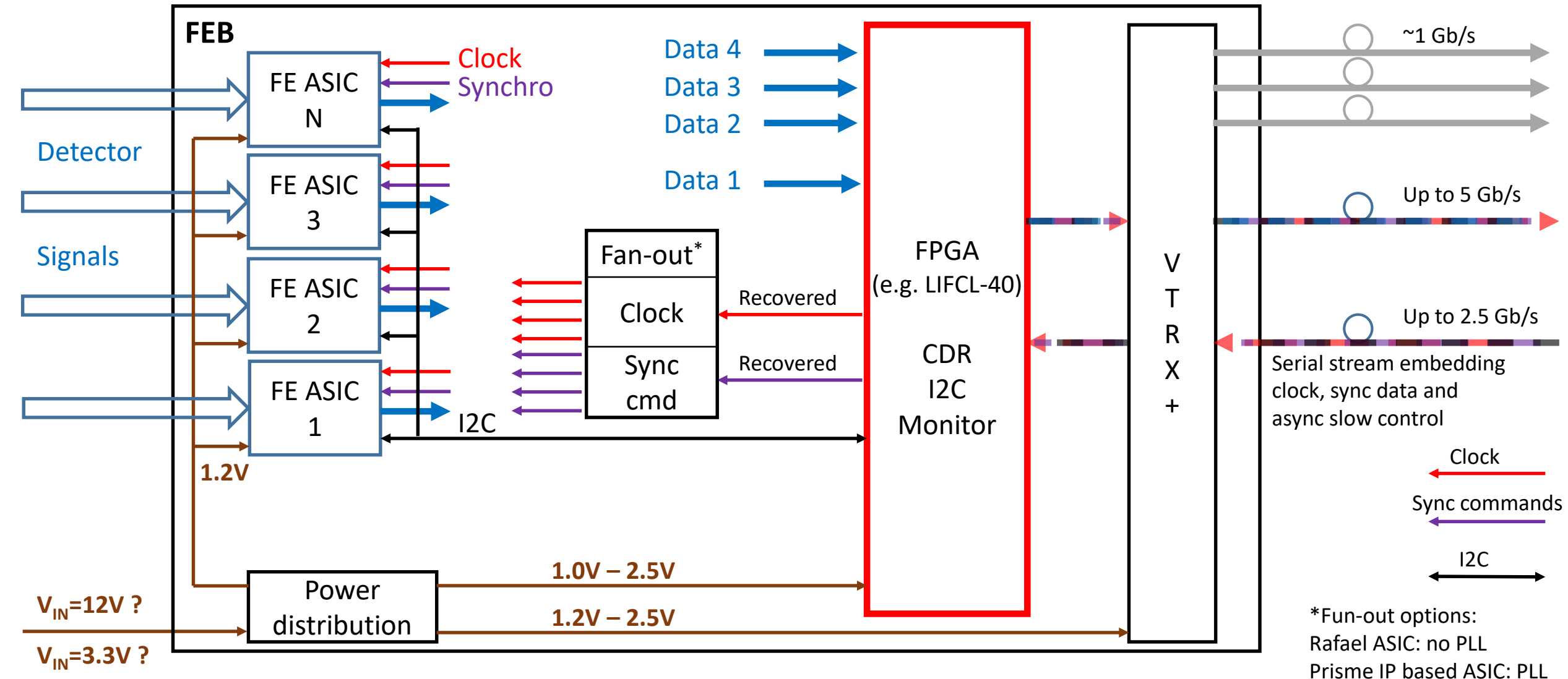
- Implement a subset of IpGBT functionality

→ Use rad hard fan-out ASIC to distribute clock and sync commands to FE ASICs



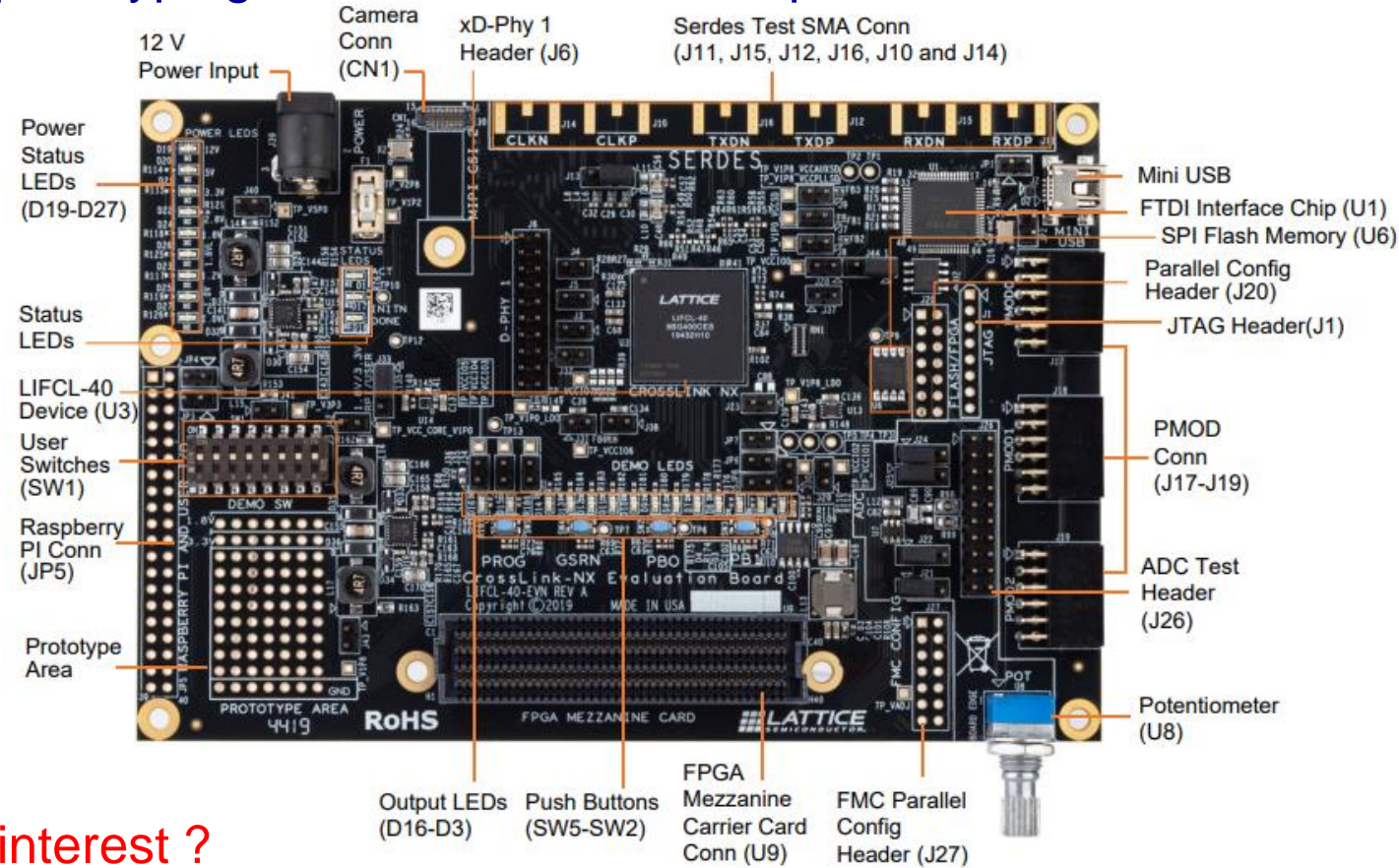
A pale copy of IpGBT with a low cost rad hard FPGA ?

- Option for low occupancy regions with data aggregation on a single optical link
→ Reference designs exist for control and aggregation of data from multiple cameras



A pale copy of IpGBT with a low cost rad hard FPGA ?

- A more serious “paper” study is needed to understand feasibility
 - Resource and power budget evaluation
- If more-than-PowerPoint-concept is fine, prototyping can start with a development kit
 - Interfacing with VTRX+
 - Clock-data recovery
 - Clock quality ?
 - Data aggregation
 - I2C slow control
 - €120 for LIFCL-40-EVN
 - Plus software license, presumably
 - But I could download a free version
- Does such R&D represent an ePIC-wide interest ?
 - A dedicated group for a common design ?



Power constraints

- Guess for Lattice LIFCL-40-9BGA400 FPGA power rails : inspired from evaluation kit design

→ Core:	1.0V – 800 mA	0.8 W
→ Analog VCC for SER-DES:	1.0V – 200 mA	0.2 W
→ Digital VCC for SER-DES, ADC, VCCAUX:	1.8V – 300 mA	0.6 W
→ IO VCC:	1.2V – 250 mA	0.3 W

- VTRX+

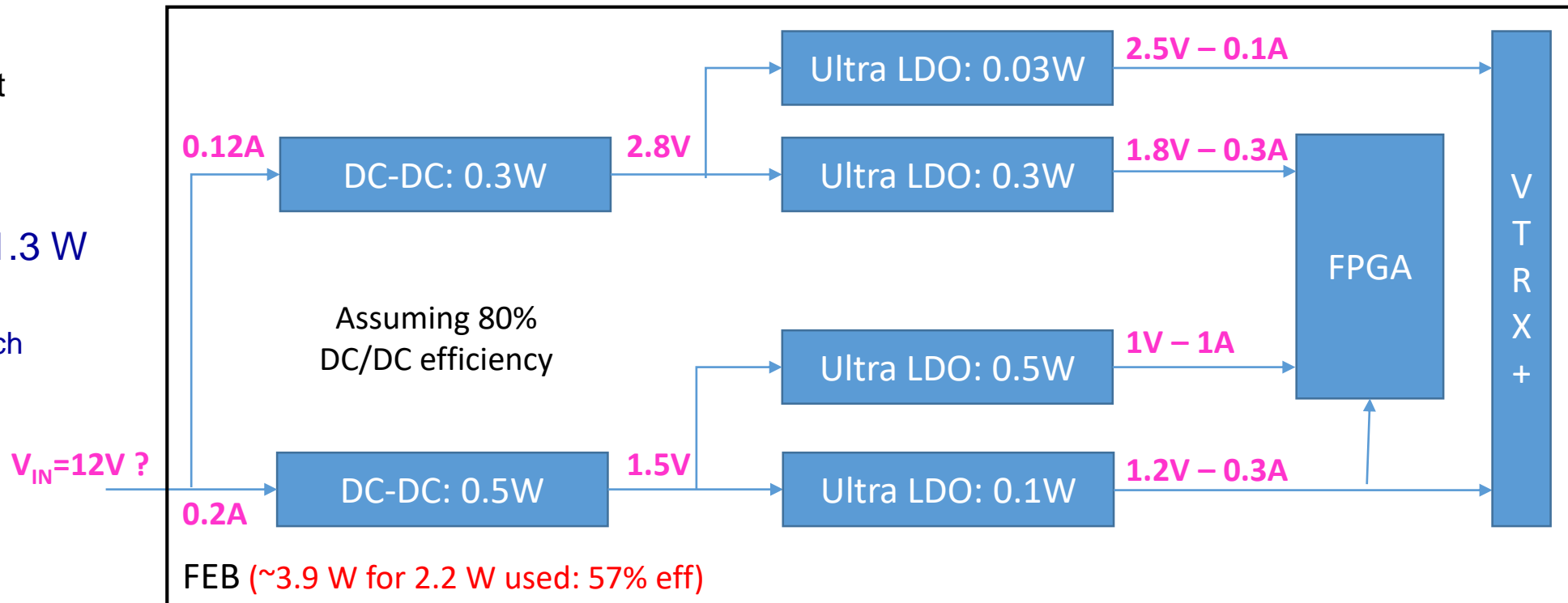
→ Supply voltage 1V2	1.2V – 4 + 12 mA / ch	Max 55 mA	0.07 W
→ Supply voltage 2V5	2.5V – 44 + 13 mA / ch	Max 100 mA	0.25 W

- Extra 2.2 W

- Needs refinement
- 3.9 W

- 256-channel FEB: 11.3 W

- 44 mW / channel
 - 14 extra mW/ch



- Distribute 3V and 2.1V from remote power supplies to FEBs
 - Assume 2.1V is distributed to FEB LDO to produce 1.2V for ASICs / VTRX+ and 1V for FPGA
 - Assume 3V is distributed to FEB LDO to produce 2.5V for VTRX+ / FPGA and 1.8V for FPGA
 - Low cross-section sense wires to ensure on-load regulation

- Power consumption of a 256-channel FEB with passive electrical RDO interface: 8.4W

- e.g. copper FireFly
- $1.2V - 4A : 2.1V \times 4A = 8.4W$

33 mW/ch

- VTRX+ add-on: ~0.4W

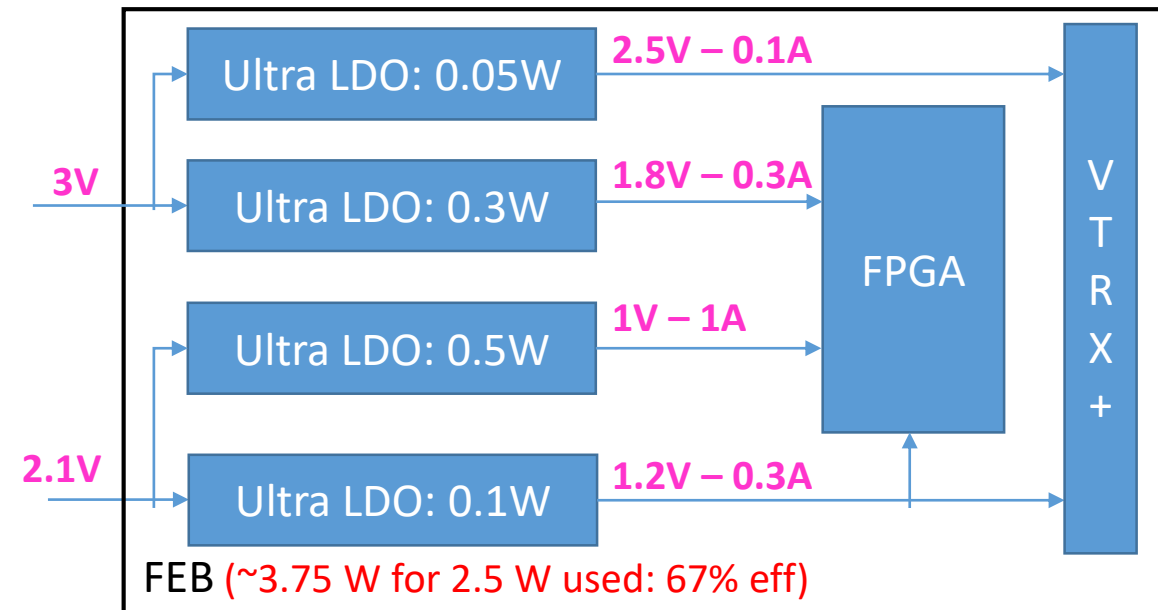
- $1.2V - 0.05A : 2.1V \times 0.05A = 0.1W$
- $2.5V - 0.1A : 3V \times 0.1A = 0.3W$

1.6 mW/ch

- FPGA add-on: ~3.6W

- $1V - 1A : 2.1V \times 1A = 2.1W$
- $1.2V - 0.25A : 2.1V \times 0.25A = 0.63W$
- $1.8V - 0.3A : 3V \times 0.3A = 0.9W$

14 mW/ch



- Power consumption of a 256-channel FEB with FPGA & VTRX+ : 12.5W

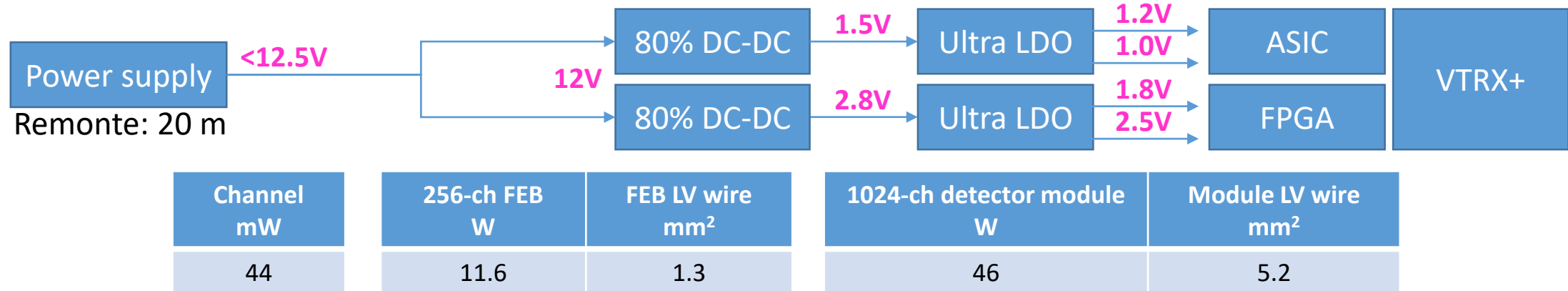
48 mW/ch

- Extra 15 mW/ch

Power distribution summary

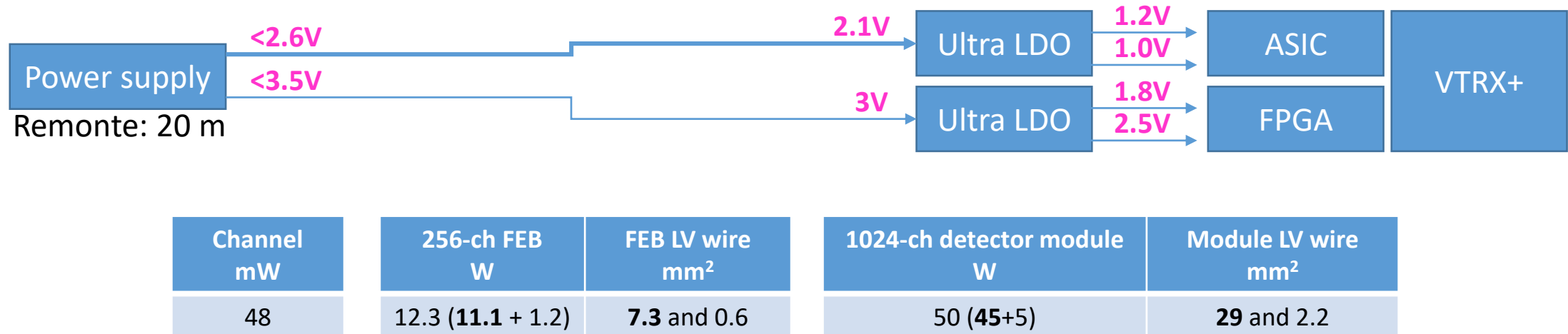
- DC/DC-based LV distribution

→ Remote power supply distributes 12V with voltage drop over 20 m cables $< 0.5V$



- LDO-based LV distribution

→ Remote power supply distributes 2.1V and 3V with voltage drop over 20 m cables $< 0.5V$

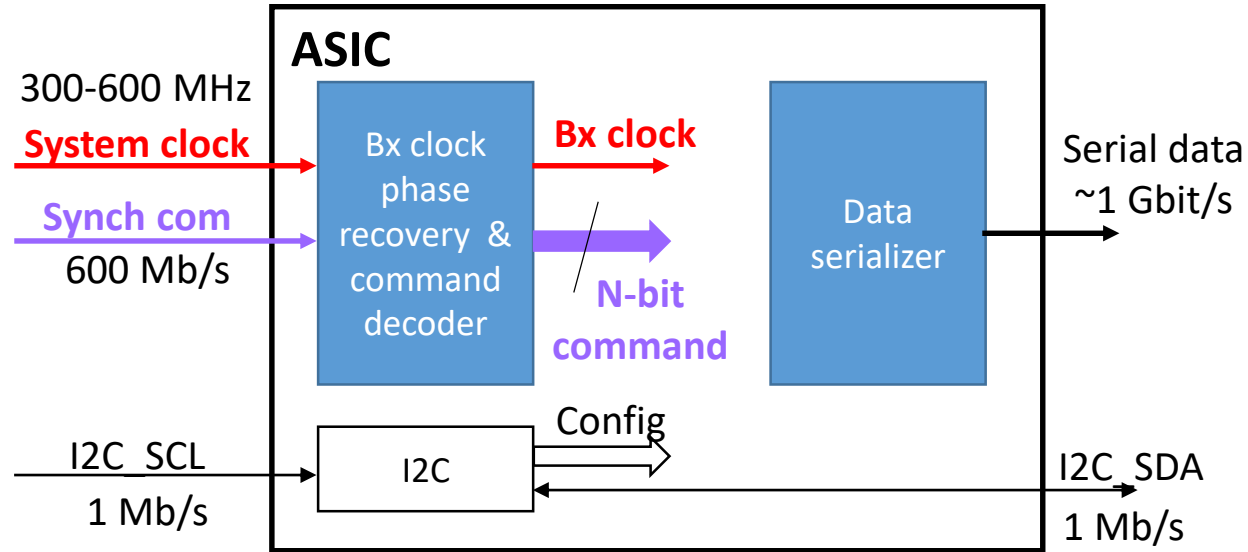


- Due to detector partitioning, VTRX+ upstream bandwidth will be largely underused
→ Not a big deal
- Requires a local on-board “intelligence”
→ Clock recovery, downstream data separation, upstream data aggregation
- Local intelligence can be implemented on a low end – low cost FPGA
→ Low to moderate rate SEU effects to be taken into account
→ If case differential IO pins are limited, use high fidelity fan-out for clock and fast commands
 - Rafael, Prisme
→ Requires a dedicated R&D
- FEB to RDO distance unlimited
- Expected power consumption of a 256-channel FEB
→ 11.6 W with on-board or closely coupled DC/DC : 44 mW / channel – extra 14 mW/ch from FPGA / VTRX
 - 5.2 mm² wires would be appropriate to distribute required power to entire 1024-channel detector module
 - Location of the magnetic field tolerant bulky DC/DC converters will most probably be problematic
→ 12.3 W without DC/DC regulators : 48 mW / channel – extra 14 mW/ch from FPGA / VTRX
 - !!! 7.3 mm² if FEBs are individually powered
 - !!! 29 mm² if a common power is delivered to a 1024-channel detector module

“Alternative” option for FEB with optical interface

Reminder: kind of “Conventional” approach

- A dedicated interface for every functionality



- Important number of heterogeneous external interface signals

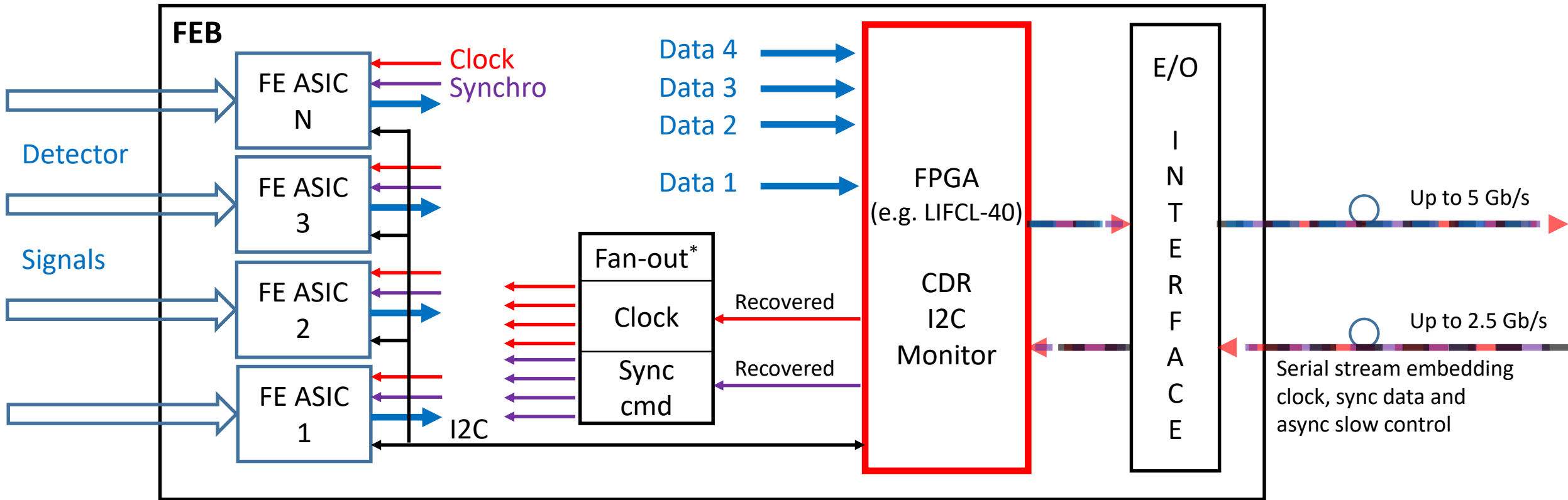
→ At least

- Clock_diff_in, SynCmd_diff_in,
- SDC_in, SDA_io
- 1 or more Data_diff_out

→ Additional features

- Trigger_diff_in
- TrigPrim_diff_out

- IpGBT or an FPGA
 - Later may be power hungry

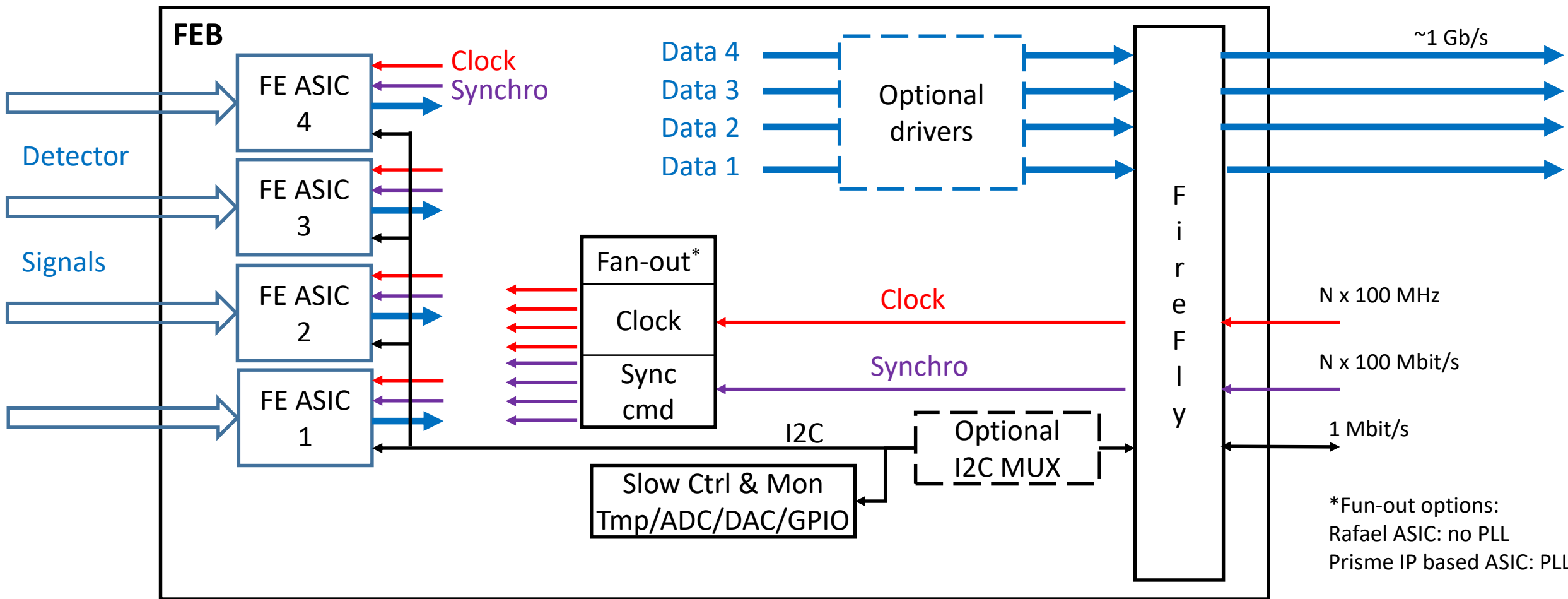


- I2C configuration of multiple on-board ASICs and of the companion ASIC can be a slow process
 - It is sequential

*Fun-out options:
 Rafael ASIC: no PLL
 Prisme IP based ASIC: PLL

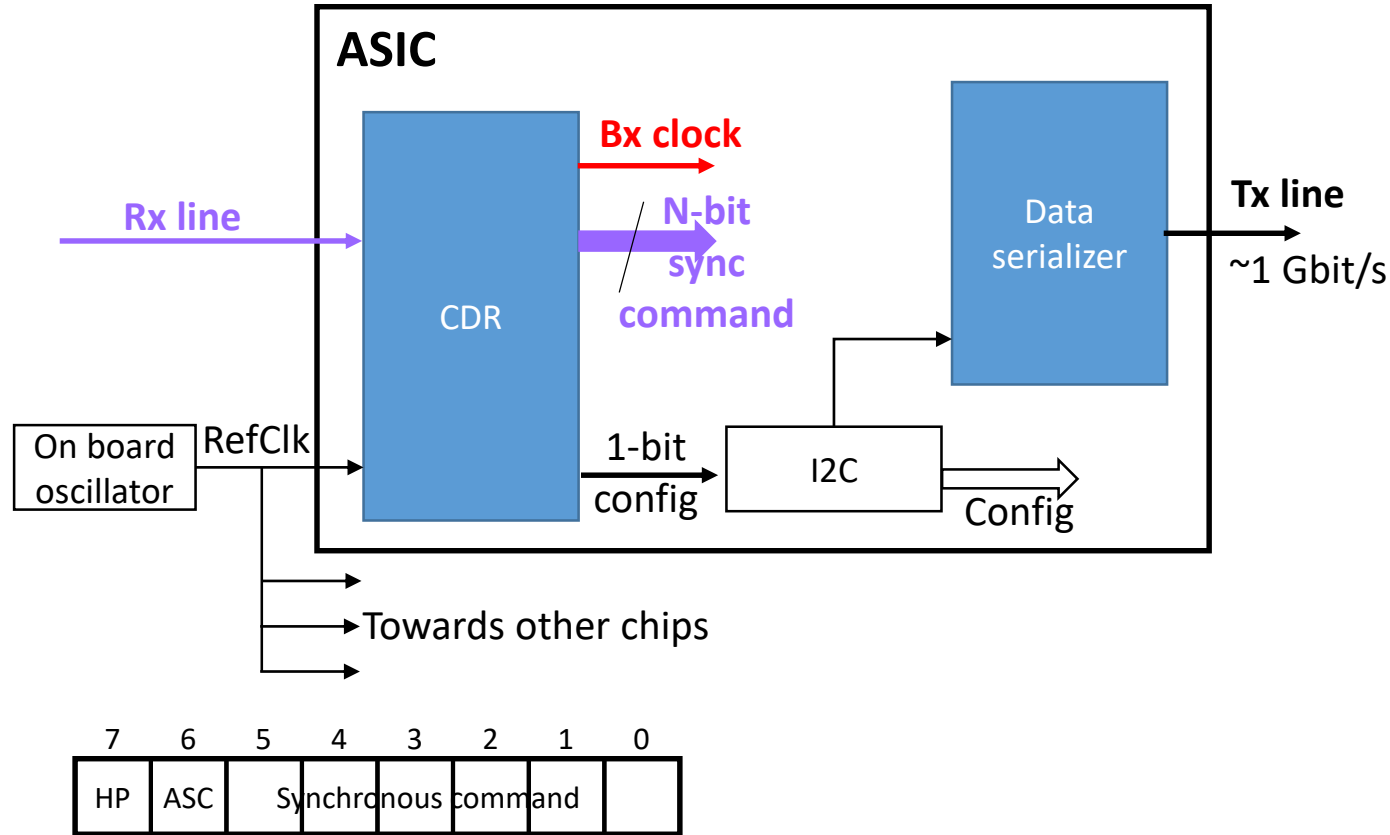
- Low extra power

→ Especially if electrical FireFly



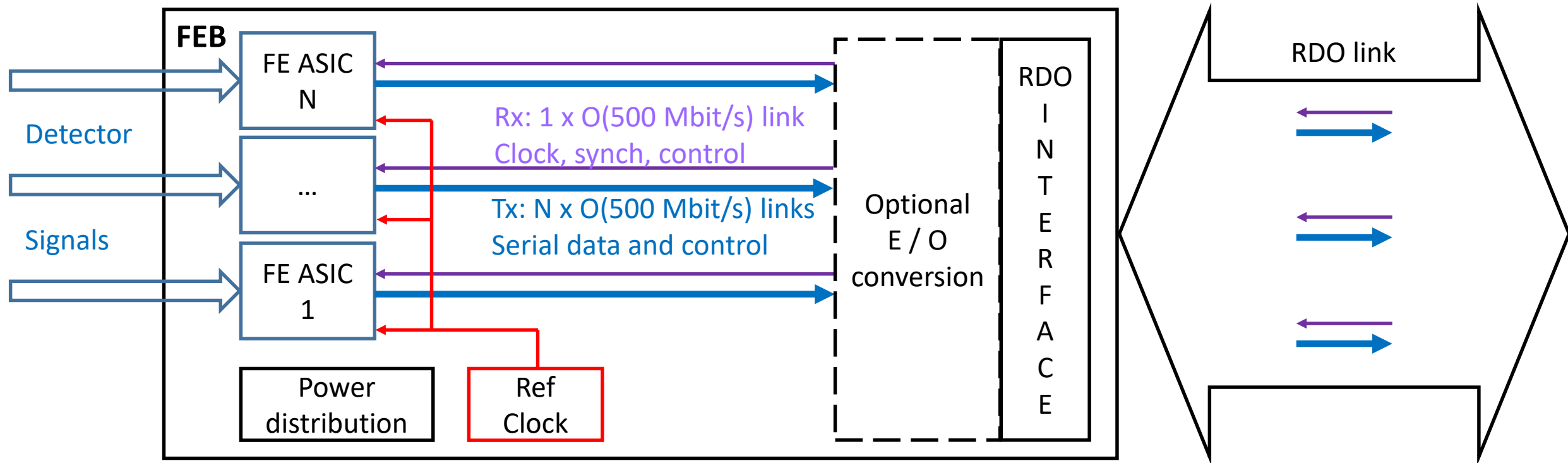
- I2C will certainly need buffers for long distance communications and in case of optical interface
- I2C configuration of multiple on-board ASICs and of the companion ASIC can be a slow process

- Single encoded line for Clock, SyncCmd, Trigger inputs and I2C



- Minimal external interface: A single diff Rx line + at least one diff Tx line**
 → Simplest case: only 4 pins (Rx_p / Rx_n + Tx_p / Tx_n) to communicate with the chip

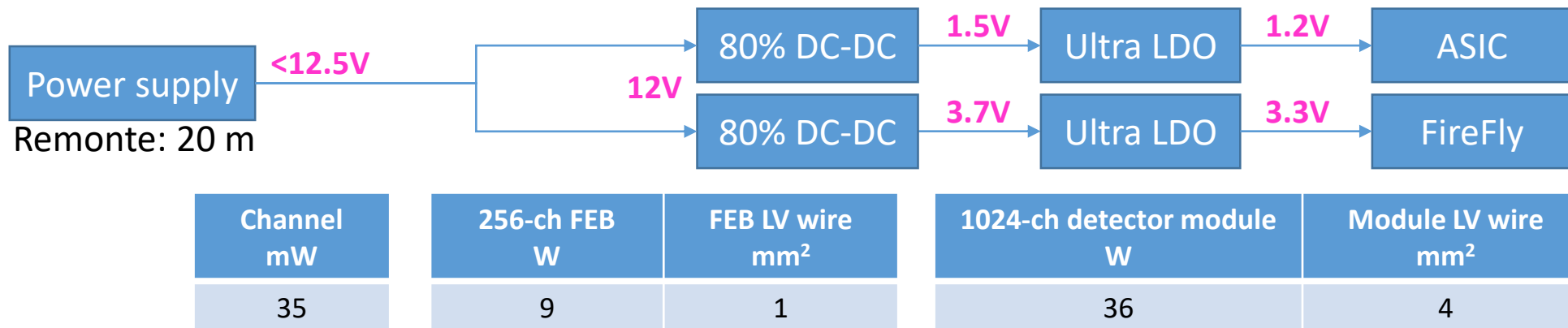
- Number of ASICs per FEB to be adapted according to detector modularity and space constraints
 - Needs a serial Rx line and at least one Tx serial line per ASICs
 - Possible choice: FireFly interface with compatible number of lanes



- Homogeneous interface**
 - RDO link is a simple collection of serial links of same nature
 - Point-to-point connection of ASICs with RDO
 - Faster parallel configuration of ASICs
 - Less than 600 (1000) Mbit/s lines can be interfaced with standard and abundant differential IOs in current FPGAs
 - Minimal extra power need in case of optical interface

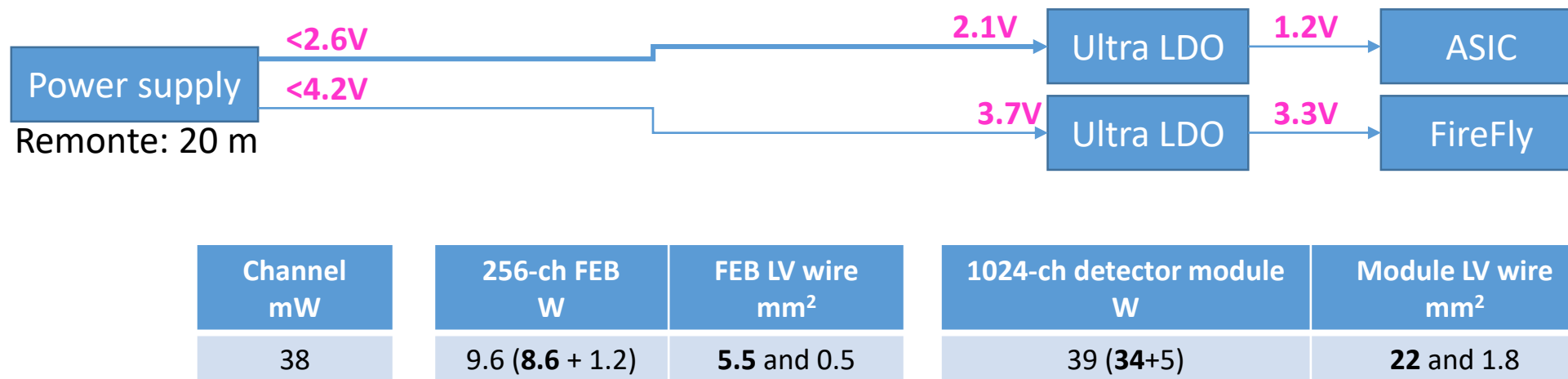
- DC/DC-based LV distribution

→ Remote power supply distributes 12V with voltage drop over 20 m cables $< 0.5V$



- LDO-based LV distribution

→ Remote power supply distributes 2.1V and 3V with voltage drop over 20 m cables $< 0.5V$



- Close to minimal active components: FE ASICs and a bi-directional optical 4-lane FireFly
 - No on-board intelligence, no aggregation, no clock-fast command distribution
 - ASIC is seen as a “DAQ unit” – a direct bi-directional connection with RDO
 - Fastest configuration
- FEB to RDO distance unlimited
- Expected power consumption of a 256-channel FEB
 - 9 W with on-board or closely coupled DC/DC : 35 mW / channel – extra 5 mW/ch due to FireFly
 - 4 mm² wires would be appropriate to distribute required power to entire 1024-channel detector module
 - Location of the magnetic field tolerant bulky DC/DC converters will most probably be problematic
 - 9.6 W without DC/DC regulators : 39 mW / channel – extra 5 mW/ch due to FireFly
 - !!! 5.5 mm² if FEBs are individually powered
 - !!! 22 mm² if a common power is delivered to a 1024-channel detector module

Summary

- In general:
 - Need to compile environmental parameters of all MPGDs
 - Understand the need of radiation and magnetic field tolerant components and their ePIC-wide availability
 - e.g. common procurement effort from CERN or other lab in the community
 - Share information about COTS components that can be used in low radiation environment of ePIC
- Potential need of 170 VTRX+ units for CyMBaL tracker
 - Pigtail length needs to be determined as well as locations of the associated optical patch panels
 - Based on efforts from integration group
 - Requires on-board “intelligence” implementing a subset of IpGBT functionality
 - The use of radiation tolerant low-end FPGA requires a dedicated R&D
 - ePIC-wide effort if it is of interest for other sub-detectors ?
 - Even a modest FPGA may end up to a substantial extra power per channel
- The use of magnetic-field tolerant DC/DC modules may be attractive for efficient powering
 - But they may be bulky to be placed on FEBs, EMC noise source and bring extra material budget
 - If used, their whereabouts to be understood: on-FEB or on a remote dedicated board
- If estimations confirmed, LV distribution without close to FEBs DC/DC converters can be problematic
 - Very bulky large cross-section cables
- An alternative option: ASICs directly interfaced to E/O component via a Tx/Rx bi-directional link
 - Can be envisaged for the ASICs under development

- ASICS:

- 32-channel Sampa: 10-20 mW/ch
 - Depending on sampling rate (5-10 MSPS) and DSP activity (e.g. off-on)
- 64-channel VMM: 16 mW/ch

- Frontends

- 160-channel FEC of ALICE TPC 16W / 100 mW/ch
 - 5 SAMPAs, 2 GBTx, 2 VTRx, LDOs
 - In magnetic field
- 256-channel FEE of sPHENIX TPC/TPOT 19W / 75 mW/ch
 - 8 SAMPAs, FPGA, 2 optical transceivers, LDOs
 - In magnetic field
 - Power distribution to be checked
- 512-channel MMFE8 of ATLAS NSW 16W / 31 mW/ch
 - 8 VMMs, ROC ASIC, SCA, FEAST DC/DCs
 - Electrical interface
 - Out of magnetic field
 - 11V distributed – no need for large cross-section cables
- 512-channel FEU of Clas12 MVT/FTT/Bonus 20W / 40 mW/ch
 - 8 Dreams, ADC, Virtex6 FPGA, 1 optical SFP, 1 1GE SFP, LDOs
 - In magnetic field
 - 4.5V / 4.5A distributed to 8 FEUs over 5m with 16 mm² wires

Characteristics of the low-voltage supply system.

Parameter	Analog supply	Digital supply
Supply voltage (V)	4.9 (5.2)	4.1 (4.4)
Cable cross-section (mm ²)	150	300
Current (A)	83	133
ΔU in cables (V)	0.65 (0.92)	0.9 (1.2)
Total power per sector (W)	407 (432)	545 (585)

- Excel file exists with several configurable options
 - Electrical interface, FPGA+VTRX Plus interface or optical FireFly interface
 - DC/DC or LDO powering
 - Calculates FEE and detector module power consumption and cable cross-sections depending on
 - FEE interface options
 - Powering scheme
 - Power supply distance
 - Allowed voltage drop in cables
- Need to understand Impact of magnetic field tolerant DC/DCs
- Need an input
 - Where the LV power supplies can be placed in case of LDO powering
 - Where the patch panels can be placed
 - The space available LV power cables and patch panels

Backup

- Just for fun: presented on 18 may, 2022, during SRO-X workshop

→ https://indico.jlab.org/event/519/contributions/9563/attachments/7748/10855/220518_SroX_FrontEnd_IM.pdf



Summary

- Frontend electronics specifications

- Sub-detector: interface, S/N, dynamic range, saturation, timing, channels, data, environment, mechanics
 - Sub-detector responsibility (e.g. some hints for MPGD in backup)
- Common: data aggregation, clock and command distribution, configuration, monitoring, protocols
 - Led by a central DAQ group

- Protocol / format definition

- Transport layer: common to most (all?) sub-detectors
- Application layer: data, synchro commands, errors: all sub-system comply

- Clock distribution

- Do not over-constraint – it is not easy
- Experience with CERN developments
 - e.g. TCLINK IP: Timing Compensated Link

- Common efforts welcome (needed, required)

- DAQ interface logic and optical bidirectional link
- COTS components validation for magnetic field and radiation
 - Power regulators
 - FPGAs, optical transceivers, PLLs
- Components within the HEP community
 - e.g. DC-DC and linear regulators, precision clock fan-out, IP blocks

Central DAQ group in close collaboration with sub-detectors?

eRD104 – Silicon service reduction