

Development of a new readout ASIC for Micro-Patterned Gaseous Detectors of EIC experiments: the SALSA chip

Summary table of persons involved in the project:

University or Institution	Last Name	First Name	Current position	Role in the project
CEA Saclay IRFU	Neyret	Damien	Senior Researcher	<i>Scientific coordinator, contact person, Working on DSP processing algorithms, test procedure development, tests with detectors</i>
University of Sao Paulo	Van Noije	Wilhelmus	Full Professor	<i>Scientific coordinator, contact person, interface with the Imec for IC production and assembling, set up test procedures</i>
CEA Saclay IRFU	Baron	Pascal	Senior research Engineer	<i>Microelectronics engineer, working on design and tests of the front-end (CSA and shaper)</i>
CEA Saclay IRFU	Bouyjou	Florent	Senior research Engineer	<i>Microelectronics engineer, working on PLL block design and checking</i>
CEA Saclay IRFU	Degerli	Yavuz	Senior research Engineer	<i>Microelectronics engineer, working on design, integration, validation, tests</i>
CEA Saclay IRFU	Flouzatz	Christophe	Senior research Engineer	<i>Microelectronics engineer, working on design, integration, validation, tests</i>
CEA Saclay IRFU	Gevin	Olivier	Senior research Engineer	<i>Microelectronics engineer, working on design, integration, validation, tests</i>
CEA Saclay IRFU	Guilloux	Fabrice	Senior research Engineer	<i>Microelectronics engineer, working on design, production, and checking</i>
CEA Saclay IRFU	Kebbiri	Mariam	Technician	<i>Technician working on electronics and detector preparation and tests</i>
CEA Saclay IRFU	Mandjavidze	Irakli	Senior research Engineer	<i>Electronics system engineer, working on DSP studies, test bench development</i>
University of Sao Paulo	Bregant	Marco	Professor	<i>Test procedure development , test coordination in Sao Paulo, test with detectors, preliminary irradiation tests</i>
Federal University of Minas Gerais	Hernandez	Hugo	Professor	<i>ADC design, and set up test structures and procedures)</i>
University of Sao Paulo	Munhoz	Marcelo	Full Professor	<i>Test with detector, preliminary irradiation tests</i>
University of Sao Paulo	Sanches	Bruno	Senior research Engineer	<i>DSP coding/simulation and set up test structures and procedures</i>
Federal University of Pampa	Severo	Lucas	Professor	<i>ADC design, and set up test structures and procedures</i>
CEA Saclay IRFU			Temporary contract	<i>Microelectronics engineer working mostly on design, simulation and tests</i>
University of Sao Paulo			Temporary contract	<i>UVM testbenches, AMS simulations, integration and testing</i>

Introduction: context and objectives

This document presents the SALSA chip R&D program, proposed by the CEA Saclay IRFU (France) and the University of Sao Paulo (USP, Brazil) in the framework of the electron-ion collider (EIC) project [EIC] and more generally for future particle and nuclear physics experiments. It aims to develop a modern versatile ASIC able to read, digitize and process signals from micro-pattern gaseous detectors (MPGD), and other kinds of detectors. This project mainly aspires to set the SALSA ASIC at the base of the readout electronics of gaseous detectors foreseen for the future experiments of the EIC collider at the Brookhaven National Laboratory (USA) in early 2030s. This document is the sequel of the one accepted in 2022 for the 2023 fiscal year, to continue the development of the SALSA chip.

Context

Micro-patterned gaseous detectors, like Micromegas [MM] or Gaseous Electron Multiplier (GEM) detectors [GEM], appeared during the 90s and began to be used in particle physics experiments from the beginning of 2000s. Compared to former gaseous detectors like drift chambers, their small amplification gaps generate short signals that typically last between 10 and 100 ns, allowing them to handle much larger particle flux. Their thin electrodes on a PCB substrate allow to reach very good spatial resolutions in the order of 100 μm .

MPGDs are nowadays used for different purposes, with different characteristics of their signals.

- As track detectors [MMCompass] to determine the position of particles crossing the detector planes
- As readout of Time Projection Chambers (TPC) [bulkMMTPC], to measure tracks in a gas volume
- As photon detectors, for example as in RICH detectors [RichMPGD], to detect electrons from photoelectrodes

Several kinds of MPGDs are envisaged for the EIC project. MPGD trackers, based on Micromegas, GEMs and/or MicroRWell detectors, are considered in the EPIC experiment [EPIC] both to detect particles at large angle (barrel region) with flat and cylindrical detectors and at low angle with flat end-cap detectors. MPGDs were indeed foreseen in all proposals published by the three proto-collaborations in 2021 [Athena] [ECCE] [CORE]. These detectors are planned to be used inside a large 1.5 to 2T solenoid, with a moderate particle flux of a few tens of kHz/cm^2 . The detector surface covers several m^2 , requiring an overall number of readout channels at the level of a few hundreds of thousand. MPGDs were also considered as photon sensors for the readout of a part of the RICH detectors at EIC [YR], but finally silicon sensors were preferred for this task.

Beside the MPGD applications, a versatile chip could be also used for non-MPGD detectors. For instance, wire chambers could be read by such an ASIC if it is able to handle signals with long tails. The readout chip may also be suitable for photomultiplier tubes if it can sustain large amplitude signals.

In addition to its intrinsic functionalities, the readout chip has to deal with constraints coming from the general DAQ system and the environment. The DAQ systems at EIC are foreseen to be based on a streaming readout scheme, like several other new experiments around the world. In such a system, the frontend electronics is continuously reading the detectors and is sending digitized data to the DAQ. The latter takes in charge the synchronization and assembly of the different data streams in a coherent way. This is in opposition to the more traditional DAQ scheme where a specific trigger system based on fast detectors distributes signals to the frontend electronics in order to initiate the readout of selected events. Thus, a new readout chip has to comply with the streaming readout, which is not the case for most of the readout ASICs currently available in the community. However the triggered DAQ scheme is still used in the domain, the future ASIC should also be able to work in such an environment.

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At last, environmental aspects are also playing an important role in the design of a readout chip. Radiation levels could be large if the readout chip is positioned close to the interaction point. The readout electronics would be also exposed to a strong magnetic field in the solenoid volume. Power consumption should be low in order to limit the heating brought by the chip. In addition the readout chip must sometimes be placed far from the detectors, introducing potentially large interconnect capacitance that results in a higher noise in the amplified signals.

Objectives of the project

The proposed ASIC will be designed to amplify and shape analog MPGD signals from 64 channels, digitize these signals with integrated Analog to Digital Converter (ADC) with sampling rates between 5 and 50 MS/s at least, and to process these data with an integrated digital signal processor (DSP) in order to facilitate their management by the DAQ system. Compared to the previous generations of readout chips, the goal of this project is to develop a versatile ASIC, suitable for various applications of MPGDs and other kinds of detectors.

Several generations of readout ASICs for MPGD and other detectors were developed in the past, at University of Sao Paulo, at IRFU and elsewhere. Most of these ASICs had characteristics somehow adapted to particular usages, like the SAMPAs ASIC developed at USP for the readout of the ALICE TPC and muon chambers, or the DREAM ASIC developed at IRFU for large trackers at Jefferson Lab. Moreover, several ASICs do not include any internal digitization device that has to be added as a complementary circuit in the electronics boards. Only very few ASICs, like SAMPAs [SAMPAs] or VMM [VMM] are equipped with ADCs.

This project aims to develop an ASIC with a wider field of applications. Even if most of the modern ASICs integrate some programmable parameters, such as gain and peaking time for instance, most of them are targeted to quite an enclosed field of application and detector types. The approach is to push forward the versatility of the architecture to make it optimized for more detectors. This at the end could drastically simplify the design at system level but also could lead to substantial economies. By using modern technology with standard programming protocols, one can make more and more analog parameters tunable. To increase the genericity, we want to increase the dynamic range of tunable values of the standard parameters but also to propose new circuits. Thus, the peaking time, the gain, but also the size of the charge preamplifier could be adapted to the particular detector type. The fall time of the preamplifier could also be adjusted to deal with very high counting rates and anti-saturation systems would also be integrated to avoid long dead times and saturation-induced crosstalks. Though the foreseen sampling frequency for the ADC is 50 MS/s, an interleaved mode, coupling two ADCs to one channel, will be available in order to reach 100 MS/s when faster sampling is required, even if this would divide the number of channels by two.

The SALSA ASIC will be compatible with the streaming readout scheme required by the modern particle physics experiments. It will also work in classical triggered DAQ systems, by accepting external signals to initiate event by event readout, and also by having the capacity to produce trigger primitives when interesting signals are observed. Standard streaming readout schemes are based on the continuous emission of sampled data to the DAQ system, which can represent a tremendous amount of information. The data reduction algorithms, specific to the applications, will be performed in order to retain pertinent information. Basic treatment can be as simple as the subtraction of the signal baseline and the deletion of samples under a given threshold. More sophisticated processings like coherent noise removal, digital shaping of the sampled signals, and/or extraction of the peak amplitude and time could be also performed. In addition, management of external trigger or veto signals will be implemented in the DSP in order to comply with the traditional triggered readout. Trigger primitive generation from digitized data will be implemented as well, based on programmable timing, amplitude and multiplicity criteria. A particular attention will be paid to the embedded

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memory management of the chip, to its interaction with the DSP and with a number of gigabit/s serial data links. The memory size and its operation will be compliant with the digital signal processing, de-randomization and pipelining needs in case of the triggered readout.

The targeted architecture is shown in Figure 1, although this design may evolve in time. The table below summarizes the specifications of the chip. Compared to the previous generations of chips designed in 130 nm or larger technologies, the choice is taken to use the more modern and certainly sustainable 65 nm technology from TSMC, in order to benefit from a larger density of components, a higher speed over power ratio and a demonstrated high radiation tolerance.

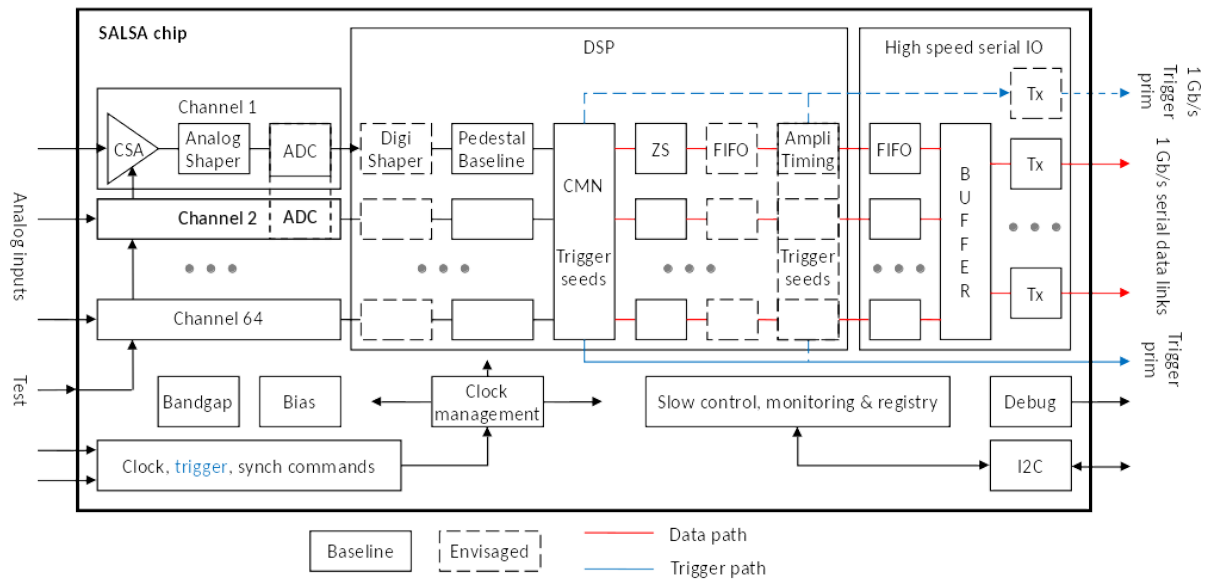


Figure 1: Considered architecture of the SALSA ASIC

Table of the preliminary specifications of the future SALSA ASIC

Front-end characteristics	
Number of channels	64
Peaking time range	50 - 500 ns
Dynamic range	0-50 fC to 0-5 pC
Input capacitance	optimized for 50 to 200 pF reasonable gain up to 1 nF, with noise level lower than 0.5% of the full scale
Input rates	25 kHz/channel, possibility to speed up the reset of the CSA to deal with large counting rates up to 100 kHz/channel
Additional features	anti-saturation circuit two selectable input transistors to match the input capacitance (detectors + interconnect) programmable signal polarity injection of test signals on any channel each element of the channel (CSA, shaper) can be by-passed and switched off
Digitization characteristics	
ADC sampling rate	5 to 50 MS/s, possibility to pair adjacent ADC channels for faster sampling rate
ADC raw dynamics	12 bits
DAQ modes	raw streaming readout, data filtering, external trigger
Digital treatments	
Basic data treatments	pedestal subtraction, common mode correction, zero suppression

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Advanced treatments	digital shaping, peak finding and amplitude/time extraction, generation of trigger primitives
Additional features	software scalers on channel digitized signals
Data output	
Output buffer	4 - 8 kwords/ch
Output data link	several 1 Gb/s links

Description of the R&D

R&D strategy

The final SALSA ASIC will be designed as an assembly of an analog front-end stage, a digitization stage and a data processing stage that will send the processed data through several high speed serial outputs. Support services will be also included in order to provide clock signals, slow-control and analog biases to the different stages. The R&D envisaged for the development of the SALSA ASIC intends to study in parallel the crucial parts of the chip, namely the frontend, the digitization and the data treatment stages, and its overall architecture. Several service blocks, in particular the PLL clock generator and the I2C slow-control, also need to be developed, the other ones are planned to be taken from external developments, in particular those done at the CERN institute.

Successive prototypes will be developed to study the different elements of the ASIC. Two initial prototypes, SALSA0_analog and SALSA0_digital were produced in 2022-23 to study respectively the frontend stage and the ADC block. The SALSA1 prototype features a few complete channels with a basic version of the SALSA architecture. Its design is expected to be complete by the beginning of 2024. The design of a more complete prototype, SALSA2, is expected in spring 2025, with mostly all the features foreseen in SALSA, but with a limited number of channels. At last, end of 2025 a complete prototype, SALSAf, will serve as a full-scale demonstrator of the ASIC. A parallel development, the PRISME project, is also taking place in 2023 to study a 65nm PLL IP block to be integrated in SALSA to generate the different clocks required by the chip. The IP block design will be also made freely available to other groups if they need such a PLL block in their chip design. The production of a PRISME prototype is expected to be launched in July 2023.

Frontend stage

The frontend is based on a charge sensitive amplifier (CSA), a pole-zero cancellation stage (PZCS), an anti-aliasing filter for direct sampling and digital filtering, and a semi-gaussian shaper for analog filtering. The input stage of the proposed CSA is implemented using two different switchable transistors. This innovative technique holds a promise to adapt the CSA to a wide range of detector capacitances by combining or separating via slow control the two transistors thus adjusting the size of the resulting input transistor. In addition, the gain, the current and the peak and fall times of the CSA is tunable. The peaking time of the shaper will be tunable approximately from 50 to 500 ns. An integrated charge injection system will be developed in order to mimic the charge of a detector in the ASIC and to be able to perform standalone tests of the chip without a detector. Special care will be taken on the choice of transistors and guard rings to avoid coupling between the analog stages and the digital circuitry that is continuously active, especially in a streaming readout. The initial SALSA0_analog prototype gives the opportunity to test independently the new circuits of the frontend stage. A finalized and optimized version is planned to be implemented in the SALSA1 prototype.

Digitization and data processing stages

The analog-to-digital converter (ADC) stage is responsible for the digitization of the analog frontend signal. The final ASIC will integrate 64 channels, *i.e.* 64 ADCs, in a single chip. That imposes limitations

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on the area and on the power consumption. The large number of bits (12 bits) and the fast sampling rate (50 MS/s) aimed by the project are directly affecting these two quantities. However, careful selection of a suitable architecture allows to reduce the impact of the sampling frequency on the ADC power consumption. Successive Approximation Register (SAR) ADC has been shown in the last decade to be an adequate architecture to reach these specifications, although for resolutions greater than 10 bits the capacitive array mismatch limits the effective resolution. An on-chip calibration circuitry is implemented to reduce its impact on the resolution of the SAR ADC. Mismatch compensation allows to reduce the array capacitor unit close to the limit imposed by kT/C noise and thereby leading to considerable energy and area reduction. Minimizing the total capacitance of the SAR ADC allows to relax the speed requirement of the voltage reference buffer and of the input signal driver (analog front-end output), which are commonly power-hungry blocks. The performance of the first version of the ADC is being tested with the initial SALSA0_digital prototype with specific injected signals. The SALSA1 prototype will host an improved version in order to finalize the ADC design and to validate the analog-digital interface preserving the excellent linearity aimed for all dynamic ranges of the chip.

The high digitization rate and continuous readout foreseen for EIC experiments require the data being reduced quite soon in the acquisition chain, if possible already by the frontend electronics. That can be done in several ways, the simplest being the zero suppression. Other possibilities are to extract, via for instance a peak-finding algorithm, the information of the shaped signal amplitude and deliver only this information together with the time of arrival. The signal can be affected by several perturbations, like baseline shift or fluctuation, common mode oscillation, or by distortions. It is therefore necessary to implement in the chip some digital signal processing capabilities. The digital signal processor (DSP) stage will be composed of a digital conditioning section followed by a buffering and formatting system culminating in high-speed output blocks providing unidirectional upstream serial data for upper processing levels in the DAQ system. The digital signal conditioning will be composed of a pipeline of filters of different strategies including FIR, IIR and nonlinear filters. The filter output data will be passed through a compression block capable at least of zero suppression lossy data reduction. Other data reduction strategies can also be applied.

Service blocks

Service blocks are defined as common blocks providing signals shared by the entire ASIC, such as the PLL generator of various required clocks, the slow control interface and the biasing control and monitoring. Some service blocks are partially available as IP components from the HEP community, in particular at CERN. The others are developed by our groups and optimized for the needs of the SALSA ASIC. Preliminary designs of the blocks were already integrated into the PRISME and the SALSA1 prototypes in order to evaluate their performances.

ASIC production

The production of the prototypes will be done through the HEP community in order to benefit from the design sharing allowed for Basic Sciences by the microelectronics software suppliers and the TSMC foundry. The design files will be produced after the global simulations and verification sign-offs. The packaging of the SALSA1 prototypes and beyond, and of the future ASIC are not defined yet. Our groups will define the best suitable package in terms of performance but also in terms of long-life availability and support from the packaging industry. The number of prototypes to be packaged will be driven by the number of samples available by Mini@sic or MPW production runs. In the order of one hundred, the production will be divided into four pools: about twenty samples in an open cavity package for early tests, visual inspection and possibly radiation hardness tests; about thirty packaged samples for each of our groups, USP and IRFU; the remaining twenty packaged samples for possible external usages.

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Evaluation and performance measurements

The functional and performance measurement test setup is being developed in parallel with the ASIC design. It is oriented to fine evaluations of individual building blocks, such as the very frontend input stages, ADCs, clock management and high speed serial links. The validation tests focus on the functionality and performance of the analog channel in terms of resolution and linearity within the dynamic ranges, counting rate, saturation, noise and transfer function figures for a wide range of input capacitances. Both signal polarities are planned to be studied. Accurate evaluation of the ADCs will be performed. Characteristics such as Differential Non linearity (DNL), Integral Non Linearity (INL) and Effective Number Of Bits (ENOB) are derived and their dependency on the ADC input clock jitter verified. The SALSA1 chips and followings contain several fully instrumented channels and allow the validation of the interoperability between the analog and digital parts, the assessment of the channel-to-channel cross-talk and, to some extent, of the level of the digital noise induced on the analog circuitry. In order to assess ultimate performance keeping the possibility to evaluate its part-to-part variation, an ASIC carrier board is designed with a minimal on-board functionality. Even though the ASICs are soldered on the carrier board, the production of a relatively simple card in quantities necessary for the tests is fairly fast and should not be costly. The team will also evaluate the chip performance with real MPGD detectors of various types performing tests with cosmic rays and/or with radiation sources. The evaluation of the prototypes with MPGDs would also include a beam test period in order to measure and compare the performance of such detectors (efficiencies, spatial and time resolutions) in real conditions with present readout electronics and with the SALSA ASICs.

Irradiation tests are foreseen for the SALSA1 prototypes, even if this aspect is not the most important at that level. Such tests would be more adapted to the SALSA2 prototypes and beyond. They will allow the total irradiation dose, latch-up and single event upset evaluations. The readout of the embedded irradiation monitoring means such as, for example, memory error correcting code (ECC) activation counters, must be implemented. For each ASIC production, the radiation hardness tests will be planned at an X-ray facility (e.g. Obelix@CERN, Geneva Switzerland), at a heavy ion (e.g. HIF@UCL, Louvain, Belgium) or at a proton irradiation facility (e.g. PS@CERN) and at a neutron irradiation facility (e.g. RIC@IJS, Ljubljana, Slovenia). There is also an ion irradiation facility available at the University of São Paulo.

Milestones and timelines

Studies on the frontend and ADC stages were started at the beginning of 2022 based on the simulations done with the process design kit provided by TSMC. The production of initial SALSA0 prototypes, with a surface of the order of 1mm^2 , were launched by the end of the year 2022, hosting four channels of the frontend stage in the SALSA0_analog prototype and an ADC block in the SALSA0_digital one. This production was financed by local budgets. The goal for both teams was to validate a first prototype of both front-end and ADC stages in the 65nm technology and to have a first assessment of the performances of all main stages before designing a chip with complete channels. The prototypes were received in June 2023 and are presently under study.

In 2023 the objective is to develop, produce and test SALSA1 prototypes hosting half a dozen of fully instrumented channels, including frontend and digitization stages, as well as a preliminary version of the DSP stage for a limited data treatment. Service blocks like biasing for stable voltage regulation, phase-locked loop (PLL) for clock generation, I2C bus slave for control and configuration, and 1 Gbit/s serial data links for digital output ports are also planned in that prototype. The SALSA1 prototype aims to validate the general design of the channels featuring both analog and digital parts, also exploring various implementations of desired functionalities and to measure their performances. The chip architecture in its baseline version is also tested and validated. The validation will be done both

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with the dedicated test-bench and with real MPGD detectors in order to check how the prototypes react in close to real conditions.

The submission of the SALSA1 prototype, which was initially foreseen in mid-2023 was delayed for several reasons. On one hand the design of the front-end stage and the ADC block included in the SALSA0 prototypes was more time consuming than foreseen, in particular due to the time required by the simulations in 65nm technology. The SALSA0 prototypes were finally submitted only at the end of 2022. The production of the ASICs was also longer than foreseen as they were finally delivered in June 2023. On another hand, a part of the manpower foreseen for the design of SALSA1 was dedicated to the PRISME project during the first semester of 2023, in order to take the opportunity given by the grant from the Generic EIC R&D program to speed up the design of the PLL IP block for the SALSA clock generation, as well as the service blocks designed in parallel for this prototype. More efforts will be dedicated to SALSA1 during the second half of 2023 in order to be able to submit the ASIC beginning of 2024.

The strategy for the year 2024 is first to evaluate carefully the performance of the SALSA1 prototypes that shall arrive around mid-2024. In parallel the SALSA2 prototypes will be designed based on the SALSA1 design, with optimized performance of the readout channels and the service blocks thanks to the results of the SALSA1 tests. The DSP stage will be also fully developed, with the implementation and the simulation of all the algorithms foreseen in the specifications: zero suppression with integrated common mode noise reduction, peak finding, trigger generation, hit scaling, etc. The design would be ready by the end of 2024 or more probably the beginning of 2025, for a delivery foreseen after the summer of 2025.

Table of major milestones foreseen during 2024 fiscal year

Milestone	Date
SALSA1 evaluation and SALSA2 specifications	2024/07/01
Submission of SALSA2 prototype	2025/03/01
Beginning of SALSA2 tests	2025/09/01

Funding aspects for 2024

The development of the SALSA prototypes requires additional engineer manpower, to work on chip design and simulation and to perform tests with the prototypes. Therefore electronics engineers hired on temporary contracts at IRFU and at USP are foreseen on the grants provided by the eRD109 call. The production of ASIC prototypes and their packaging is also quite costly. A 12mm² MPW submission is roughly estimated to be around 60k\$ per submission, while the packaging costs are estimated to be around 10k\$. Most of the materials required for the test setup are already present in our laboratories and will be shared between them, in particular prototypes of Micromegas detectors that are readily available. A budget was foreseen in the 2023 contract to complete the equipment needed for the performance evaluation of the ASICs. A residual cost for the consumables is estimated to be 7k\$ in each institute. Production of electronics cards to handle the SALSA2 prototypes is estimated to be around 17k\$, including the assembly of the printed circuit boards. Irradiation tests of SALSA2 would represent an overall cost of 8k\$, including the material costs of the tests, and access fees in some of the irradiation facilities. At last, travel expenses have to be taken into account for some of the tests and for IRFU-USP project meetings. The expenses and the manpower resources are listed in the table below.

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Table of manpower and costs in 2024

Tasks	Manpower (p.month)	Material costs	Institute
SALSA2 design	9 9		IRFU USP
SALSA2 ASIC production		Proto MPW submissions: 60 k\$ Packaging: 10 k\$	IRFU
Test-bench setup	2 2	Equipment at IRFU: 4 k\$ Equipment at USP: 4 k\$	IRFU USP
Production of test cards	4 2	Production at IRFU: 12 k\$ Production at USP: 5 k\$	IRFU USP
ASIC performance measurements	7 7		IRFU USP
Irradiation tests	2 2	IRFU: 4 k\$ USP: 4 k\$	IRFU USP
Travels		IRFU: 7 k\$ USP: 7 k\$	IRFU USP
Temporary manpower		Temporary contract microelectronics engineer: 60 k\$ Temporary contract engineer: 44 k\$	IRFU USP
Total	46	221 k\$	

Table of 2024 budget per institution

Institution	IRFU	USP
Budget	157 k\$	64 k\$

Outlook of the project for 2025 and beyond

After the validation of the SALSA1 design and the measurement of its performance in 2023-2024, the next prototype, SALSA2, will be developed in 2024. It is meant to evaluate almost final designs of the analog and digital stages, including the DSP with all its algorithms, of the common services and of the overall architecture, but with a low number of channels. The goal is to assess the achievable performance in real conditions, with various radiation sources and in test beam campaigns, in order to validate the final architecture and perform an extensive study of the performance of the ASIC in very different conditions. Radiation tests like Total Ionizing Dose (TID), latch-up and Single Event Upset (SEU) will be performed on SALSA2 to stress the radiation-hardened design of every sensitive part of the analog and digital stages. All these tasks are expected to take place during the largest part of the year 2025.

The year 2025 will be also dedicated to the design of the final SALSAf prototype with the nominal number of channels. The chip production will be launched at the end of 2025, to be evaluated in 2026. The objective is to validate the targeted performance of the chip coupled to different types of MPGDs, in various environmental and experimental conditions, e.g. in test beam campaigns. Radiation tests will be also repeated on the final prototype to ensure its hardness in harsh radiation environments. Samples of the chips in its final package will be distributed to interested users for evaluation accompanied with detailed documentation and support from the designers. The mass production procedure of the chips will be at last launched in 2026 with a pre-series run and a dedicated production test bench.

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The table below summarizes the budgets foreseen for 2025 and 2026. The budget for 2025 will be particularly large due to the costs associated with the production of the full-scale SALSAf prototype which will have a surface of the order of 1 cm². It is complicated to estimate precisely from now the cost of the MPW production and the final size of the chip, the budget mentioned is a rough estimation of the cost including the packaging of the chips.

Table of foreseen budgets for the years 2025-2026

Year	2025	2026
Estimated budget	300 k\$	20 k\$

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