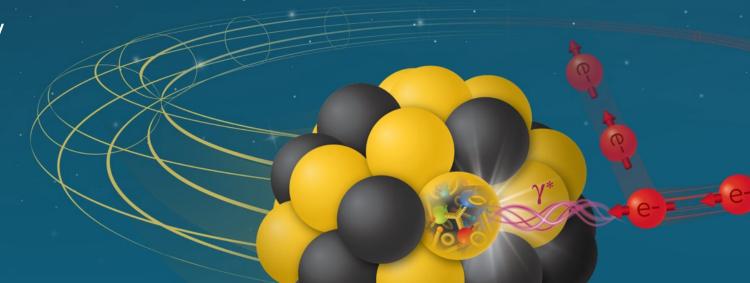
Silicon: Overview

Ernst Sichtermann ePIC Silicon Vertex Tracker Detector Subsystem Collaboration Lead

Lawrence Berkeley National Laboratory

Incremental Design and Safety Review of the EIC Tracking Detectors
March 20-21, 2024

Electron-Ion Collider



Charge Questions Addressed

- 1. Are the technical performance requirements appropriately defined and complete for this stage of the project?
- 2. Are the plans for achieving detector performance and construction sufficiently developed and documented for the present phase of the project?
- 3. Are the current designs and plans for detector, electronics readout, and services sufficiently developed to achieve the performance requirements?
- 4. Are plans in place to mitigate risk of cost increases, schedule delays, and technical problems?
- 5. Are the fabrication and assembly plans for the various tracking detector systems consistent with the overall project and detector schedule?
- 6. Are the plans for detector integration in the EIC detector appropriately developed for the present phase of the project?
- 7. Have ES&H and QA considerations been adequately incorporated into the designs at their present stage?

Outline

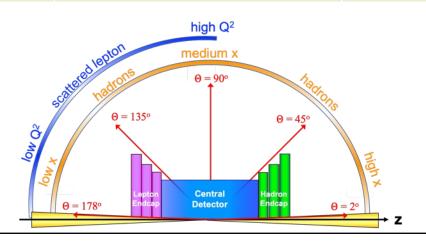
- Requirements
- Sensor
- Sensor Tiling and Grouping
- Local Mechanics
- Detector Subsystem Collaboration
- Timeline
- Risks and Mitigation
- Summary

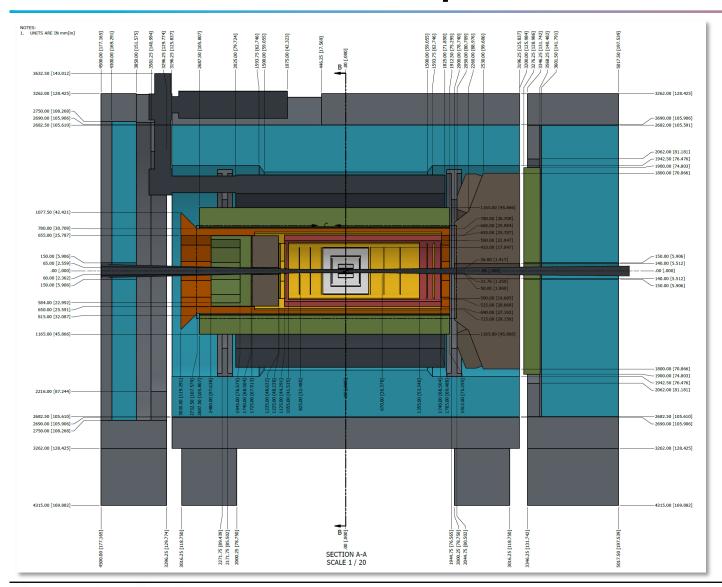
Requirements

Performance Requirements

- https://eic.jlab.org/Requirements/index.html
- Based on physics in the <u>Yellow Report</u>

	Momentum Resolution	Spatial Resolution
Backward (-3.5 to -2.5)	~0.10%×p⊕2.0%	~ 30/pT μ m \oplus 40 μ m
Backward (-2.5 to -1.0)	~ 0.05%×p⊕1.0%	\sim 30/pT μ m \oplus 20 μ m
Barrel (-1.0 to 1.0)	~0.05%×p⊕0.5%	~ 20/pT μ m \oplus 5 μ m
Forward (1.0 to 2.5)	~0.05%×p⊕1.0%	\sim 30/pT μ m \oplus 20 μ m
Forward (2.5 to 3.5)	~0.10%×p⊕2.0%	\sim 30/pT μ m \oplus 40 μ m





Spatial extent along the beam axis:

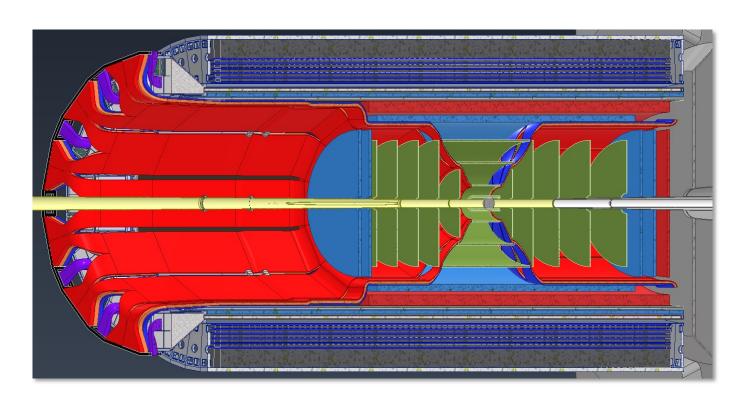
$$-106.25 < z_{SVT} < 136.25$$
 cm

Radially:

$$r_{out} < 43.00 \text{ cm}$$

 $r_{in}(z)$ determined by beam-pipe + 5mm

Beam-pipe bake-out with SVT installed; clamshell of detector halves,



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 cm

Radially:

$$r_{out}$$
 < 43.00 cm

 $r_{in}(z)$ determined by beam-pipe + 5mm

Beam-pipe bake-out with SVT installed; clamshell of detector halves,

Minimized services – space is at a premium.

Inner Barrel (IB)

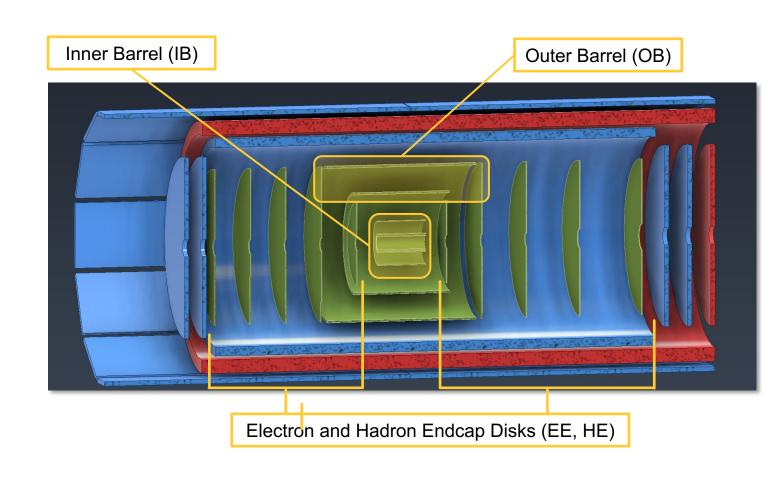
- Three layers, L0, L1, L2,
- Radii of 36, 41, 120 mm
- Length of 27 cm
- $X/X_0 \sim 0.05\%$ per layer
- Curved, thinned, wafer-scale sensor

Outer Barrel (OB)

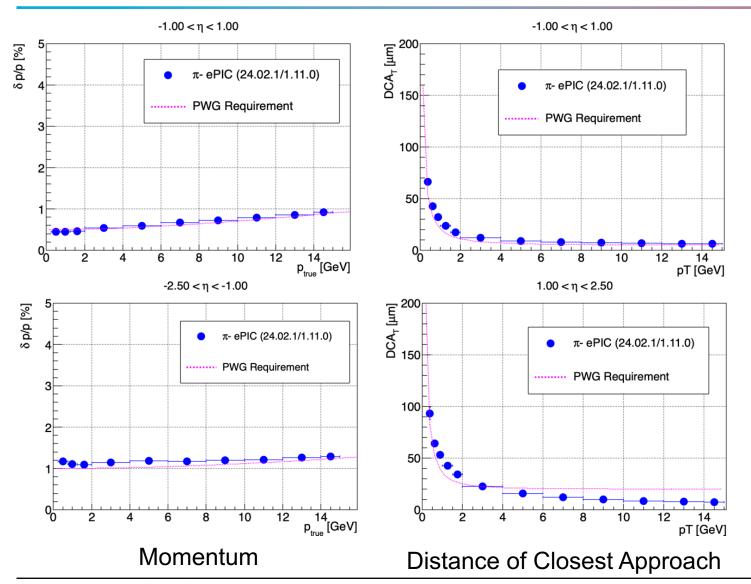
- Two layers, L3, L4
- Radii of 27 and 42 cm
- X/X₀ ~0.25% and ~0.55%
- More conventional structure w. staves

Electron/Hadron Endcaps (EE, HE)

- Two arrays with five disks
- X/X₀ ~0.25% per disk
- More conventional structure



Lengths for L2—L4 increase so as to project back to z = 0; disk radii adjust accordingly

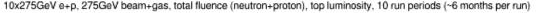


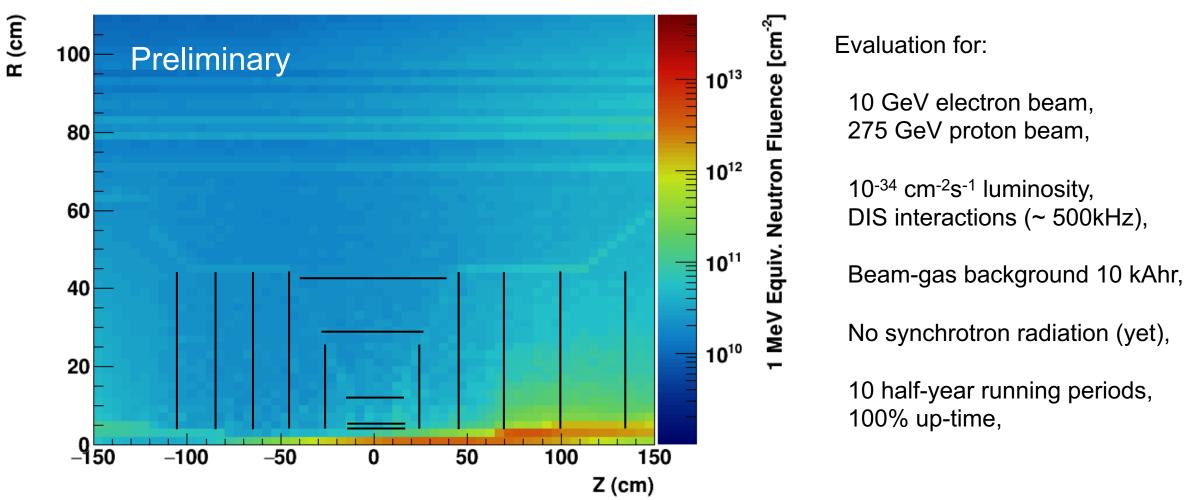
SVT concept is optimized for resolution,

Simulated resolutions meet the requirement in the central region,

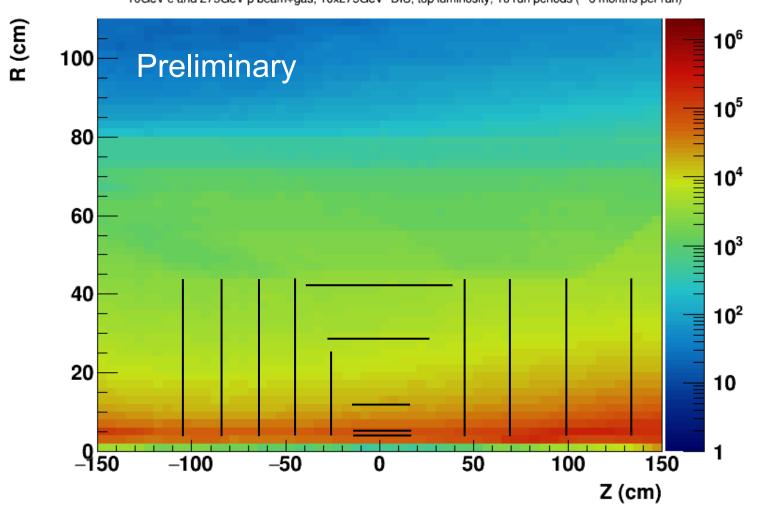
Simulated resolutions substantially meet the requirements in the forward/hadron and backward/electron region,

Physics objectives in the far backward/ electron region will need to be met by means of a combination of precision tracking and precision electron calorimetry.









Region close to the beampipe is projected to experience a few hundred kRad,

Most of the SVT projected to be below ten kRad,

Fluence up to few 10^{12} n_{eq}/cm^2 for the inner region of the the hadron endcap, otherwise 10^{11} n_{eq}/cm^2 or less,

Low, $O(10^{-7})$ hit occupancy per pixel in a $O(\mu s)$ readout frame

Sensor

Technology of choice for the SVT is Monolithic Active Pixel Sensor,

This choice was made following a technology survey, c.f.

Laura Gonella on behalf of eRD16 and eRD18, "EIC Silicon Vertex and Tracking: Technology Survey" at the 1st EIC Yellow Report Workshop

Drivers include high granularity, low power consumption, and low material, as well as synergies with large-scale developments in the broader community – in particular the ALICE-ITS3 development,

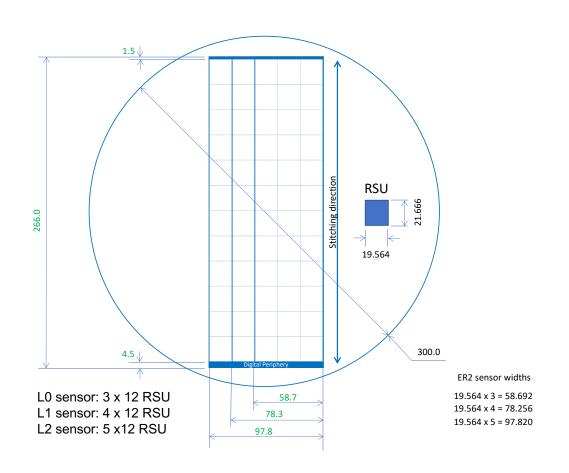
Pragmatic choice to seek to join the ITS3 development and adapt, where needed, the sensor, called "MOSAIX", for use in the SVT,

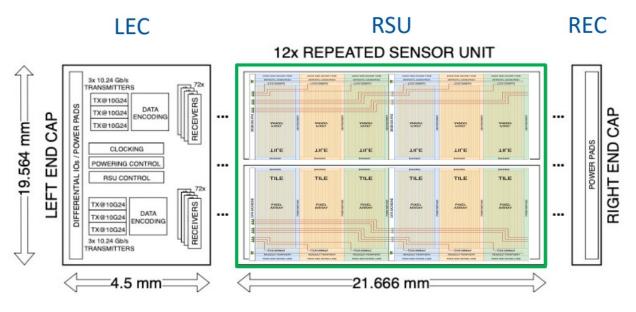
Large SVT area of ~8 m² is one of the drivers in the need to adapt ITS3 to become EIC-LAS; same for the choice to use an ancillary IC to provide serial powering, bias voltage, and multiplex slow controls,

Formal partnership with ITS3 now in an advanced stage.

MOSAIX

Credit: ALICE ITS3 Collaboration





Pixel size: $\sim 20 \times 22 \mu m^2$ Frame duration: 2 to 5 μ s

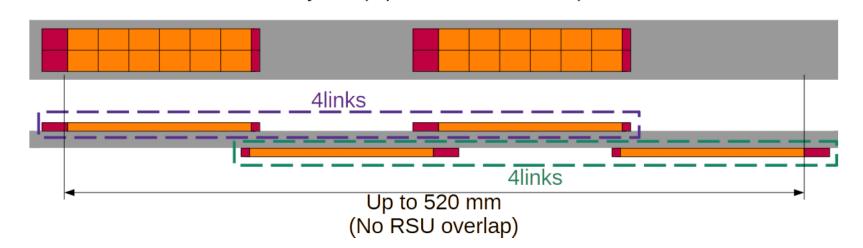
Data link: 10.24 Gbps

EIC-LAS with 5 or 6 RSUs is the outcome of extensive tiling studies and foundry constraints as they are currently known; a) only a single variant will be accommodated on any given wafer and b) NRE considerations limit the number of variants to two, at most.

Staves are foreseen as the basic building elements for the Outer Barrel, i.e. L3 and L4.

Tiling of EIC-LAS sensors onto staves is relatively straightforward, provided the structure allows for geometrical overlap:

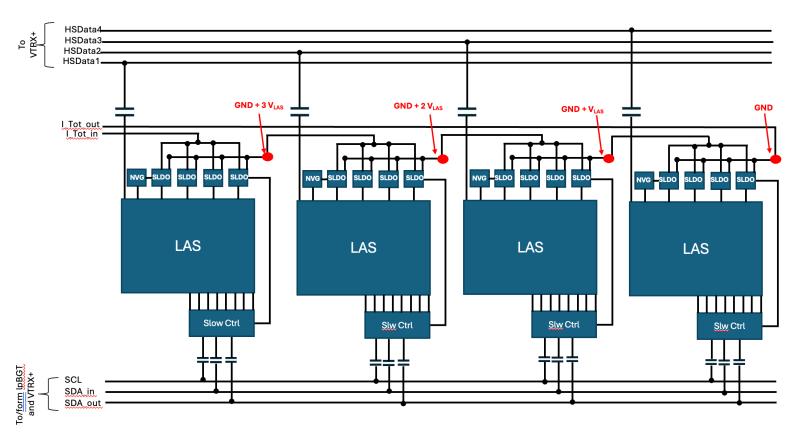
Layer 3 (Opt 1 & 2, 6RSU-LAS)



This tiling naturally leads to groupings of (up to) four EIC-LAS in powering, readout and slow-control.

Tiling naturally leads to groupings of (up to) four EIC-LAS; this is key to service reduction with serial powering and multiplexed slow control.

At a functional level:

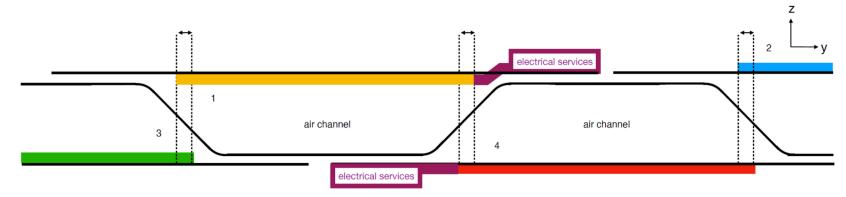


A group of (up to) four EIC-LAS is serially powered via one current loop; controlled with three slow-control lines.

EIC-LAS with 5 or 6 RSUs is the outcome of extensive tiling studies and foundry constraints as they are currently known; a) only a single variant will be accommodated on any given wafer and b) NRE considerations limit the number of variants to two, at most.

Disks are currently foreseen to have a corrugated core. Tiling can then be done on four surfaces.

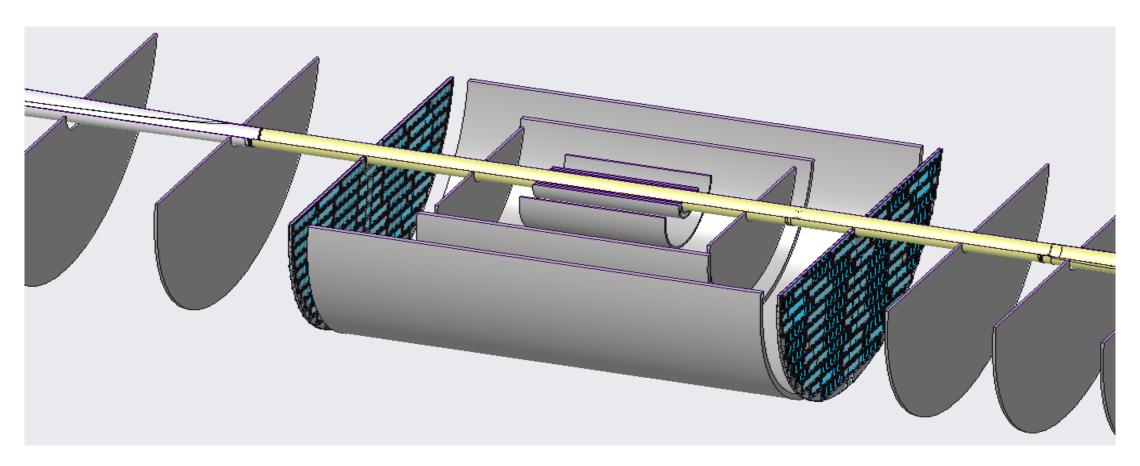
In sideview, with the length axis of the sensor going into or coming out of the screen:



Overlap along the length axis is possible by alternation,

Corrugation pitch and height determine EIC-LAS overlap along the short axis; current values of ~34 mm and 6 mm, respectively, are being further optimized.

Local Mechanics



Note the crossing angle and acceptance cones of the beampipe. Top-down symmetry favors a horizontal segmentation of the disks.

Electron-Ion Collider

The Outer Barrel will consist of staves,

Stave will have twins of sensors on alternating sides (c.f. slide 16),

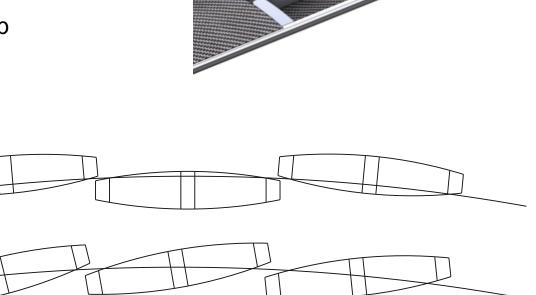
Core will consist of foam blocks, supporting all sensor edges,

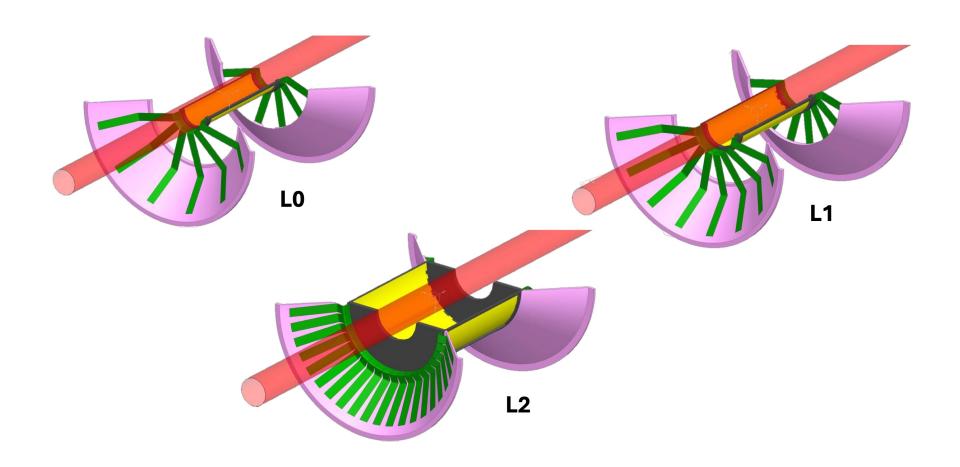
Surface between twins of sensors will be covered with a CF skin,

Thickness and possible curvature, as well as material and lay-up remain to be optimized,

After co-cure or bonding the structure will be self-supporting.

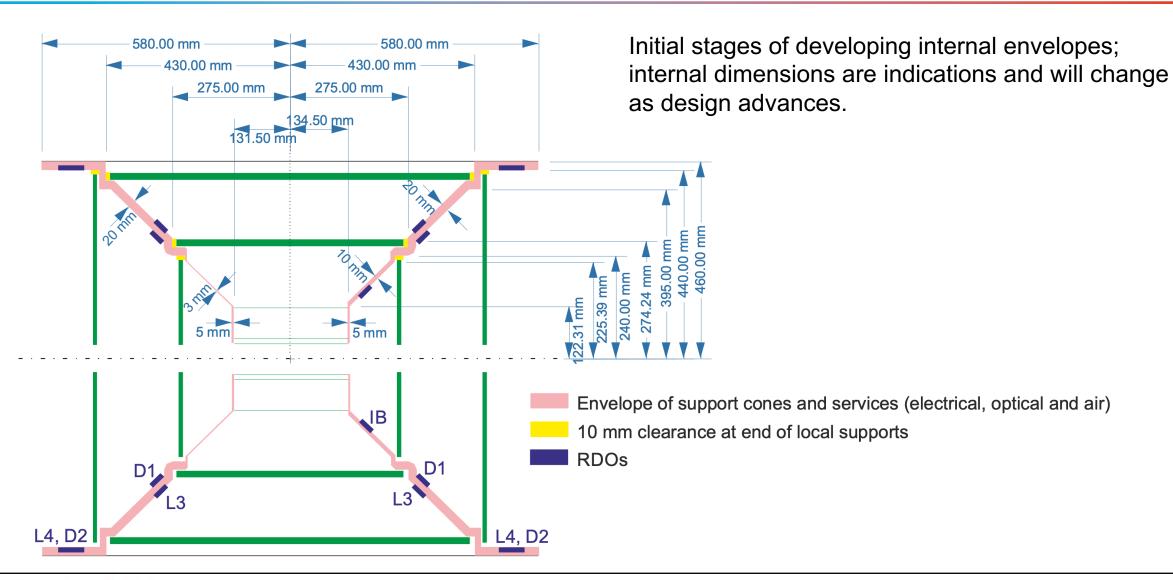
Castellated as well as tilted arrangement of staves being considered for the OB.





Initial stages of suitably adapting the ITS3 concept(s) to the ePIC SVT

Internal Envelopes



Detector Subsystem Collaboration

























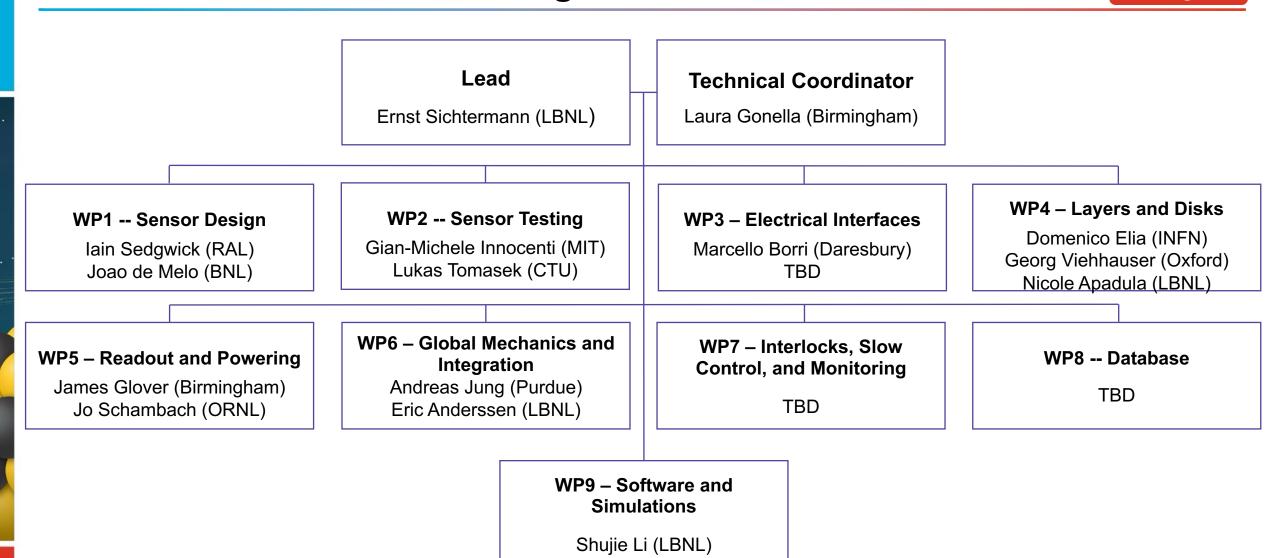




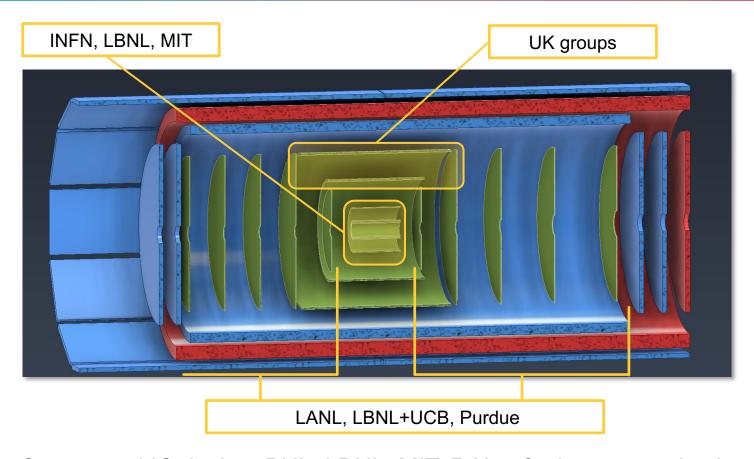




Extensive Si-detector experience in the ALICE, ATLAS, CMS, sPHENIX, STAR collider experiments



Electron-Ion Collider



Sensor and IC design: BNL, LBNL, MIT, RAL – further groups in characterization

Readout: ORNL, MIT

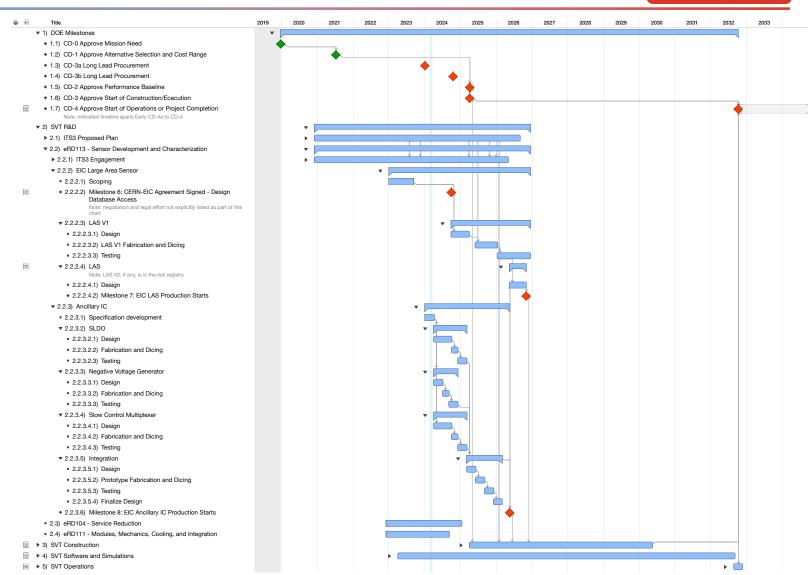
Additional groups expressed interest

Electron-Ion Collider

Schedule

Timeline

- Sensor development:
 - ITS3 wafer scale sensor development (ER2, ER3) for IB 2024 – 2026,
 - EIC-LAS development for OB and Disks complete and ready for production start in calendar Q4 2026,
 - Ancillary IC development for EIC-LAS complete and ready for production start in calendar Q2 2026.

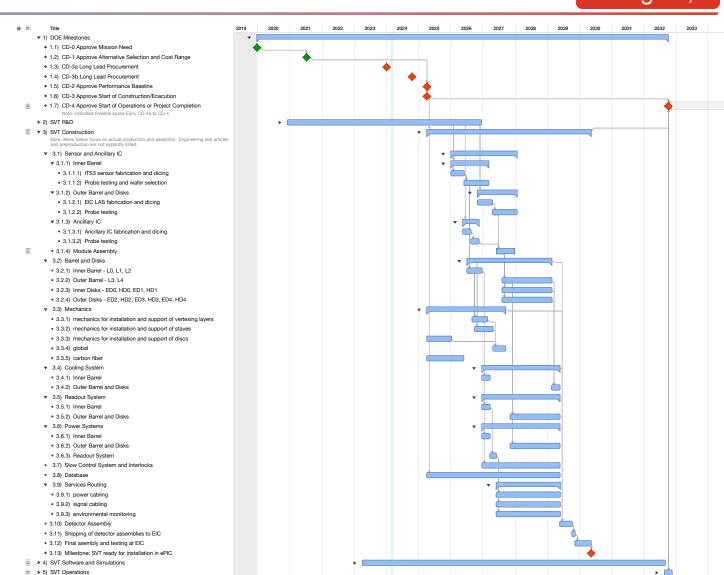


Timeline

Charge 5,7

Construction:

- Engineering test articles following R&D in 2025—2026,
- Pre-production phase of about 1 year for IB; 2 years for OB,
- Production and QA through calendar Q2 2029 followed by assembly,
- Current plan is shipment of surveyed and assembled half barrels and disks to BNL in calendar Q4 2029,
- Final assembly and testing at BNL through calendar Q1 and Q2 2030, prior to installation in ePIC.
- SVT schedule is compatible with Project requirements, being finalized.



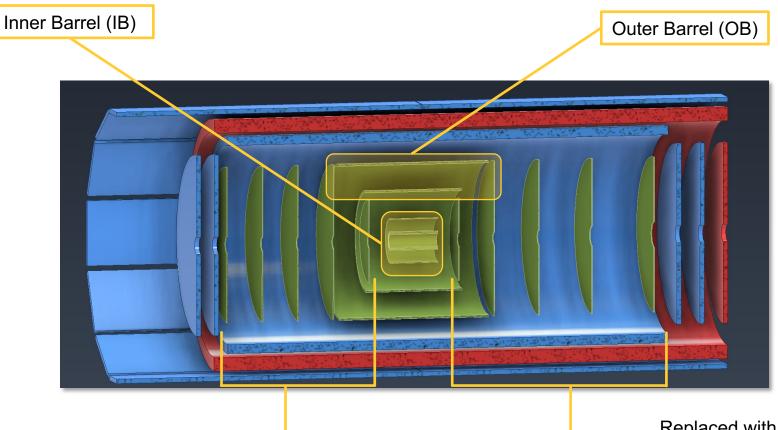
Risks and Mitigation

Alternative Tracker

- Goal is always to progress towards using ITS3 based sensors
 - Only way to meet full performance requirements
- Branchpoints both based on schedule delays:
 - 1. ITS3 (inner barrel) schedule remains compatible with project schedule but LAS (outer barrel & disks) development is delayed
 - 2. ITS3 (inner barrel) schedule becomes incompatible with project schedule

Alternative Tracker – Layout

Replaced by two or three layers based on the existing ITS2 sensor, as used in ALICE and sPHENIX without EIC specific modifications Branchpoint 2 only



Replaced with two MPGD barrel layers derived from the outer MPGD tracker, specifically its innermost (Micromegas) layer *Branchpoint 1 & 2*

Electron and Hadron Endcap Disks (EE, HE)

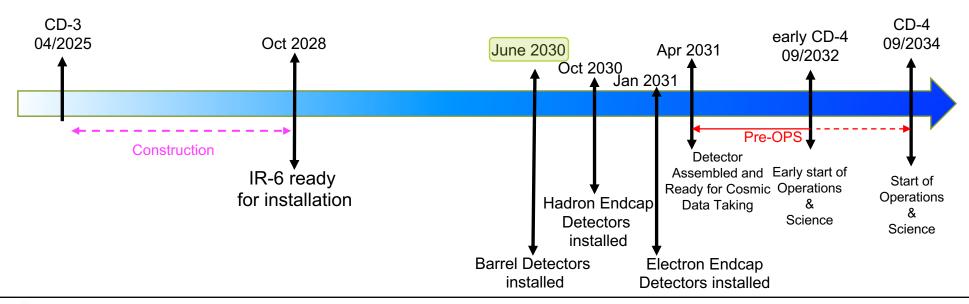
Replaced with (in total up to) seven near-identical MPGD disks on each side, specifically based on existing uRWELL disks Branchpoint 1 & 2

Electron-Ion Collider

Alternative Tracker – Schedule

• Will be further refined leading up to CD-2 based on ITS3 development

Branchpoint	Date	Milestones
1 (LAS Delay)	Q2/Q3 2026	1 year for MPGD foils + 3 years construction
2 (ITS3 Delay)	Q3/Q4 2027	Same 3 years construction as current IB



Summary

- Silicon Vertex Tracker acceptance and technical performance requirements are defined,
- SVT layout, consistent with the requirements, has been optimized for resolution,
- SVT will be based on a new Monolithic Active Pixel Sensor in 65 nm technology that is being developed in collaboration with the ongoing ALICE-ITS3 MOSAIX development,
- SVT will use an ancillary IC for serial powering, biasing, and multiplexing of slow controls with minimized material in view of risk, schedule, and resources,
- SVT designs are advancing,
- SVT workforce identified and growing,
- SVT timelines are consistent with the Project timelines and critical decisions.