Silicon: Sensors (Inner & Outer Barrel, Disks)

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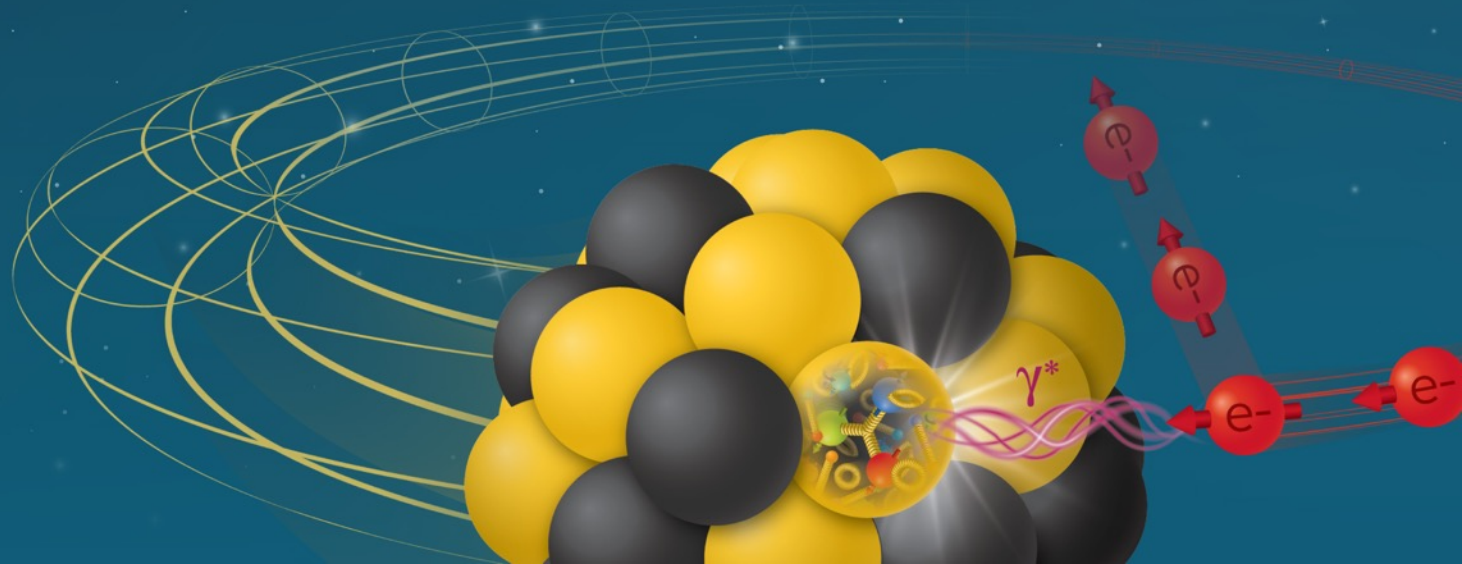
Incremental Design and Safety Review
of the EIC Tracking Detectors
March 20-21, 2024

Electron-Ion Collider



Charge Questions Addressed

1. Are the technical performance requirements appropriately defined and complete for this stage of the project?
2. Are the plans for achieving detector performance and construction sufficiently developed and documented for the present phase of the project?
3. Are the current designs and plans for detector, electronics readout, and services sufficiently developed to achieve the performance requirements?
4. Are plans in place to mitigate risk of cost increases, schedule delays, and technical problems?
5. Are the fabrication and assembly plans for the various tracking detector systems consistent with the overall project and detector schedule?
6. Are the plans for detector integration in the EIC detector appropriately developed for the present phase of the project?
7. Have ES&H and QA considerations been adequately incorporated into the designs at their present stage?

Outline

- ePIC SVT sensors
- Development status and plan
- Summary

ePIC SVT sensors

Sensor technology for the SVT

Charge 3, 4

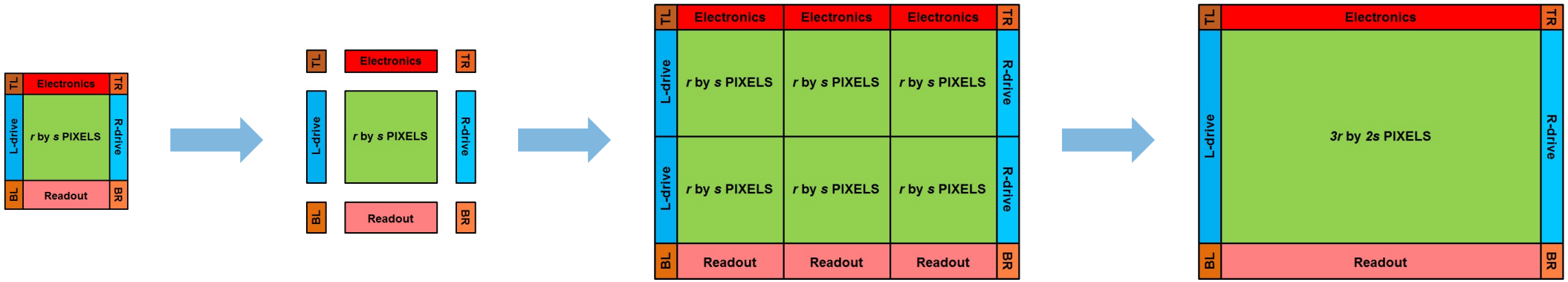
- The ePIC SVT will be built with **Monolithic Active Pixel Sensors (MAPS) in 65 nm CMOS imaging technology**

- High granularity and low power → High spatial resolution
- Stitching on 300 mm wafers for large area sensors → Increased detector active area, reduced material budget
- Collaboration with ITS3 → Reduced risk and cost of sensor development

Stitched MAPS

- MAPS size is typically constrained to the size of a single reticle (~ cm^2)

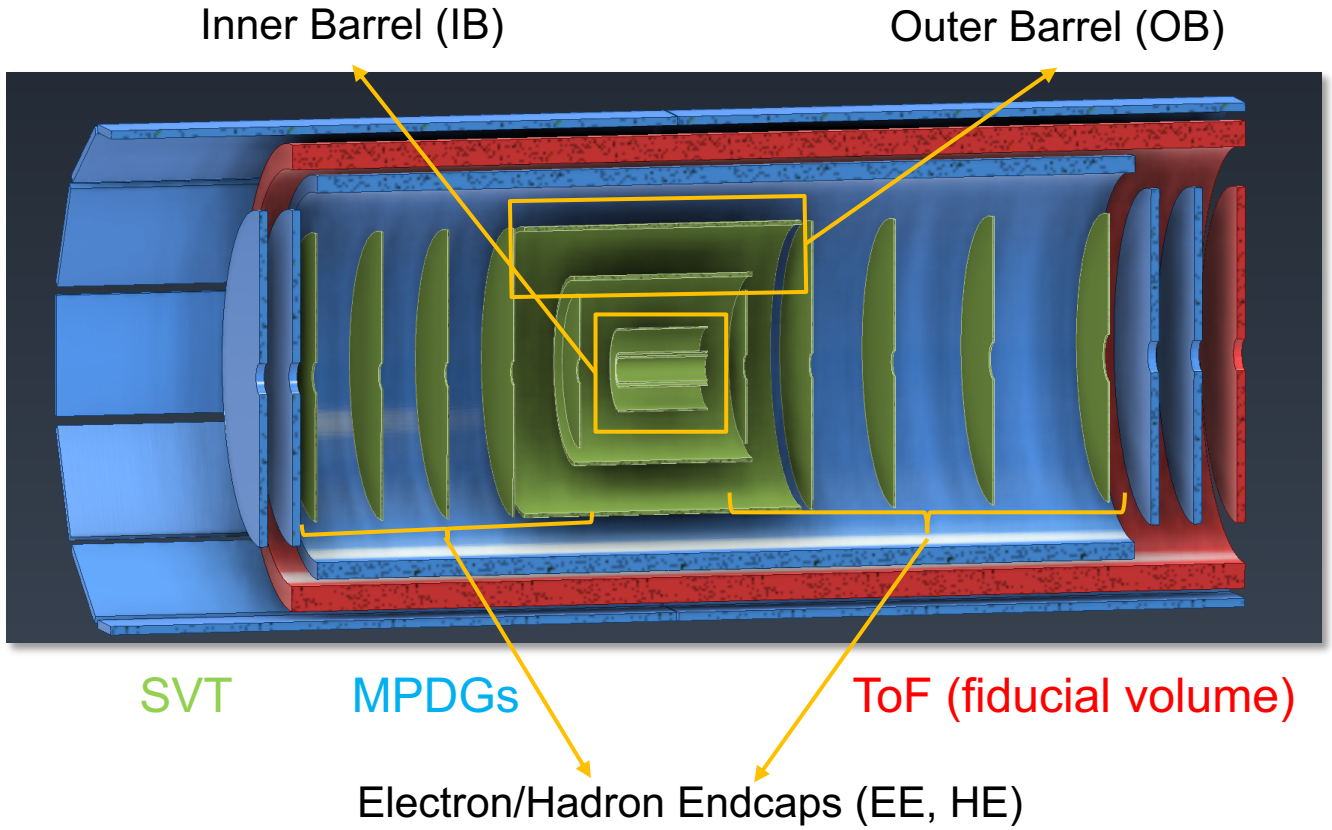
- Stitched MAPS sensor can achieve larger active area
  - Lithography elements can be applied separately over the wafer
  - Stitching allows to form a uniform pixel matrix
  - The sensor size can be up to wafer scale



SVT Sensors

Charge 3

- **ITS3 wafer scale sensor**
  - Inner Barrel
- **EIC-LAS**
  - Outer Barrel
  - Electron/hadron endcaps
- **Ancillary ASIC**
  - Outer Barrel
  - Electron/hadron endcaps



ITS3 Wafer Scale Sensor

Charge 3

- The ITS3 sensor will be used in the ePIC Inner Barrel
- This is a wafer scale, low power sensor enabling the design of truly cylindrical **vertex layers with 0.05% X0 material budget**
- Ultra-low mass detector concept pioneered by ITS3
  - Thin, bent sensors → Minimal mechanical support
  - Low power sensors → Air cooling
  - Large sensor → No services in active area

ITS3 Wafer Scale Sensor

- **MLR1** - Submitted Q4 2020
  - **Technology exploration** and prototype circuit blocks for future sensors
  - Large number of test structures; including Analogue and Digital Pixel Test Structures (APTS, DPTS)

- **ER1** - Submitted Q4 2022
  - Exploratory designs (MOSS, MOST sensors) for **proof of stitching principles**, learning methodology and yield
  - Also, small prototypes and test chips

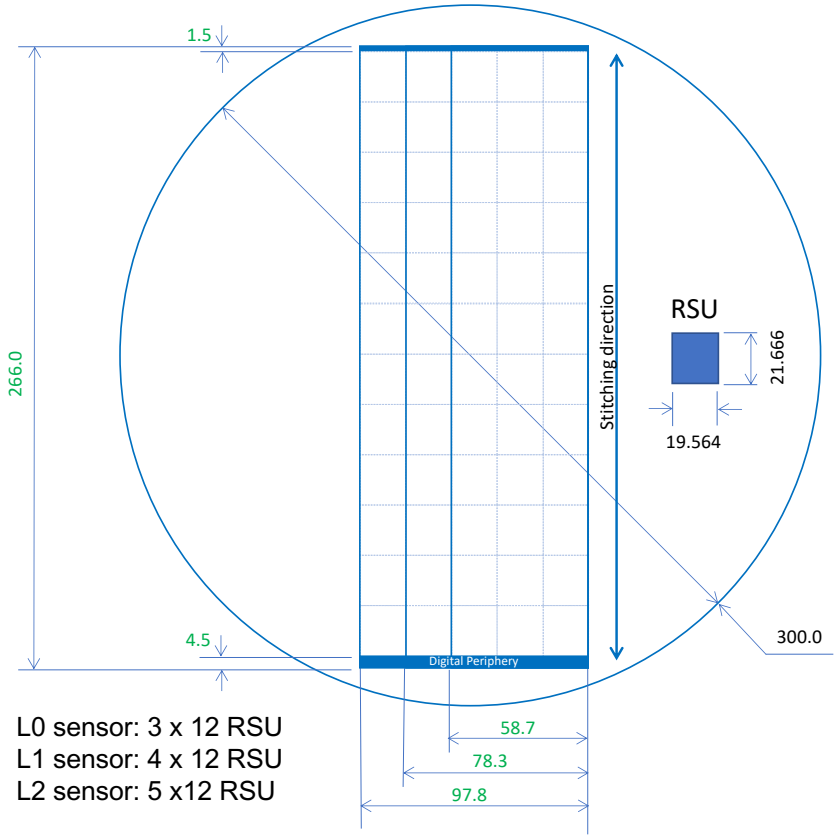
- **ER2** – Design ongoing, submission in 2024
  - **MOSAIX** sensor aims to satisfy ITS3 requirements
  - Not an evolution of MOSS/MOST; substantial redesign of existing circuits, with new features

- **ER3** – Production version
  - Minimal modifications to MOSAIX

MOSAIX

Charge 1, 2, 3

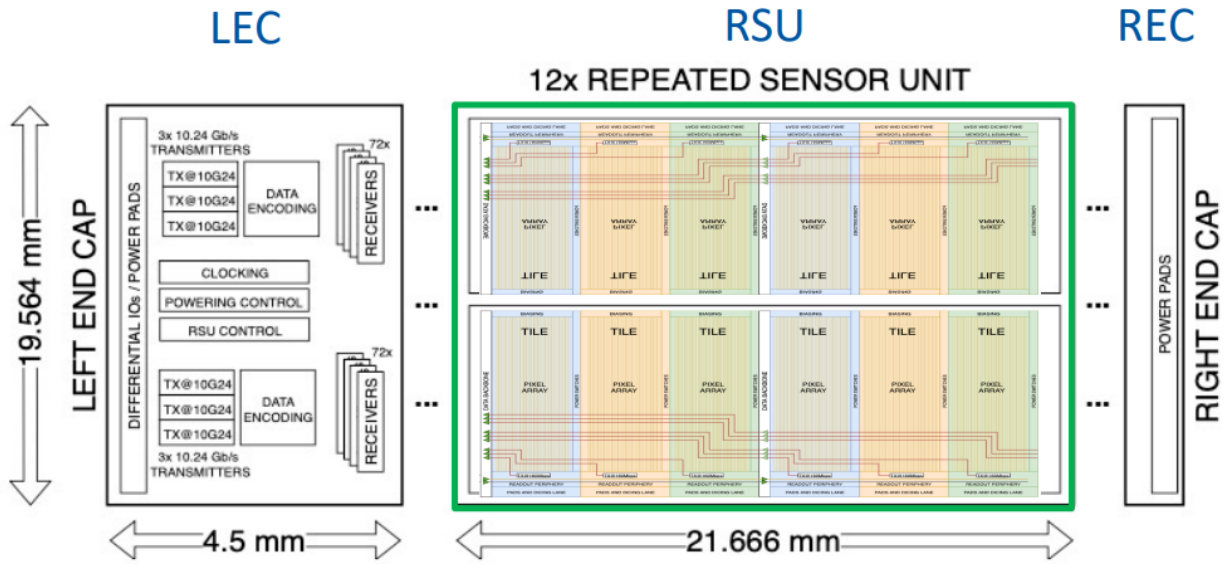
- Complex circuit designed, led by ITS3 team at CERN
  - Approximately 30 FTE of designers working on the submission, including ePIC SVT designers



L0 sensor: 3 x 12 RSU
L1 sensor: 4 x 12 RSU
L2 sensor: 5 x12 RSU

ER2 sensor widths

19.564 x 3 = 58.692
19.564 x 4 = 78.256
19.564 x 5 = 97.820



Pixel size: ~ 20 x 22 μm^2
Frame duration: 2 to 5 µs
Data link: 10.24 Gbps

EIC-LAS

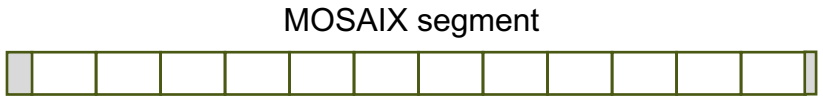
Charge 3, 4

- The ePIC SVT OB, EE and HE will cover an area of approximately 8 m^2
- A sensor design is needed for **low-cost, high acceptance, large area coverage**
- The EIC LAS sensor will be based off the ER2 and ER3 designs with modifications for use in the SVT
- Modifications of MOSAIX are kept to a minimum
  - Work within the available time and resources
  - Reduce risk of submission failure

MOSAIX to EIC-LAS

Charge 2

Inner Barrel



- 12 RSUs
- 8 data links
- 7 slow control links
- Direct powering

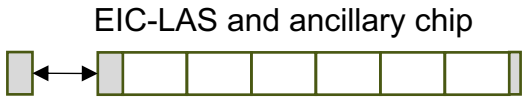
Improve yield and coverage →

Lower material budget →

Lower material budget, fit integration requirements →

Lower material budget, fit integration requirements →

Outer Barrel, E/H Endcaps



- **5 or 6 RSUs**
- **Single data link**

} EIC-LAS

- Multiplex slow control
- Serial powering

} Ancillary ASIC

Ancillary Chip

Charge 2, 3, 4

- The ancillary chip will provide sensor power, bias and slow control interfaces

- The main elements of this ASIC are
  - **SLDO** regulator for serial powering
  - Negative Voltage Generator (**NVG**) for sensor biasing
  - **Slow control** interface for low material communication to/from the control room

- It will be designed in a **180 nm SOI process**
  - No modification of MOSAIX needed for optimised, low material power, biasing and slow control
  - 4 MPW runs per year allowing for fast and cost-effective prototyping

Development status and plan

CERN/EIC agreement

Charge 2, 4

- Meeting at CERN in April 2023: EIC, ePIC SVT, ALICE ITS3 → Agreed on partnership

- Draft of agreement received in December 2023
  - Further discussions with ITS3 colleagues on ER2 and ER3 sensors procurement
  - Now with BNL legal

- The agreement provides a collaborative framework around four main points
  - **Procurement of components** for the EIC ePIC detector
  - **Participation in the design** of the Pixel Sensor Chip for the ALICE ITS3
  - **Transfer of the design database** of the ITS3 sensor to BNL
  - **Contribution to other CERN activities** related to the ALICE ITS3

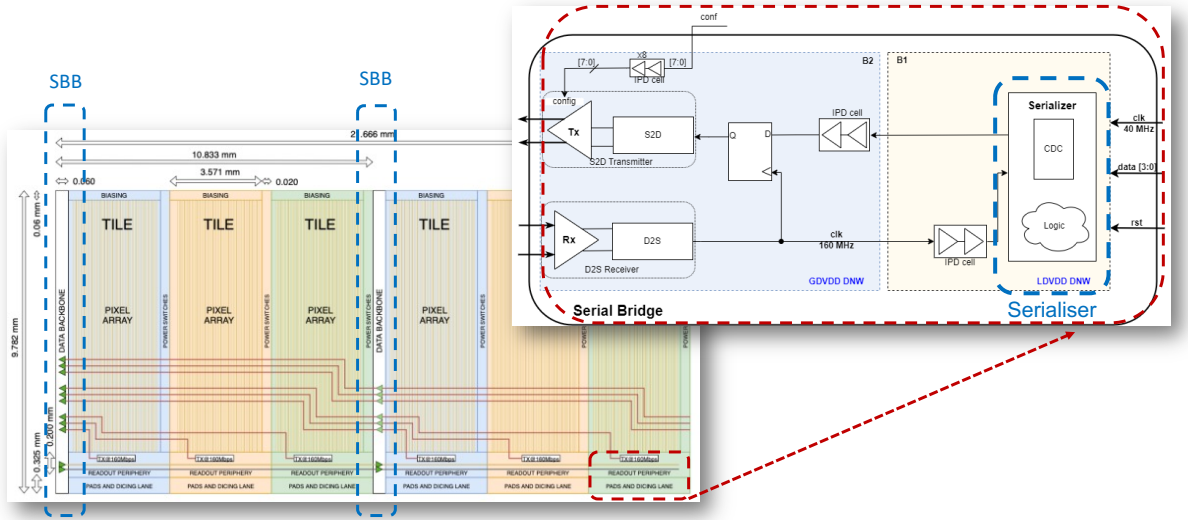
Designers' group

- Two sensor designers affiliated with ePIC institutions (BNL, MIT) are embedded in the ITS3 team at CERN
  - As per CERN/EIC agreement
  - Transfer of knowledge to the ePIC designers for EIC-LAS
- Complemented with team of experienced designers in the UK (RAL) and the US (BNL, LBNL)
- By-weekly WP1 Sensor Design meetings (I. Sedgwick, RAL; J. De Melo, BNL)
- Tools for collaborative work in place and being set up
  - Cliosoft being setup by BNL for collaborative working on sensor designs
  - Action tracker, specification document, schedule gannt project, shared document repository

MOSAIX Design – ePIC contributions

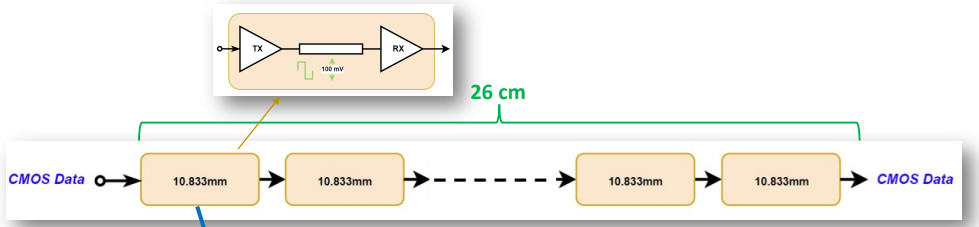
- Development of **logic libraries**
  - Enhanced Design for Manufacture (DfM) rules, reduced leakage current for improved power consumption, specialised cells for use in the pixel array
  - Overall management of the effort, library generation (netlists, abstracts etc) and verification of the generated cells by ePIC SVT designers, with layout work split across several institutes on the MOSAIX team

- Work on MOSAIX tile circuitry
  - Stitched backbone
  - Tile serialiser

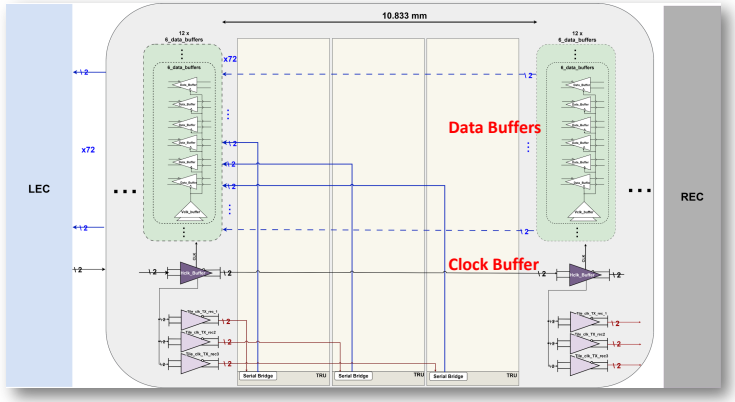


MOSAIX Design – ePIC contributions

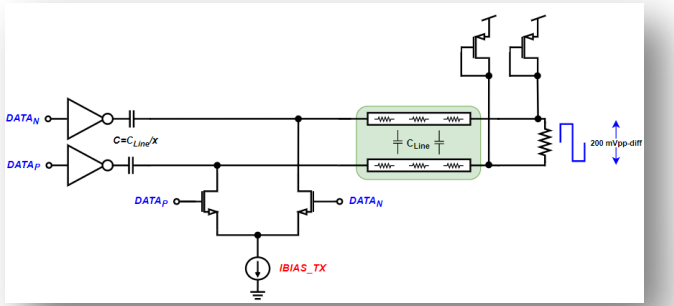
- **Stitched backbone design**

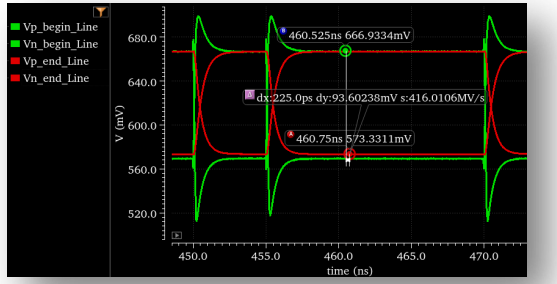


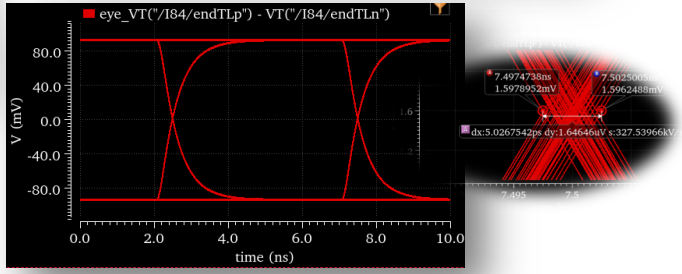
SBB floorplan



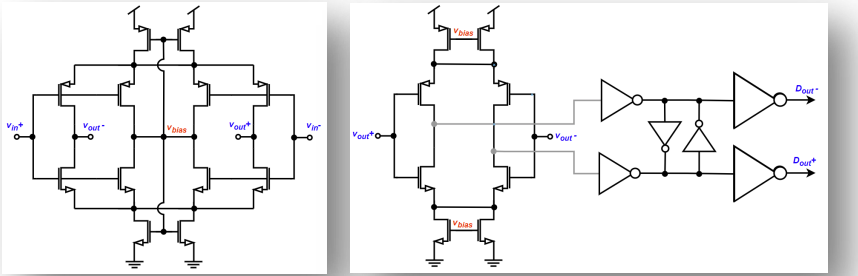
SBB – 160MHz **Clock/Data** Buffer TX





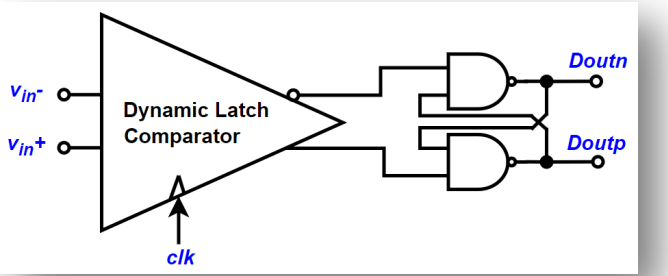


SBB – 160MHz **Clock** Buffer RX



Continuous time comparator

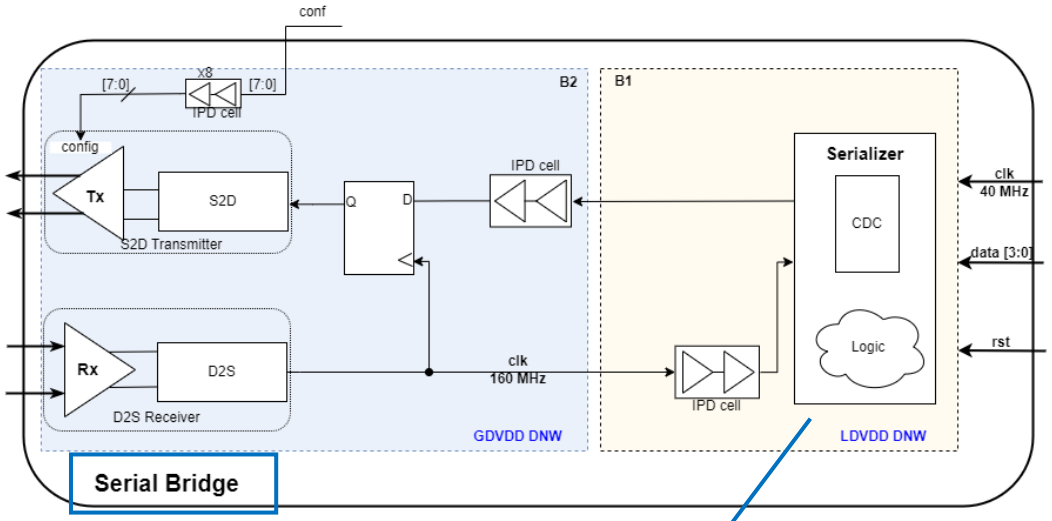
SBB – 160MHz **Data** Buffer RX



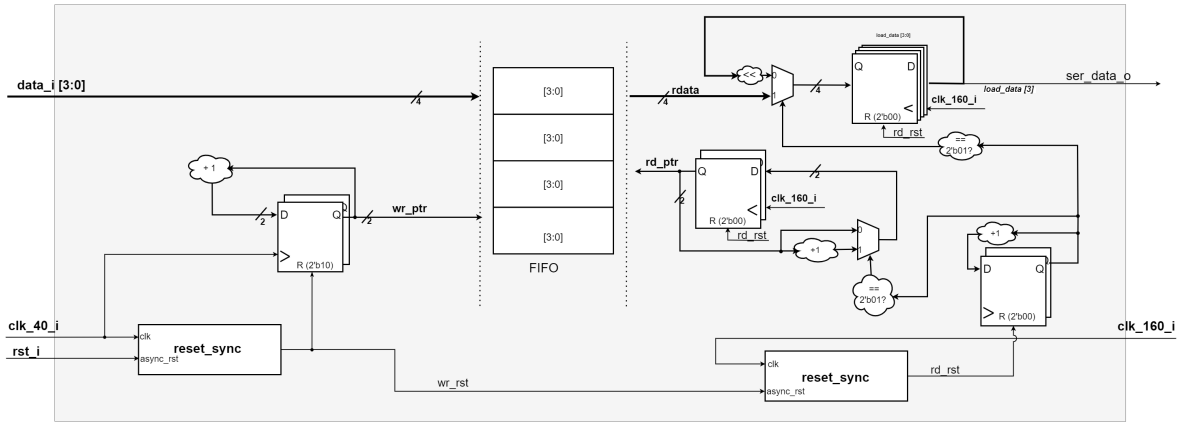
Clocked comparator

MOSAIX Design – ePIC contributions

- **Tile serialiser**
  - Digital design of tile serializer and its integration inside the tile periphery (i.e. serial bridge)
  - Digital implementation flow of the tile periphery



- Liberate characterization of the SBB to LEC and SBB to tile periphery interfaces



EIC-LAS

Charge 1, 2

- Specification capture in progress
- Access to MOSAIX database needed to start work
  - Pending progress with agreement signature

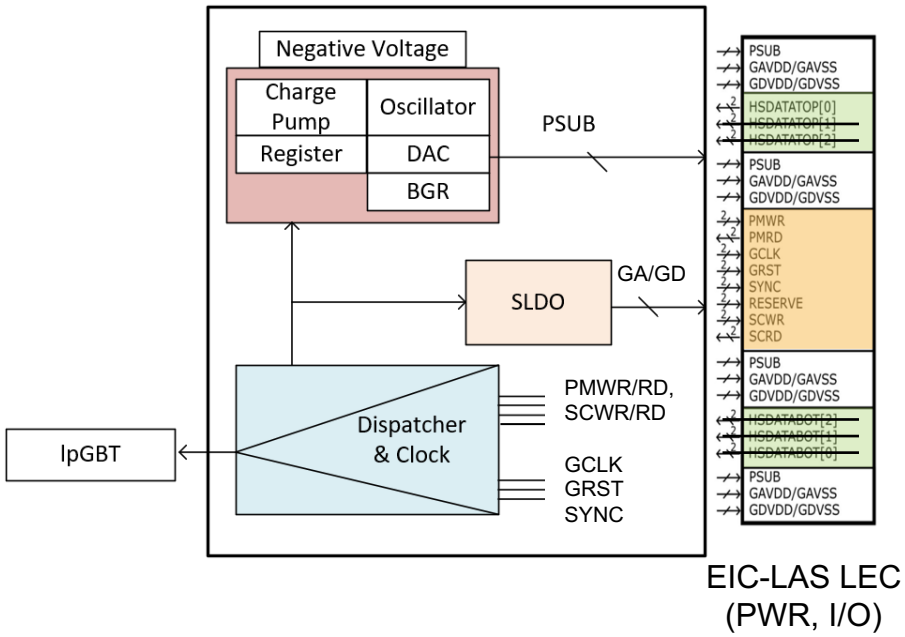
65nm EIC-LAS Specification				
Specification	Unit	Value	Comment	Status
Number of RSUs	N/A	5-6 (TBD)		
Output Data Channels	N/A	1-2	1 if no redundancy, 2 if redundancy desired	
Data Output Speed	Gbit/s	10		
Power	W			
Supply Voltage	A			
Area	μm^2			

- Estimated power consumption range: 1.2 – 1.6 W per EIC-LAS
  - Derived from evolving MOSAIX power figures
  - This estimate takes into account the reduction in the number of RSUs
  - LEC power consumption not yet scaled to reflect the reduction in the number of data links
    - More information needed on power consumption of various LEC blocks
    - Significant reduction in power consumption expected

Ancillary ASIC - Overview

Charge 1, 2

Ancillary ASIC
High level block diagram



EIC-LAS LEC
(PWR, I/O)

Negative Bias Generator Specification				
Specification	Unit	Value	Comment	Status
Voltage Range	V	0 to -6	Relative to local ground	
Current Capacity	A	10^{-3}		
Voltage Ripple	mV	< 0.1		
Power	W	$< 10^{-2}$		
Supply Voltage	V	1.8		
Area	μm^2	4×10^5		

Shunt LDO Specification				
Specification	Unit	Value	Comment	Status
Voltage Output	V	1.1 - 2.0		
No. of Channels		5	Includes 1 to drive rest of ancillary chip	
Current Capacity per channel	A	0 - 1.5		
Voltage Ripple	mV			
Power	W			
Supply Voltage	A			
Area	μm^2			
Min-Max Input Current Slew Rate	A/s			
Min-Max Equivalent Load Resistance	ohm			
Over-Voltage Limit	V	2.5		
Max Current @ Over-Voltage Limit	A	2		

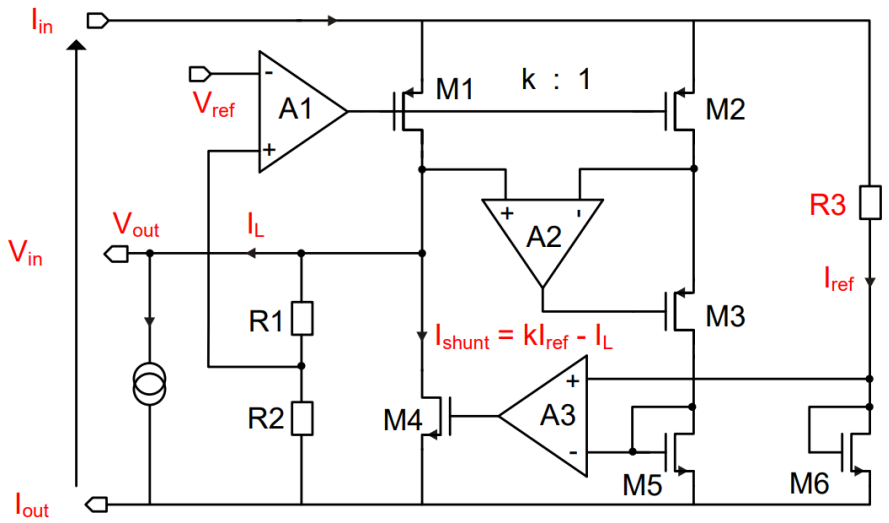
Slow Control Multiplexer Specification				
Specification	Unit	Value	Comment	Status
Input Signals	N/A	TBD		
Output Signals	N/A	PM Bus • PMWR • PMRD SC Bus • SCWR • SCRD GCLK GRST SYNC RESERVE	• CERN Low Power Signalling Compliant • Manchester Encoding • Exact details need to be confirmed with MOSAIX	
Voltage Ripple	mV			
Power	W			
Supply Voltage	A			
Area	μm^2			

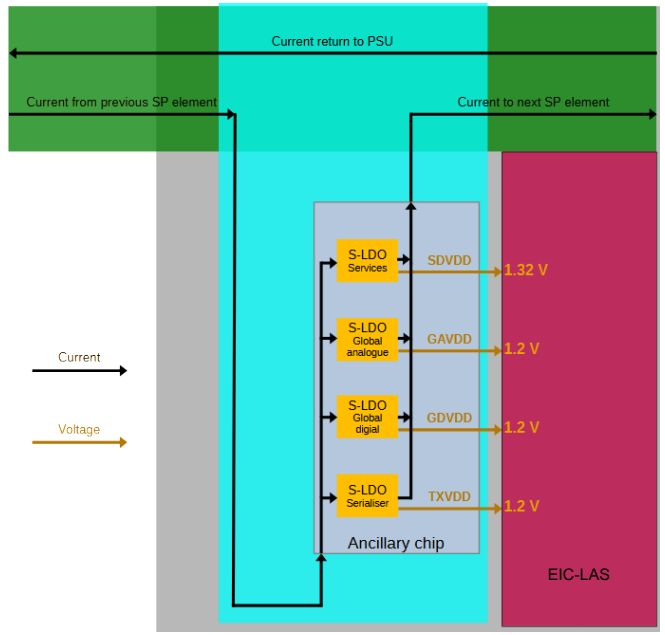
- Estimated power consumption: up to 50% of EIC-LAS power
  - Dominated by SLDO regulators
    - Based on MOSAIX/EIC-LAS current needs as estimated at this time
  - Further optimisations considered for a more efficient current to voltage conversion

Ancillary Chip - SLDO

- Current to voltage conversion to power the EIC-LAS in serial powering

- Design adapted from ATLAS/CMS Serial Powering SLDO design for the HL-LHC
  - > 10 years development, multiple prototypes in different technologies
  - Robust design, failure modes addressed to safeguard SP chain from failures of one regulator
  - No need for bypassing element in the SP chain

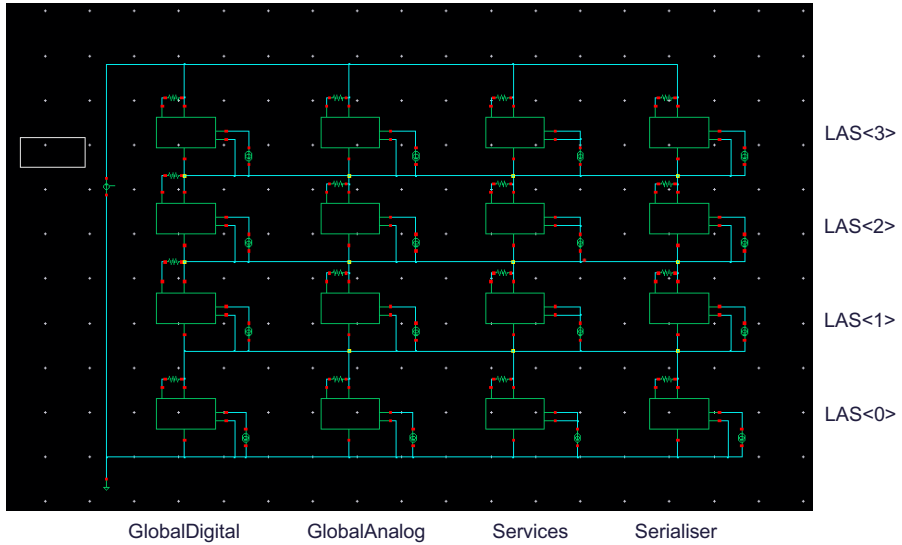


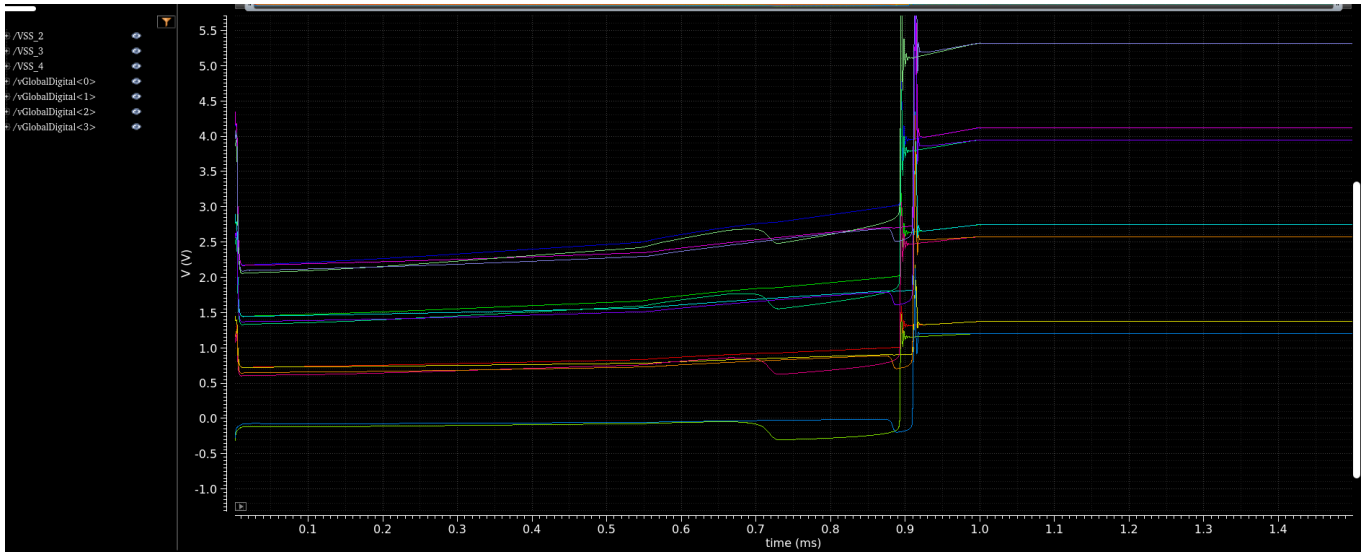


Ancillary Chip - SLDO

- Functional schematic implemented in 65 nm technology adapted to recent MOSAIX current consumption figures
  - Simulations include stave power model to inform SVT development

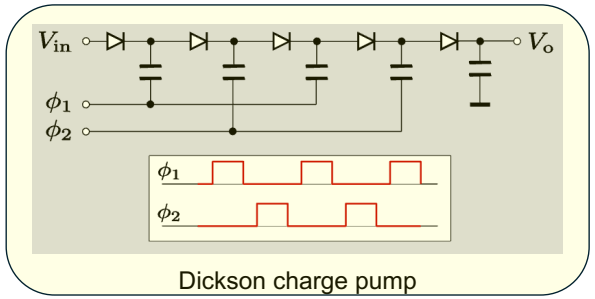
- Next: Additional features (tri-state, over-voltage protections etc.); port to 180 nm technology; full verification; layout; tape-out





Ancillary Chip - NVG

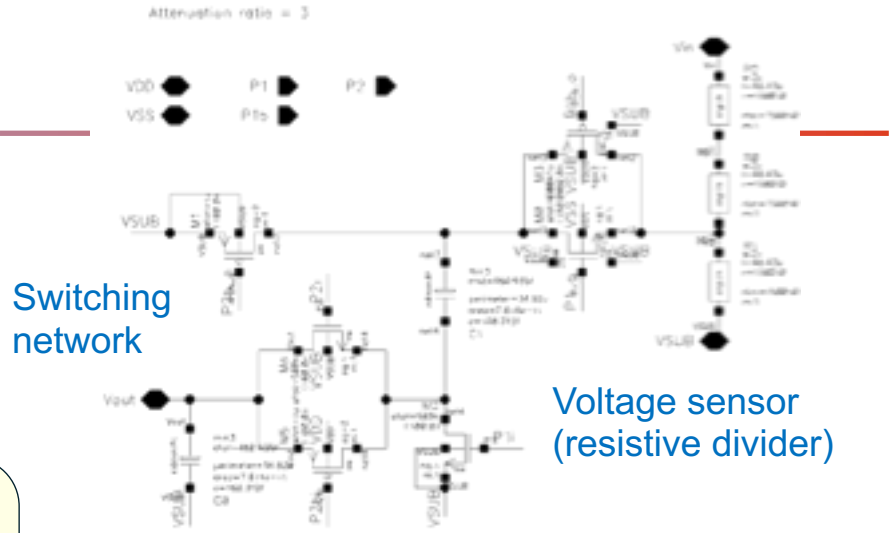
- Creates the **negative bias for charge collecting volume** from positive regulated power supply 1.2 V
  - Diode-based charge-pump circuit

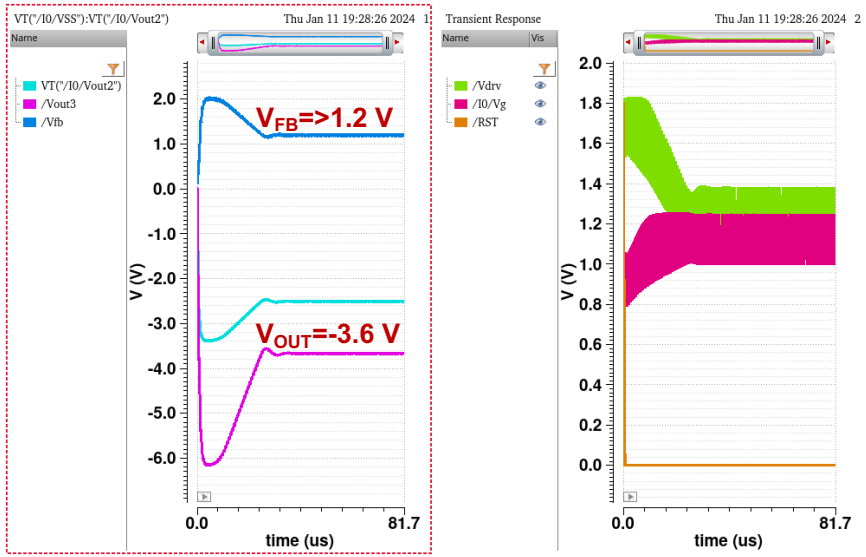


Dickson charge pump

- Circuit design progressed to **demonstration of feasibility**

- Next: realistic model of output load; corner and MC simulations; voltage DAC to generate VREF; trial layout and impact of layout parasitics; ELT transistors for radiation-hardness





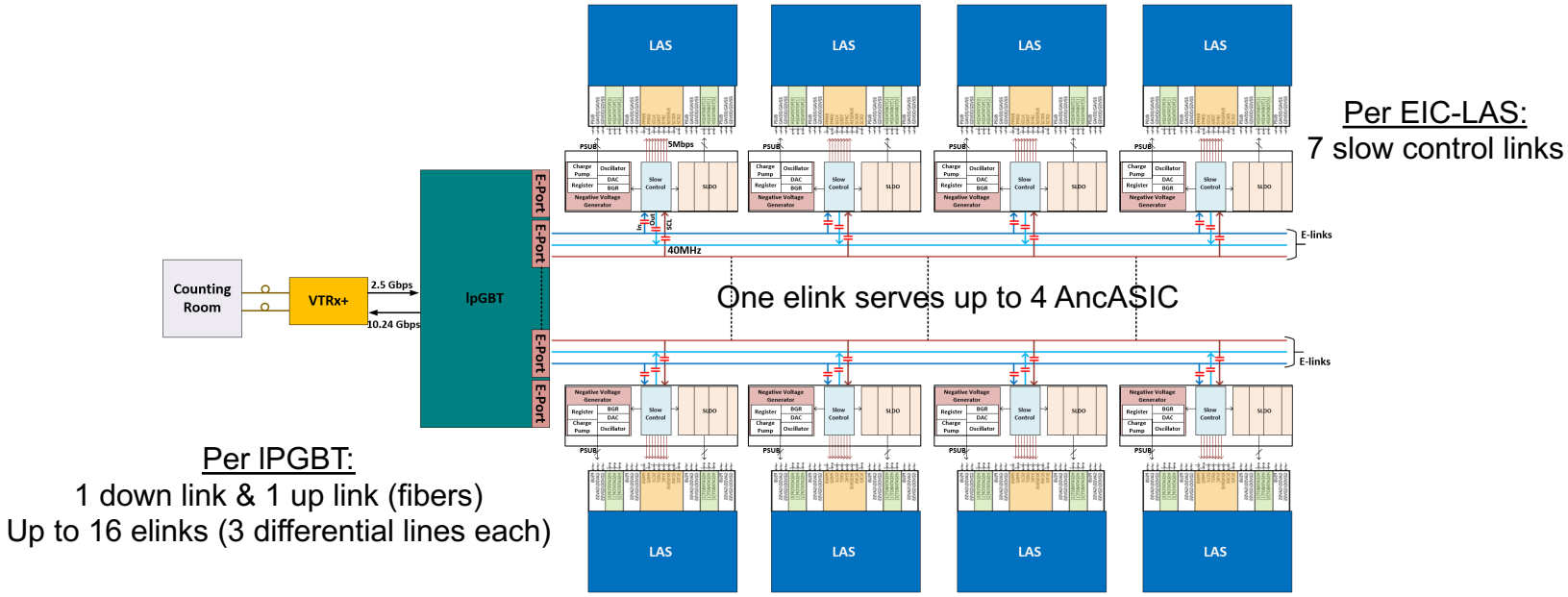
Closed-loop simulations V_{REF}=1.2 V

- V_{OUT} = -V_{REF}/α = -3 × V_{REF} = -3.6V.
- C_L = 10 pF (small value w.r.t. real to reduce $T_{simulation}$).

Ancillary Chip – Slow Control

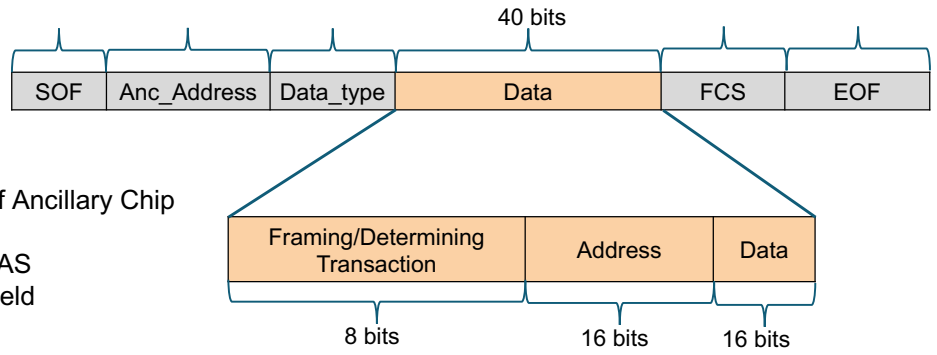
- Need to reduce number of EIC-LAS slow control links for material reduction and to fit within SVT assigned FELIX channels - See Jo's talk

- AncASIC slow control circuit interfaces with EIC-LAS on one side and lpGBT on the other side

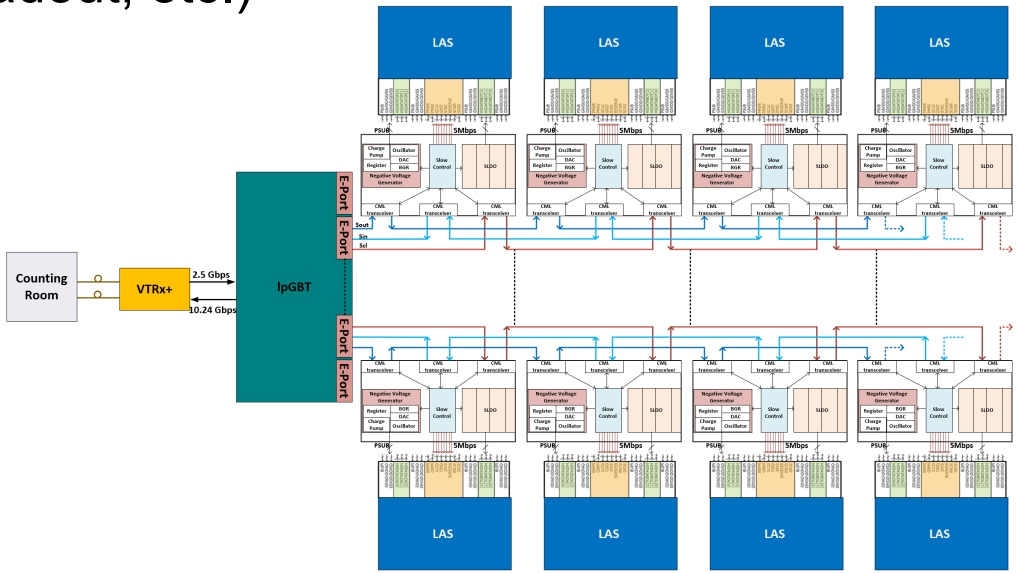


Ancillary Chip – Slow Control

- Current work focused on defining **protocol and specs for communication between lpGBT and AncASIC**
  - Matching of clock speeds of eLink and EIC-LAS, buffering of data inside AncASIC
  - lpGBT data format to include addresses of AncASIC and EIC-LAS data structure
  - Internal configuration of AncASIC
  - Data integrity methodology (checksums, correction, triplication, read back)
  - Built in fast commands (reset, synchronize, status readout, etc.)
  - AC vs DC-coupled communication



SOF: Start of Frame
Anc_Address: Address of Ancillary Chip
Data_Type: Read/Write
Data: To MOSAIX / EIC-LAS
FCS: Frame Checksum Field
EOF: End of Frame



Sensor Testing

Charge 7

- Effort coordinated within the ePIC SVT WP2 Sensor Testing (G. M. Innocenti, MIT; L. Tomasek, CTU Prague)
  - **Covers ITS3 sensors, EIC-LAS and AncASIC, including test setups development**
- Characterisation of prototypes
  - Tests in labs and test beams
  - Development of wafer probing capability for production
  - Irradiations at SVT facilities
- Production testing/QA
  - Probing of all ER3, EIC-LAS production, AncASIC production wafers

Sensor Testing - Facilities

- Clean rooms and labs equipped with radioactive sources, climate chambers, wire bonders, wafer probers, etc

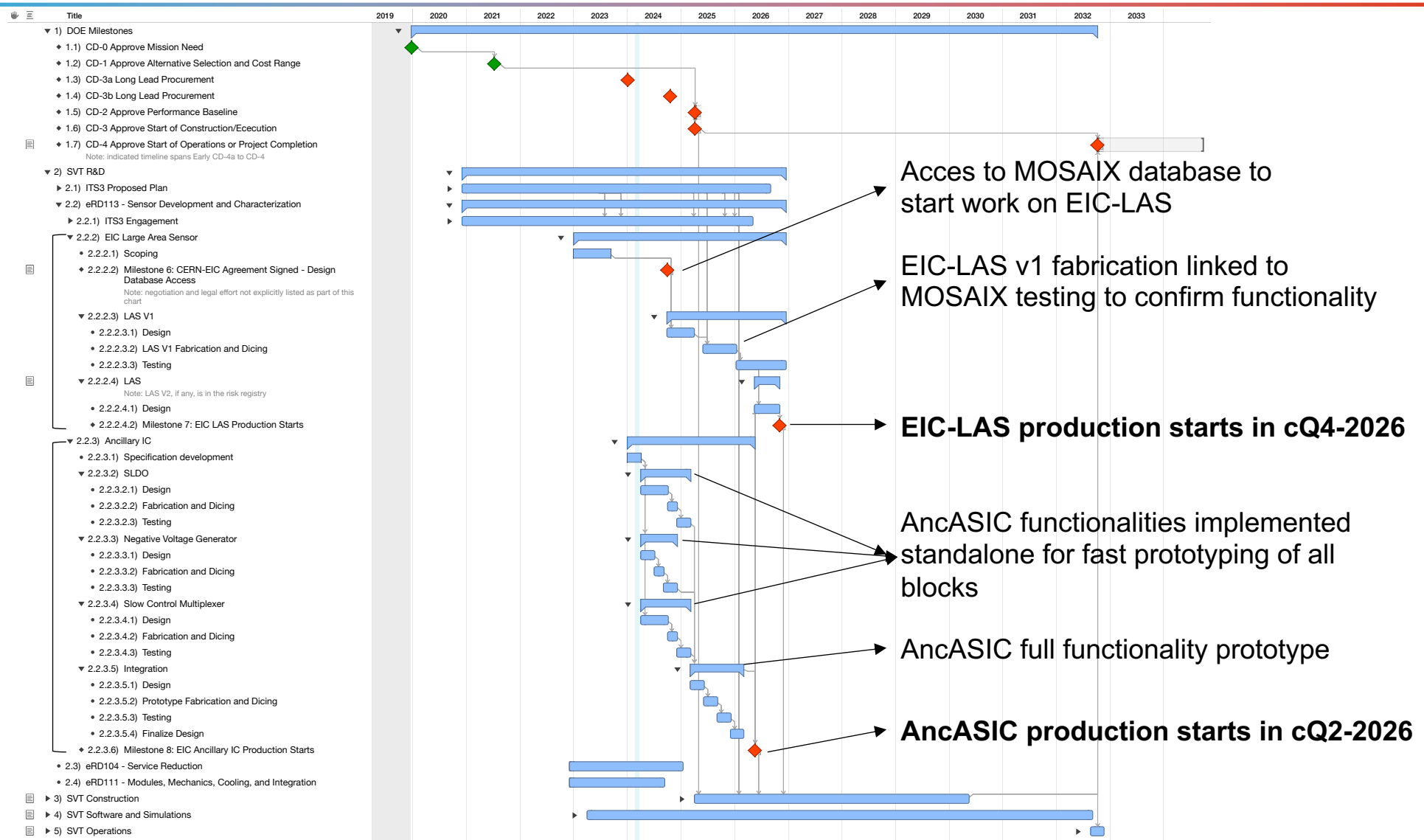
- Irradiation facilities in the collaboration available for displacement damage, TID and SEE testing
  - Birmingham: 27 MeV protons, upcoming neutron irradiation facility
  - CTU Prague: X-ray source, slow and fast neutrons
  - UJP Prague: Cobalt-60 gamma ray
  - Nuclear Physics Institute CAS Rez: reactor neutrons, ~30 MeV proton and heavy ion beam, electrons up to 25 MeV
  - LBNL: BASE @ 88” cyclotron (protons, heavy ions, neutrons)
  - Daresbury lab: X-ray source
  - LANL: 800 GeV protons

Schedule

IB wafer scale sensor

EIC-LAS

Ancillary ASIC



N.B.: calendar quarters

Summary

- MAPS detectors in 65 nm CMOS imaging technology have been identified to meet the tracking requirements at ePIC
- The ePIC SVT will be built wafer-scale ITS3 sensors in the IB and the ITS-3 derived EIC-LAS in the OB, complemented by the AncASIC for low mass power and slow interfaces
- The choice of these sensors has taken into accounts reduction of cost and risks, and EIC schedule, in addition to performance

Summary

- ePIC SVT designers are actively involved in the development of the ITS3 MOSAIX sensors
- Specification capture for the EIC-LAS and AncASIC is advancing, with progress on the design of AncASIC circuit blocks
- The sensor development schedule is in agreement with the EIC Critical Decisions timeline