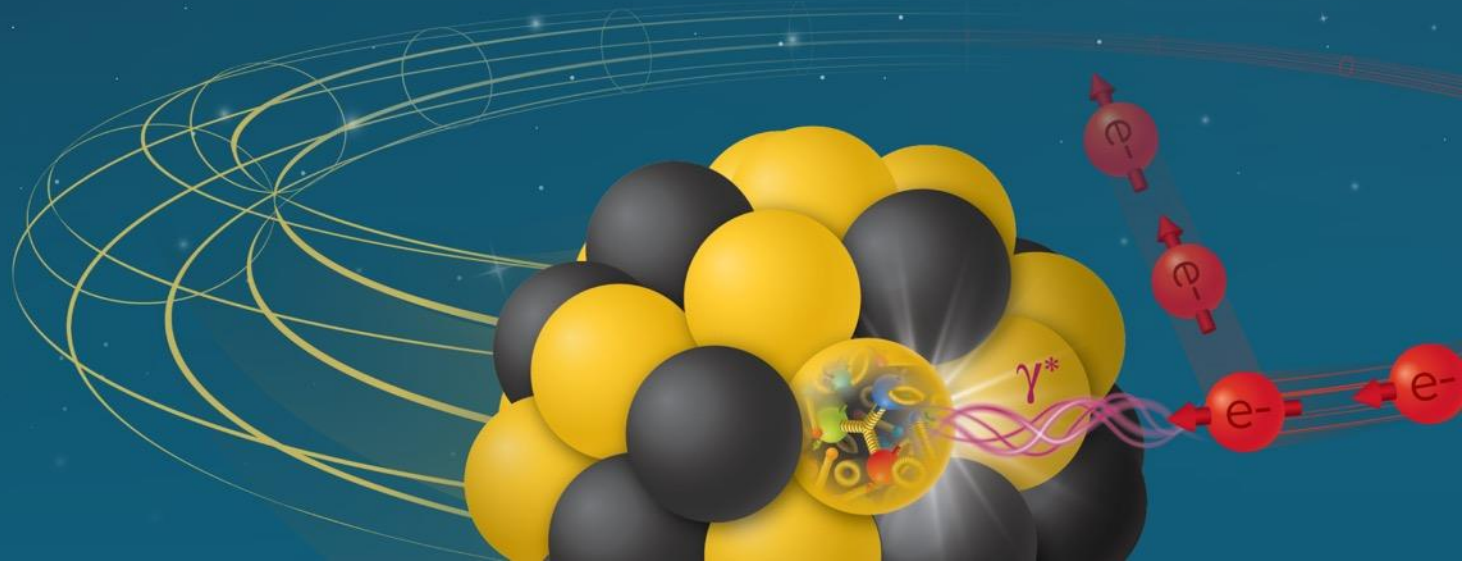
Silicon: Readout

Joachim Schambach
SVT Readout and Powering Work Package Co-Coordinator
Oak Ridge National Laboratory

Incremental Design and Safety Review
of the EIC Tracking Detectors
March 20-21, 2024

Electron-Ion Collider



Charge Questions Addressed

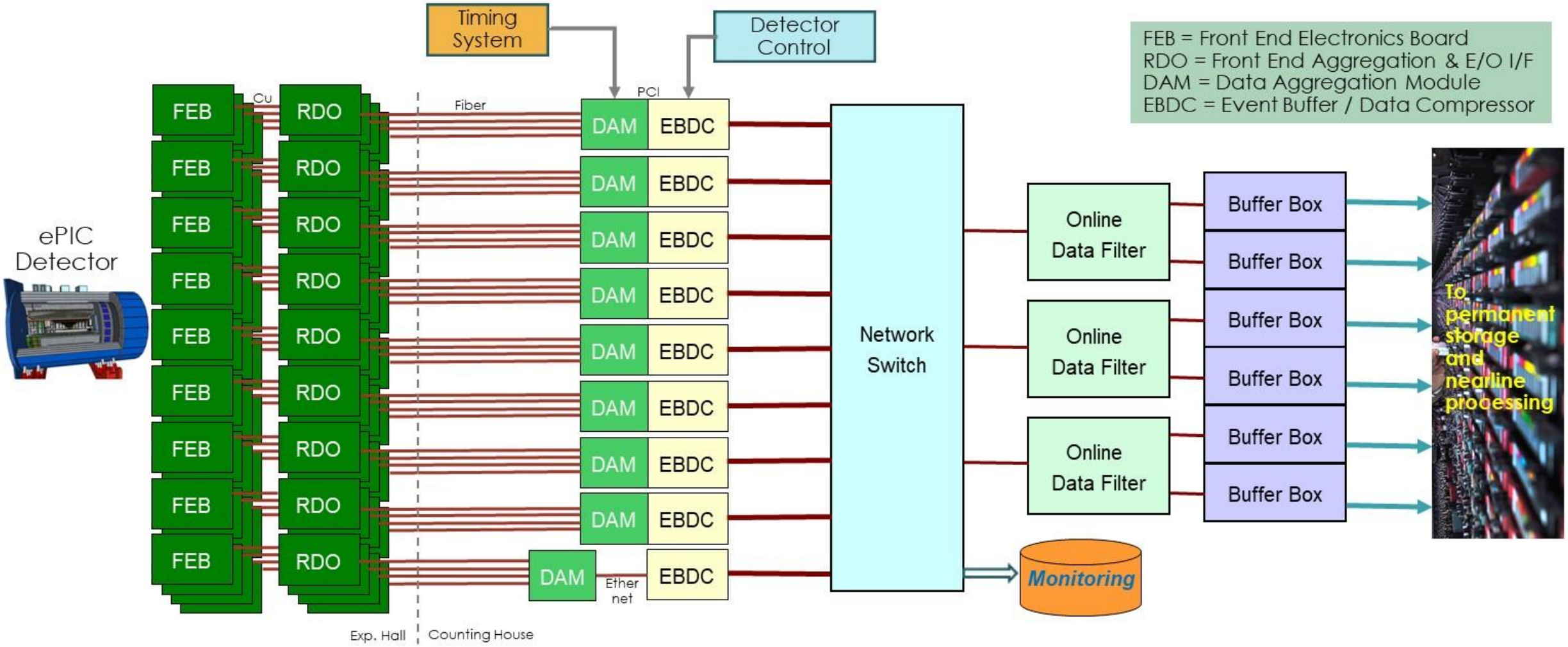
1. Are the technical performance requirements appropriately defined and complete for this stage of the project?
2. Are the plans for achieving detector performance and construction sufficiently developed and documented for the present phase of the project?
3. Are the current designs and plans for detector, electronics readout, and services sufficiently developed to achieve the performance requirements?
4. Are plans in place to mitigate risk of cost increases, schedule delays, and technical problems?
5. Are the fabrication and assembly plans for the various tracking detector systems consistent with the overall project and detector schedule?
6. Are the plans for detector integration in the EIC detector appropriately developed for the present phase of the project?
7. Have ES&H and QA considerations been adequately incorporated into the designs at their present stage?

Outline

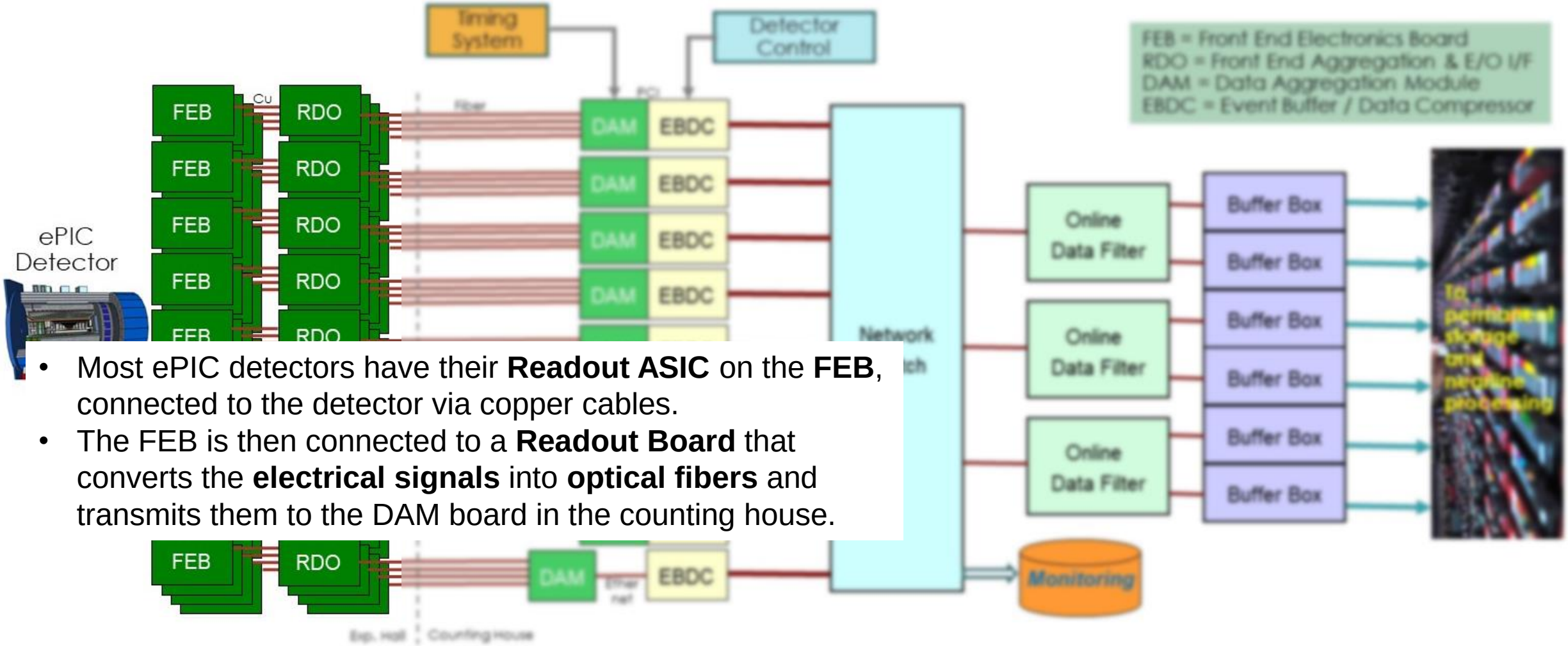
- Top Level Readout Design
- Inner Barrel Readout Design
- Outer Barrel and Disk Readout Design
- SVT Numbers
- Prototype Developments
- Summary

Top Level Readout Design

ePIC Streaming DAQ for SVT

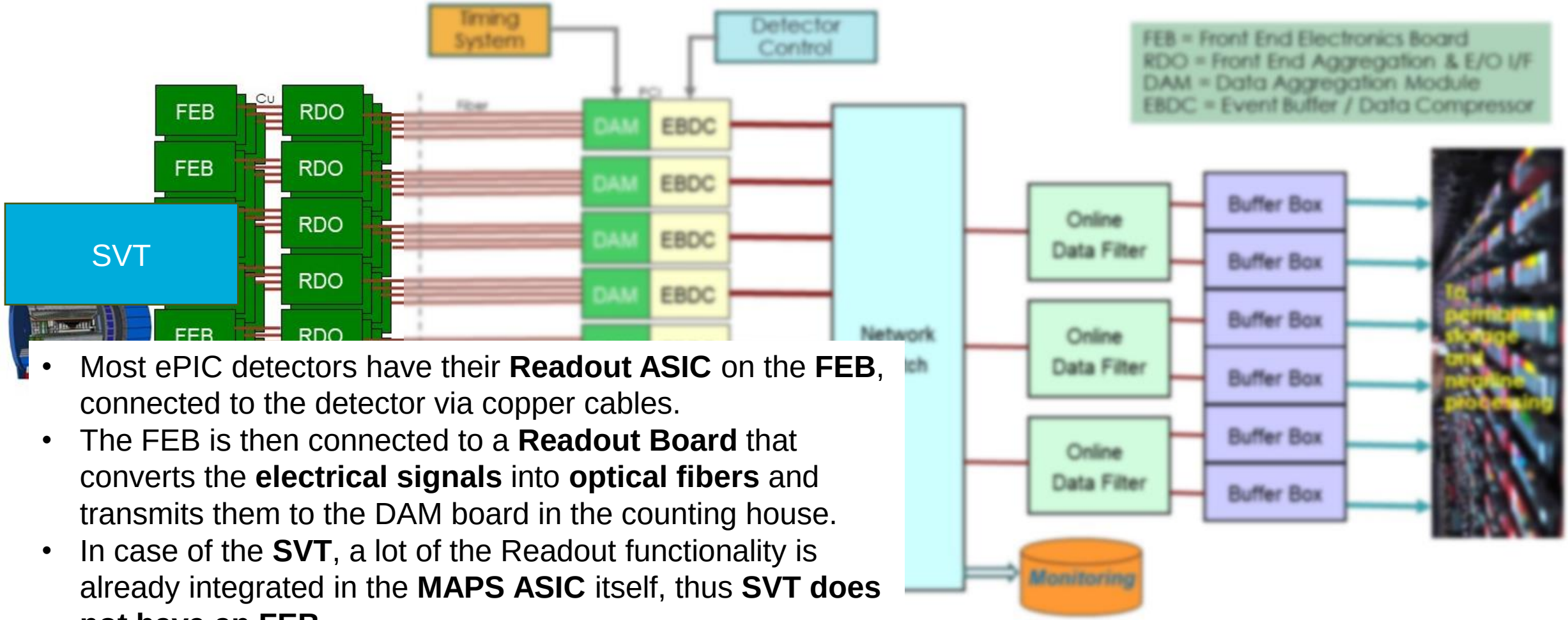


ePIC Streaming DAQ for SVT



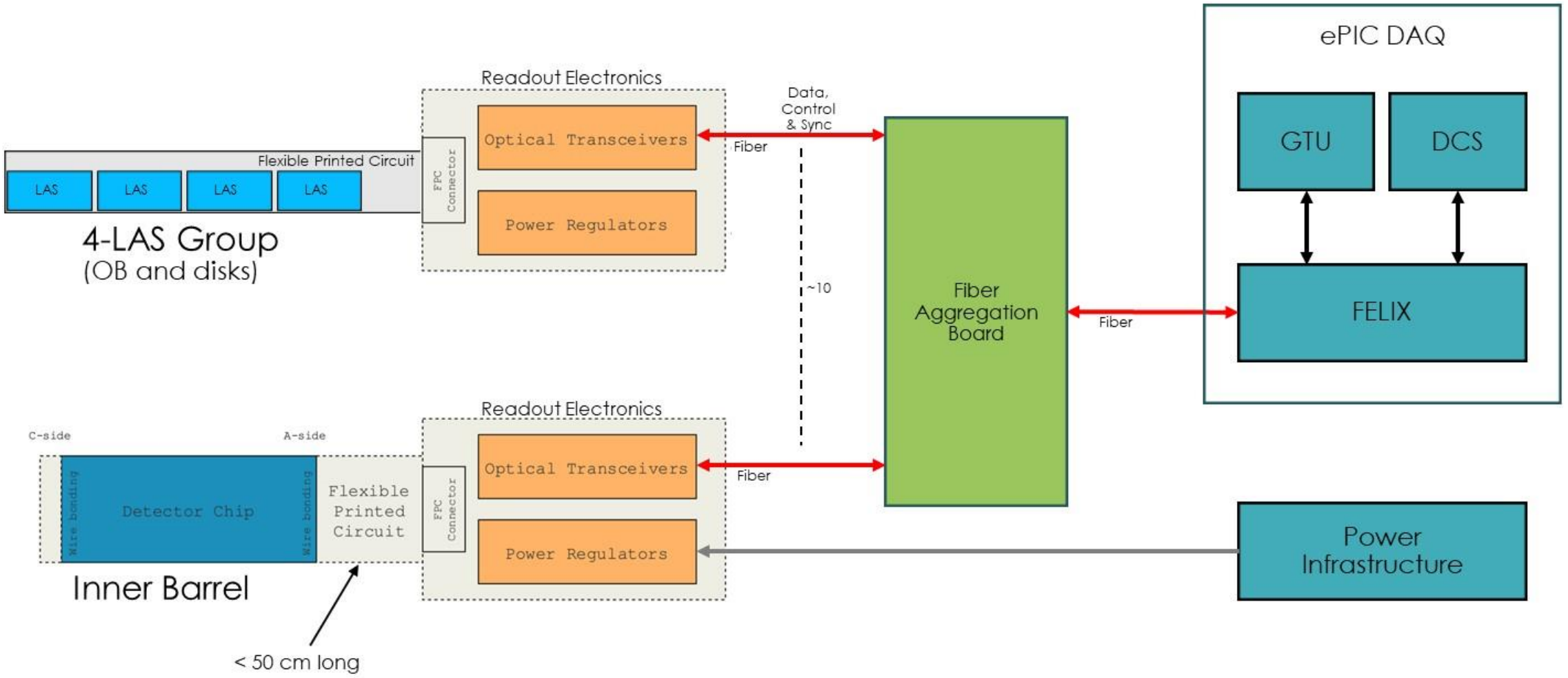
- Most ePIC detectors have their **Readout ASIC** on the **FEB**, connected to the detector via copper cables.
- The FEB is then connected to a **Readout Board** that converts the **electrical signals** into **optical fibers** and transmits them to the DAM board in the counting house.

ePIC Streaming DAQ for SVT

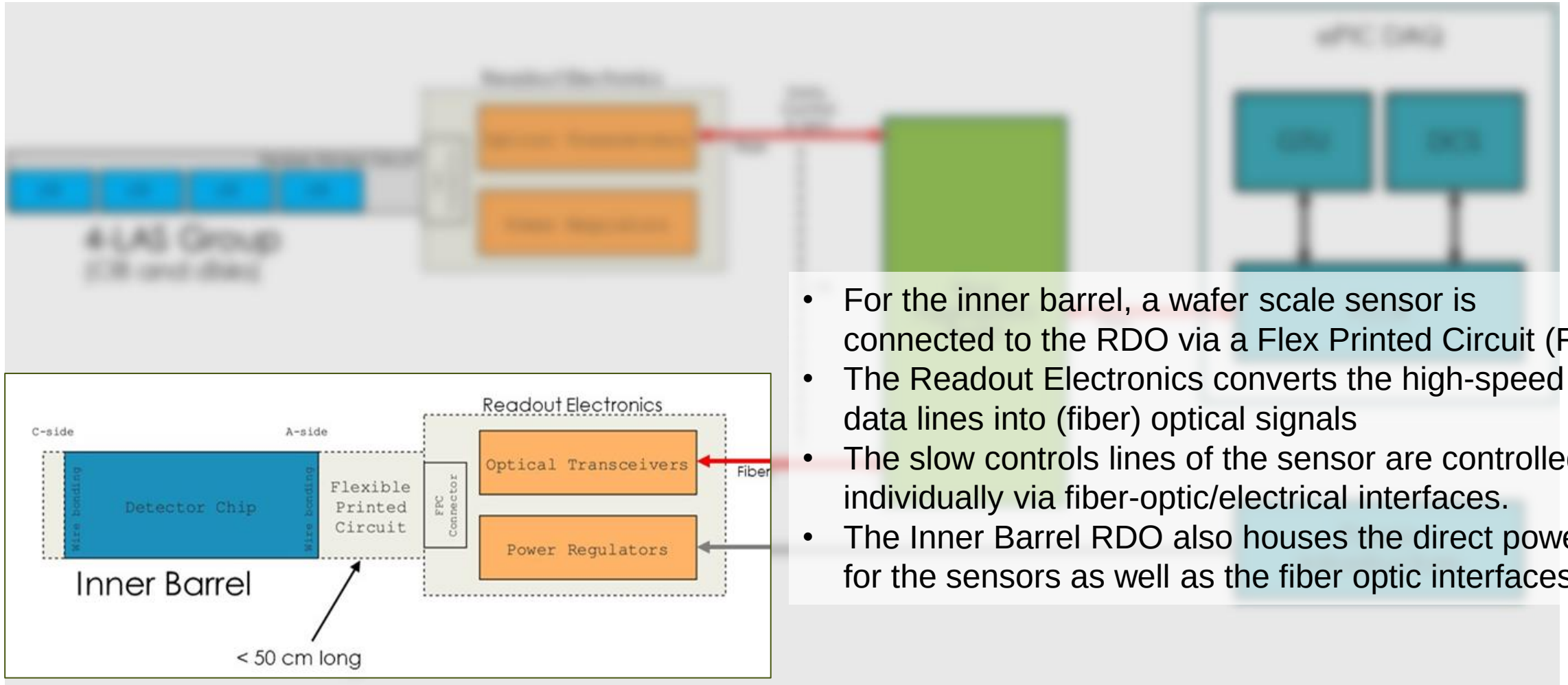


- Most ePIC detectors have their **Readout ASIC** on the **FEB**, connected to the detector via copper cables.
- The FEB is then connected to a **Readout Board** that converts the **electrical signals** into **optical fibers** and transmits them to the DAM board in the counting house.
- In case of the **SVT**, a lot of the Readout functionality is already integrated in the **MAPS ASIC** itself, thus **SVT does not have an FEB**

SVT Electronics for Data & Control

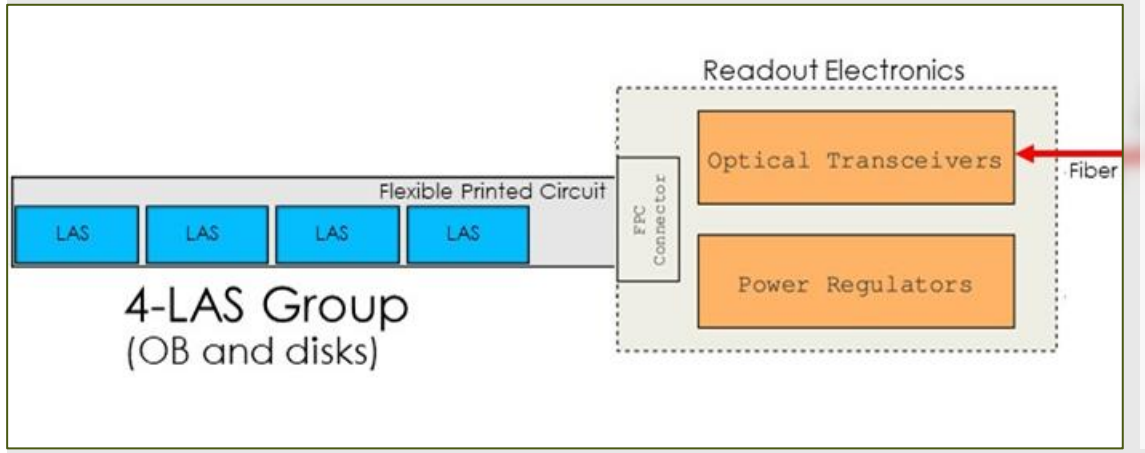


SVT Electronics for Data & Control



- For the inner barrel, a wafer scale sensor is connected to the RDO via a Flex Printed Circuit (FPC)
- The Readout Electronics converts the high-speed data lines into (fiber) optical signals
- The slow controls lines of the sensor are controlled individually via fiber-optic/electrical interfaces.
- The Inner Barrel RDO also houses the direct powering for the sensors as well as the fiber optic interfaces

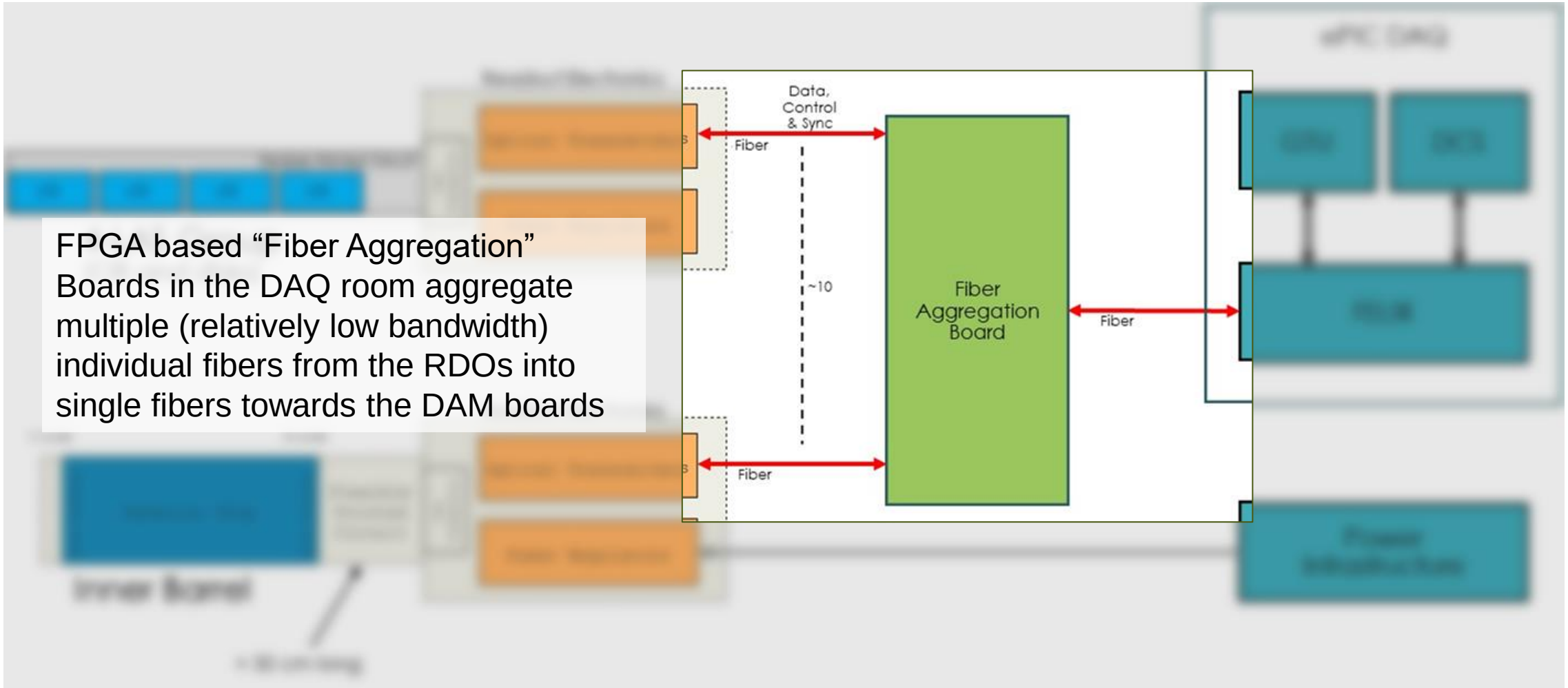
SVT Electronics for Data & Control



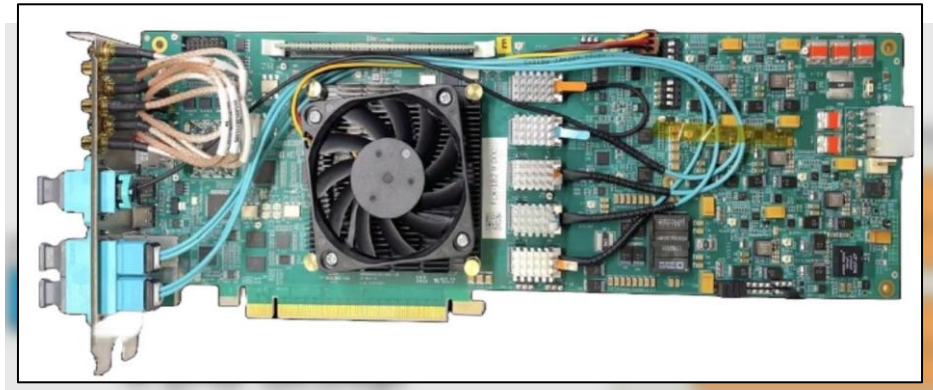
- For the Outer Barrel staves and the disks, the RDO converts groups of up to 4 SVT LAS high-speed lines to fiber optic signals.
- The slow control lines of the whole 4-LAS group are connected to electric/fiber optic interfaces.
- The groups of LASs use serial powering, so the power section of the RDO is solely for the RDO electronics itself.

SVT Electronics for Data & Control

FPGA based “Fiber Aggregation” Boards in the DAQ room aggregate multiple (relatively low bandwidth) individual fibers from the RDOs into single fibers towards the DAM boards

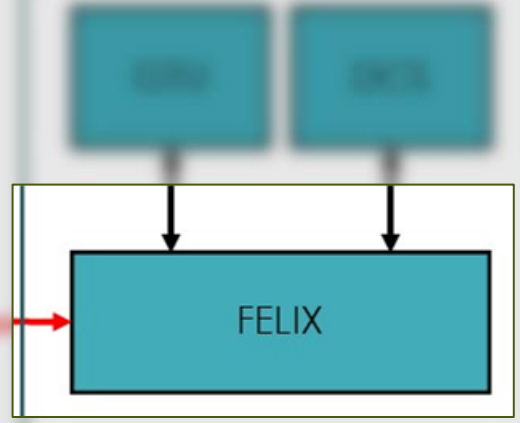


Backend: ATLAS FELIX Development for Phase-2 Upgrade



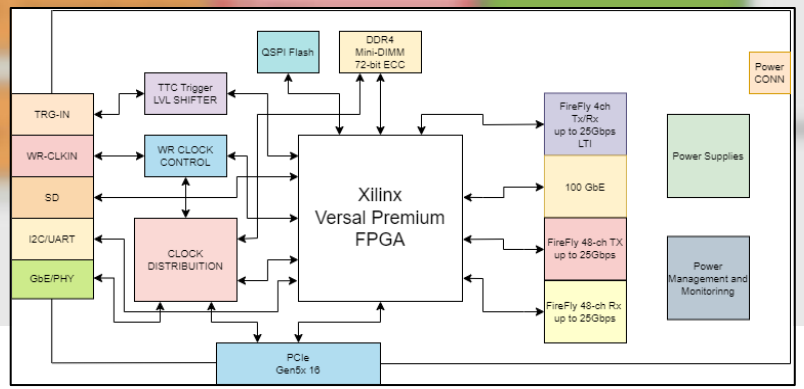
FELIX – FLX-182

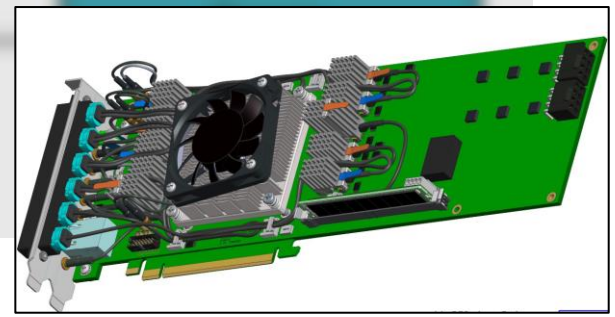
- FPGA: AMD Versal Prime VM1802
- PCIe Gen4x16 interface (240 Gb/s)
- 4 FireFly transceivers with 3 possible configurations
  - 24 links up to 25 Gb/s
  - 24 links up to 10 Gb/s (CERN-B FireFly)
  - One duplex FireFly transceiver with 2 possible configurations with 14 or 25 Gb/s



FELIX – FLX-155

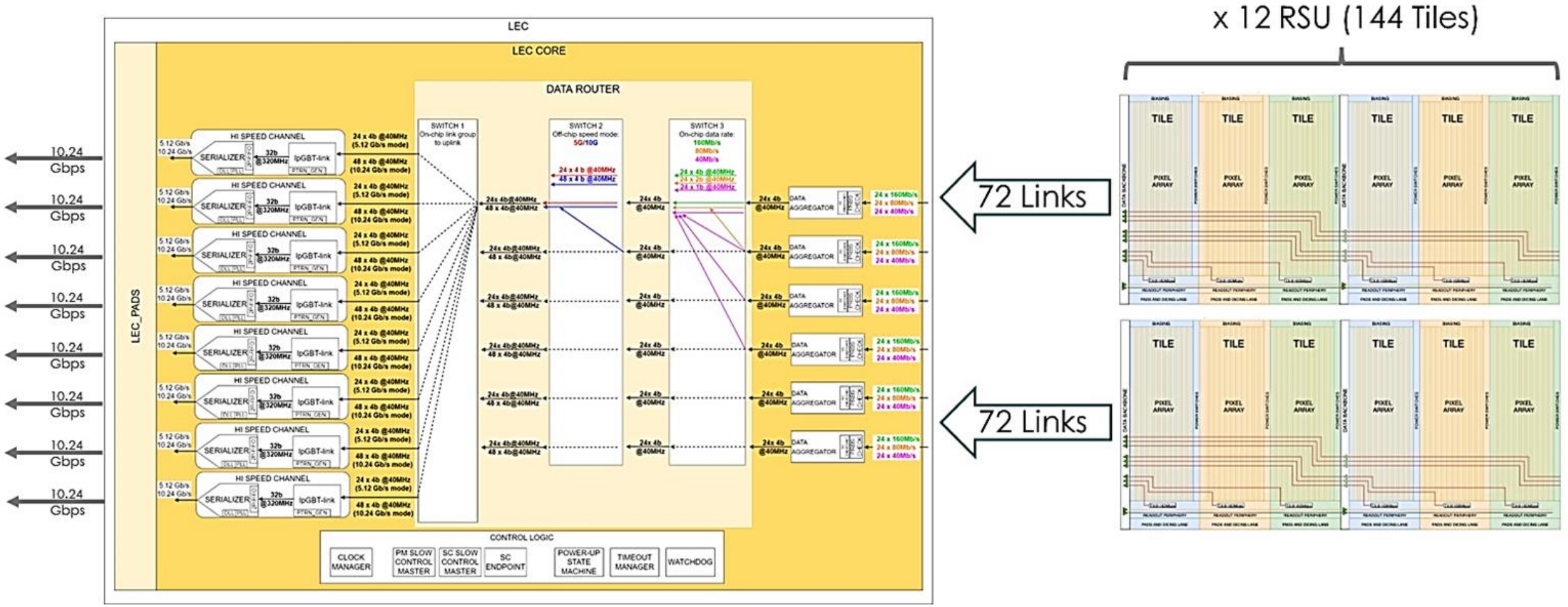
- FPGA: AMD Versal Premium VP1552 FPGA
- PCIe Gen5x16 interface (482 Gb/s)
- up to 48 bidirectional links





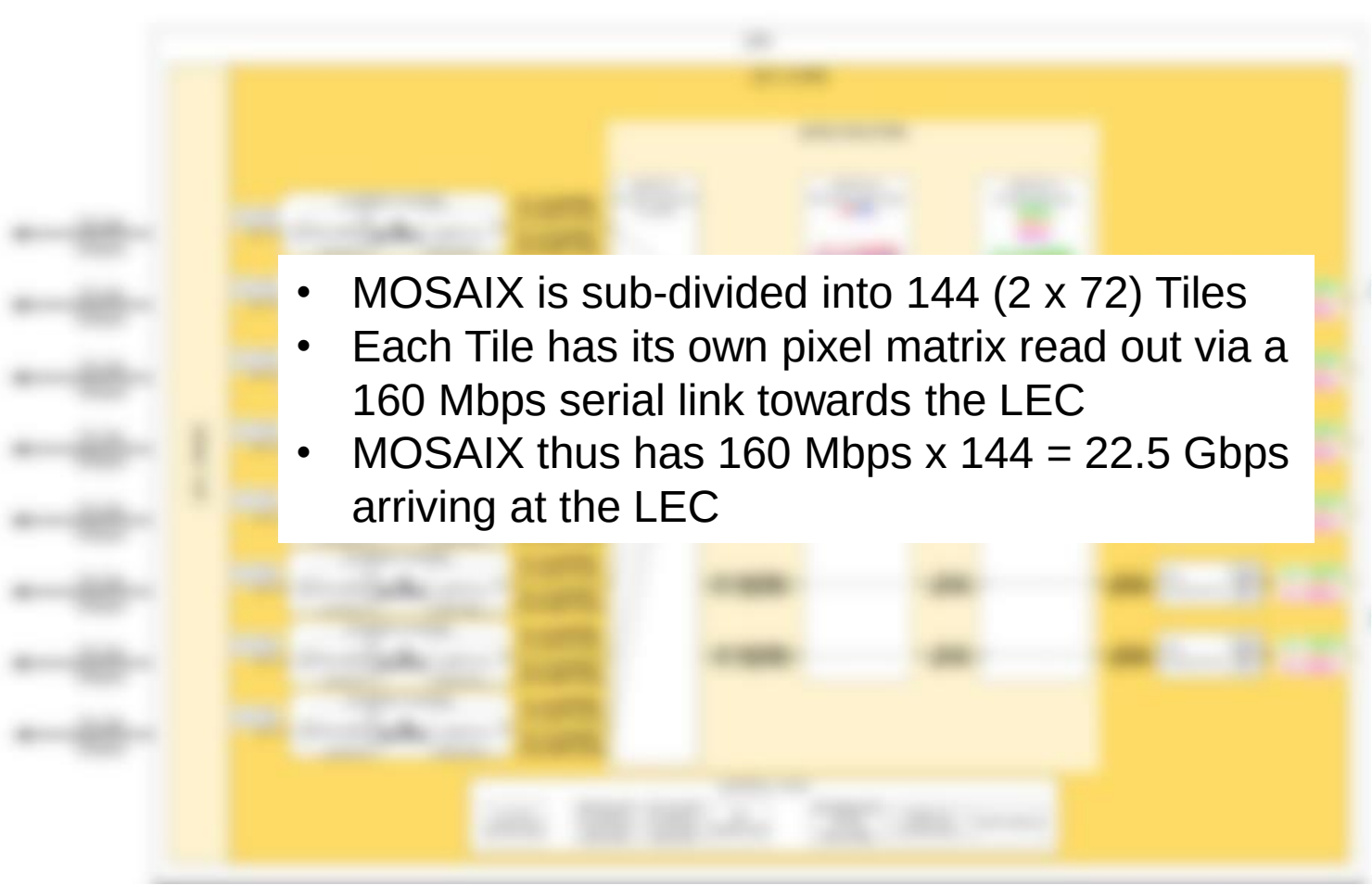
Inner Barrel: MOSAIX Readout

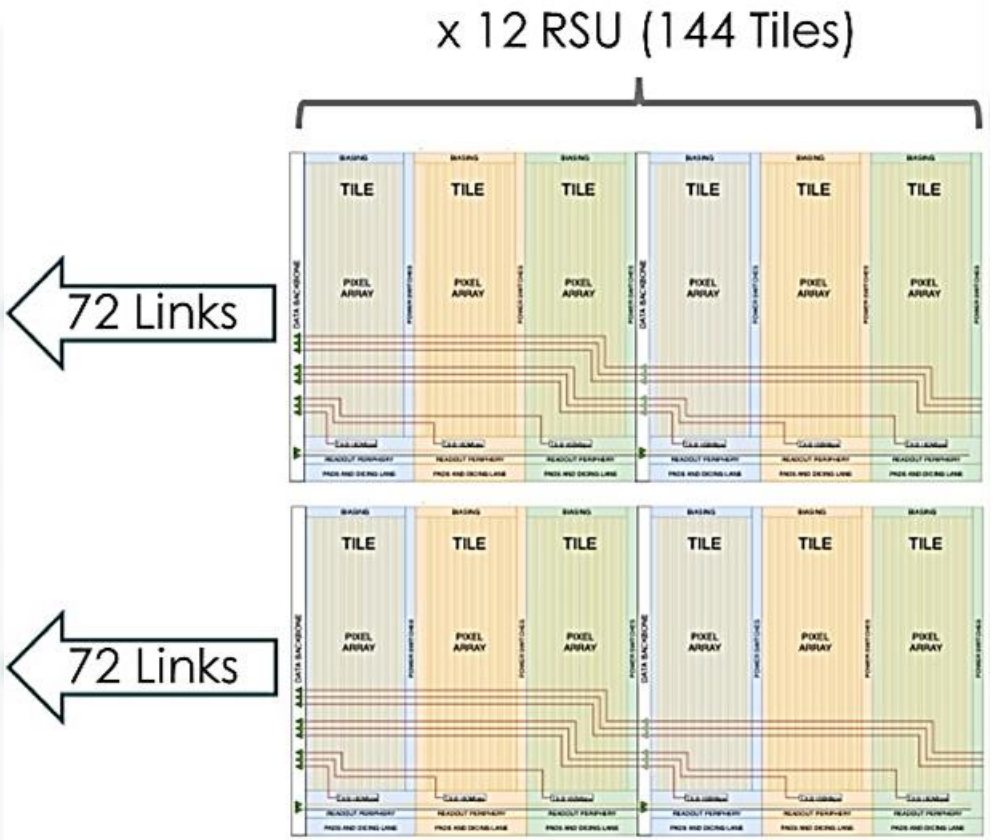
MOSAIX Data Flow – From Tiles to Left Endcap



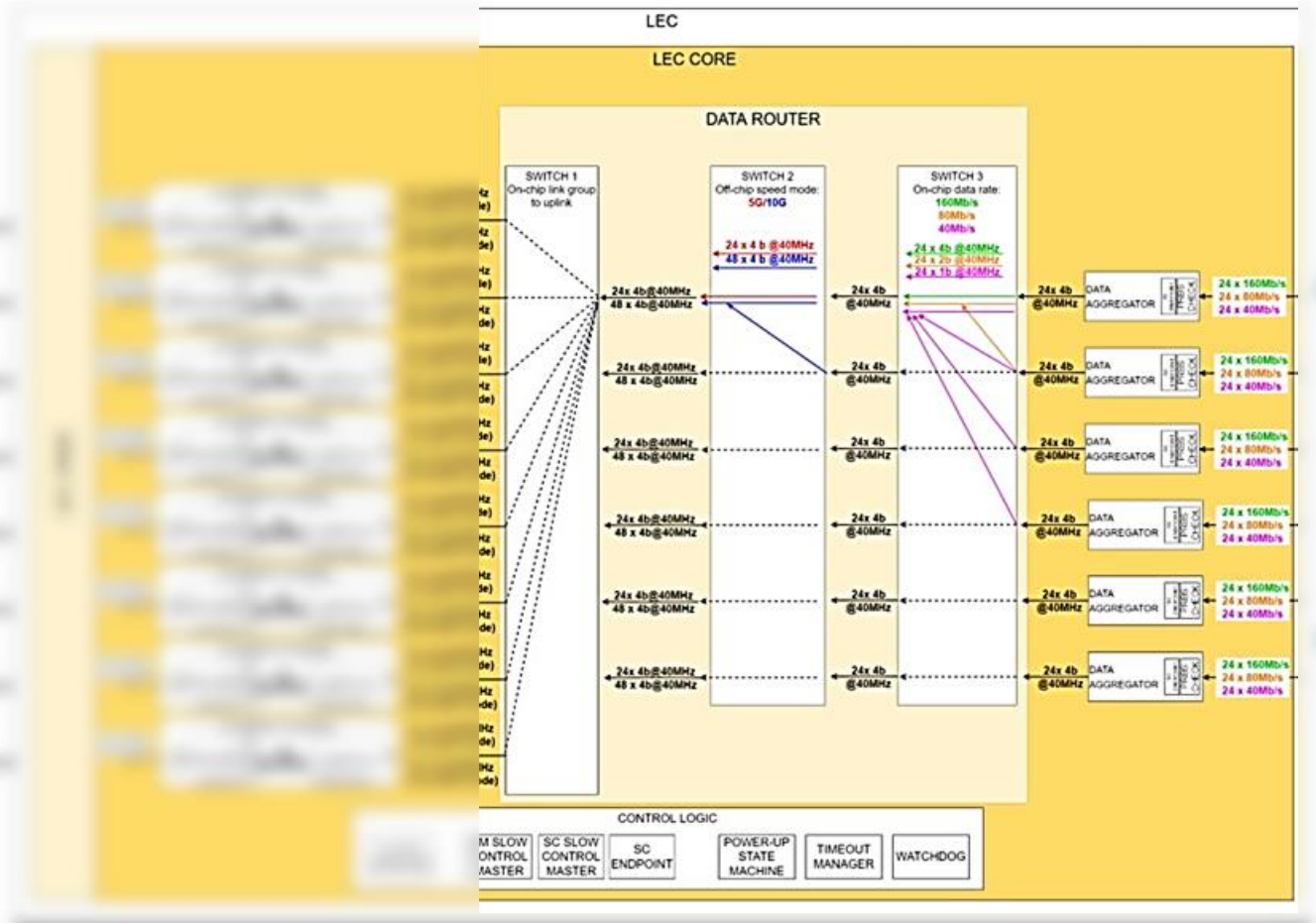
MOSAIX Data Flow – From Tiles to Left Endcap

- MOSAIX is sub-divided into 144 (2 x 72) Tiles
- Each Tile has its own pixel matrix read out via a 160 Mbps serial link towards the LEC
- MOSAIX thus has 160 Mbps x 144 = 22.5 Gbps arriving at the LEC



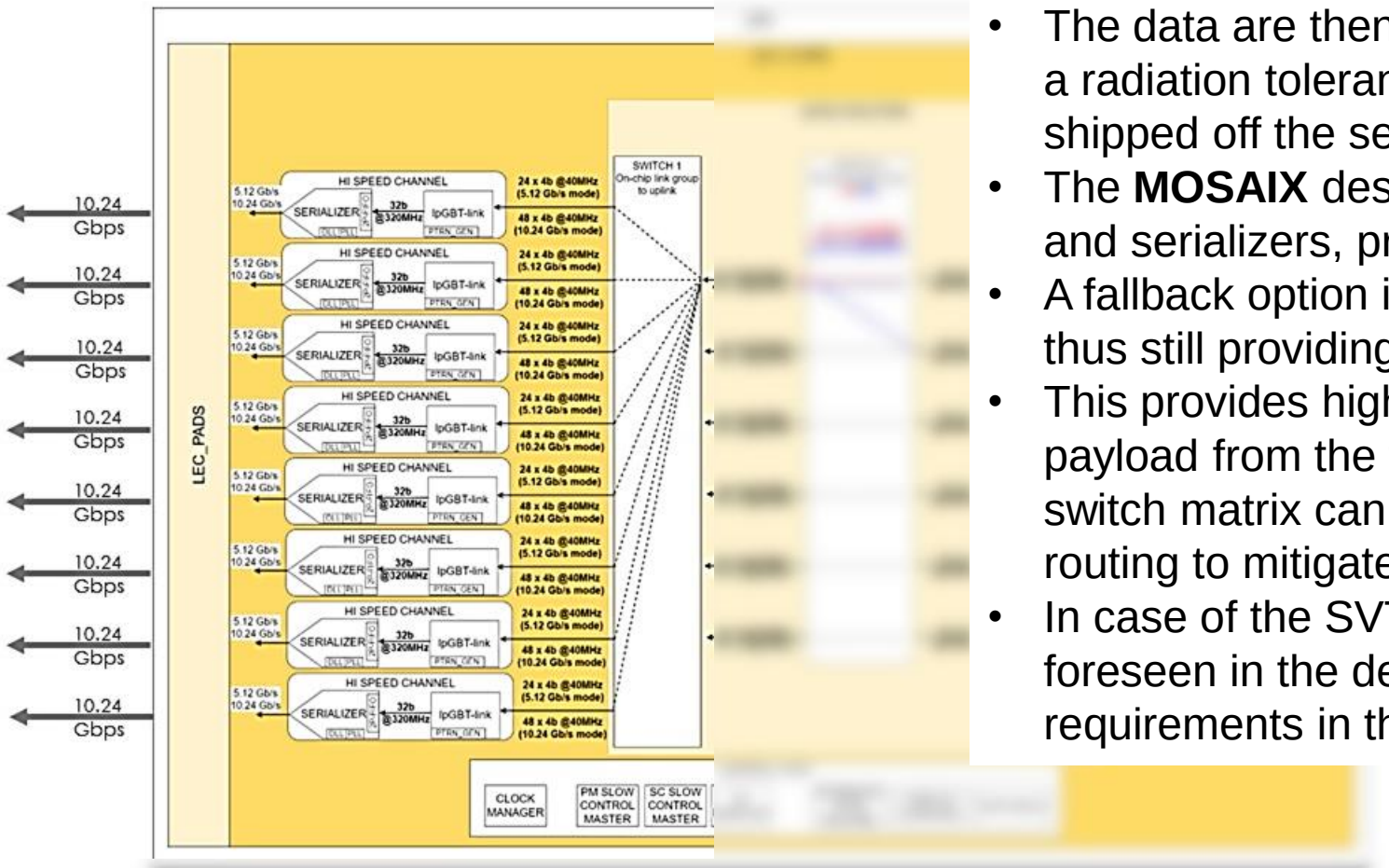


MOSAIX Data Flow – From Tiles to Left Endcap



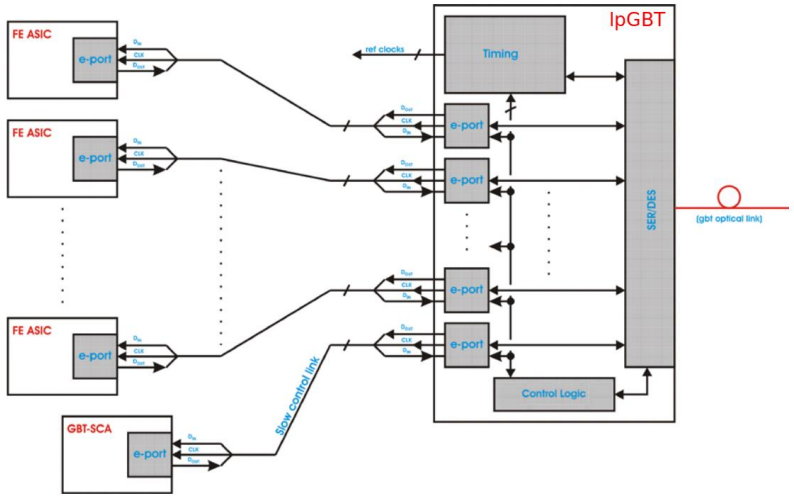
- In the LEC, the tile serial links are received and aligned
- Via a switch matrix, the data can then selectively be sent to individual encoders and off-chip serializers

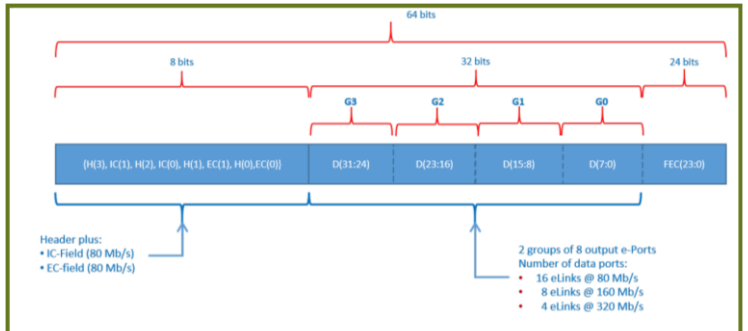
MOSAIX Data Flow – From Tiles to Left Endcap



- The data are then encoded with **lpGBT** IPs (providing a radiation tolerant protocol) and serialized to be shipped off the sensor via **10.24 Gbps** links.
- The **MOSAIX** design contains a total of **8 encoders** and serializers, providing a total **80 Gbps** bandwidth.
- A fallback option is to run the serializers at **5.12 Gbps**, thus still providing **40 Gbps**.
- This provides high redundancy for the **22.5 Gbps** payload from the tiles in case of radiation damage; the switch matrix can be programmed with different (fixed) routing to mitigate the impact of failed components.
- In case of the SVT **LAS**, only **one serializer** is foreseen in the design due to the much lower payload requirements in these sensors.

lpGBT Protocol





Downlink

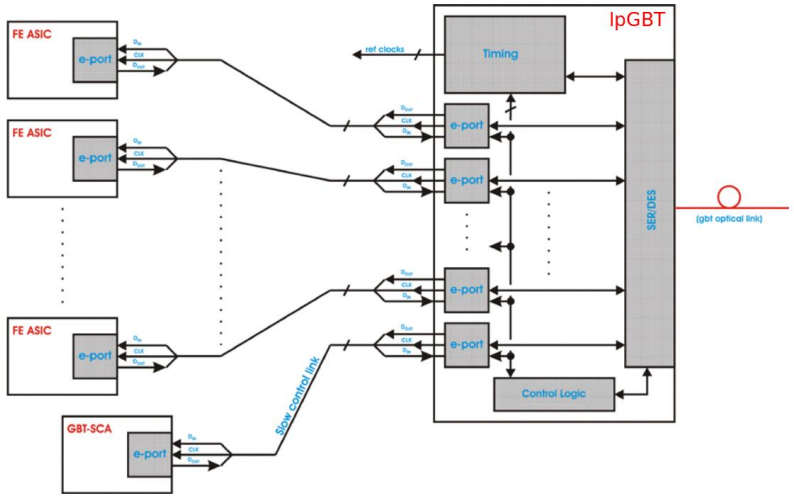
Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

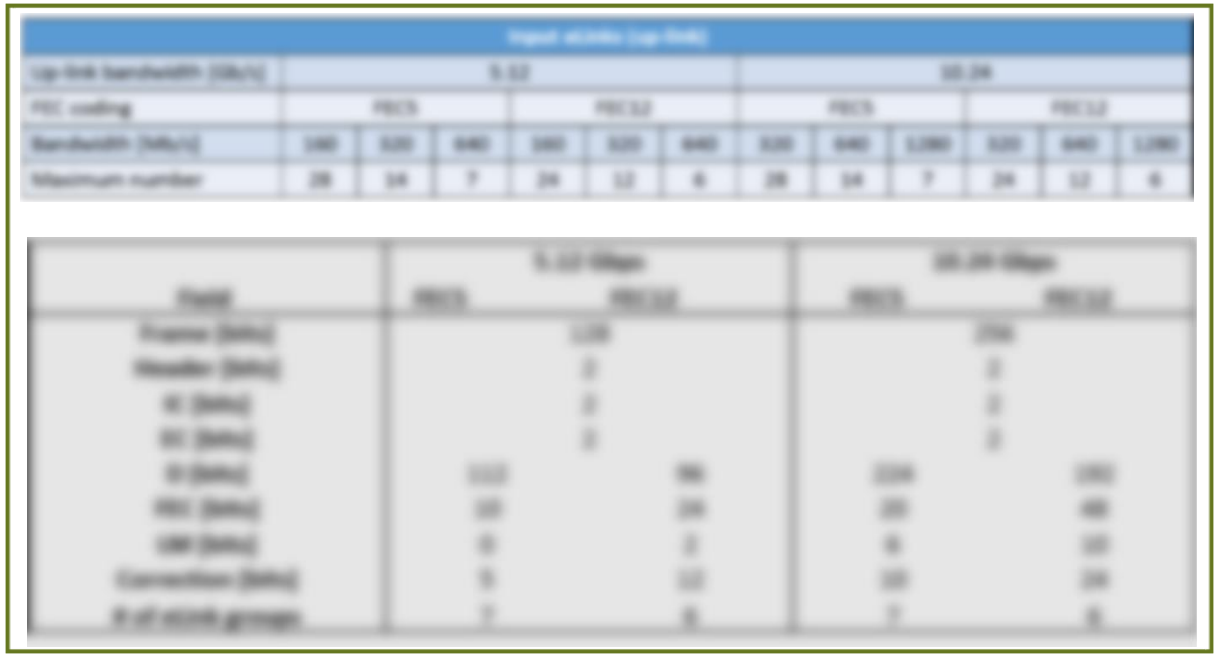
Data Uplink

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Field	5.12 Gbps		10.24 Gbps	
	FEC5	FEC12	FEC5	FEC12
Frame [bits]	128		256	
Header [bits]	2		2	
IC [bits]	2		2	
EC [bits]	2		2	
D [bits]	112	96	224	192
FEC [bits]	10	24	20	48
LM [bits]	0	2	6	10
Correction [bits]	5	12	10	24
# of eLink groups	7	6	7	6

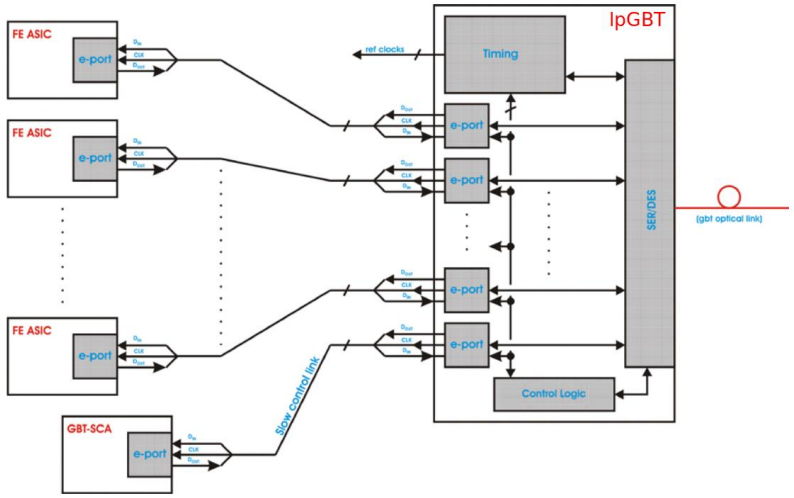
lpGBT Protocol



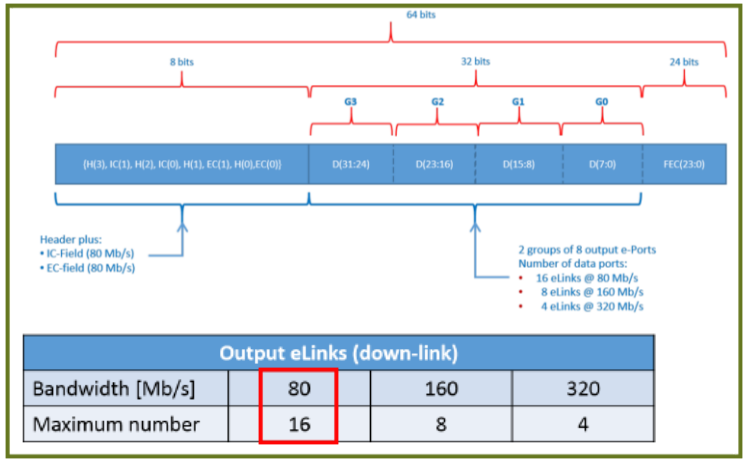


- Front Ends connect to “e-links”
- The fiber protocol includes “Forward Error Correction”

lpGBT Protocol



- Front Ends connect to “e-links”
- The fiber protocol includes “Forward Error Correction”
- Downlink runs at 2.56 Gbps
  - Downlink frame is 64bit wide, of which 32 bits are payload
  - 1.28 Gbps payload
  - Up to 16 e-links @ 80 Mbps

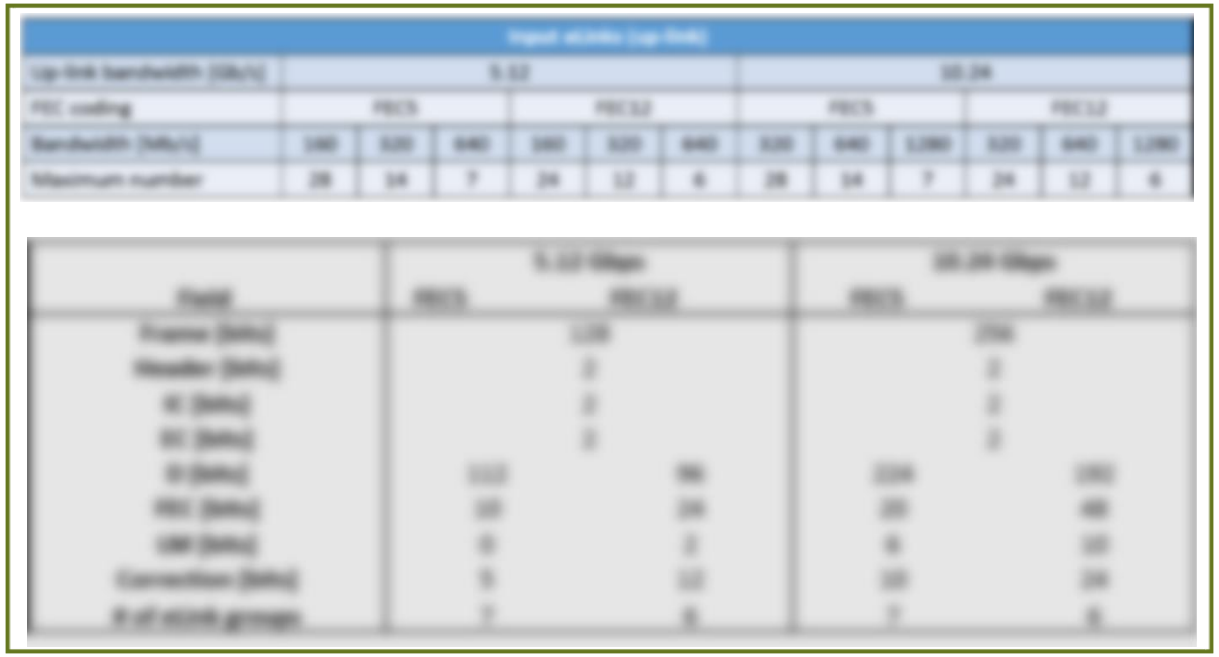


Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

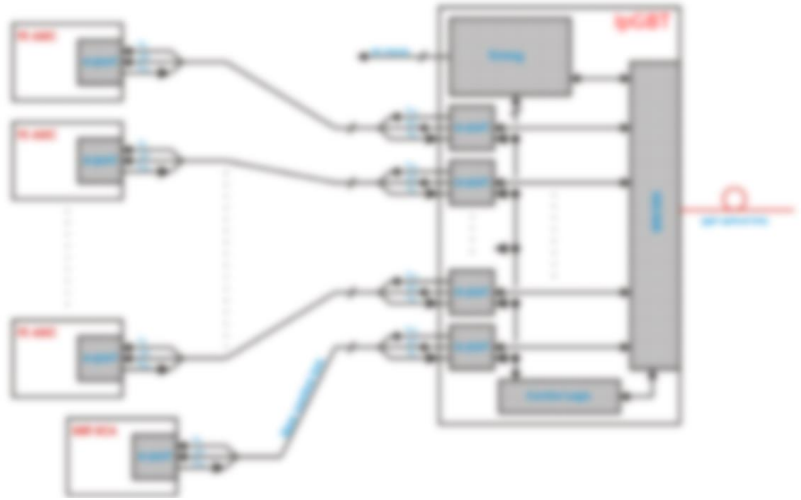
Downlink

Line Rate: **2.56 Gbps**
32 out of 64 bits are data:
Payload = **1.280 Gbps**

Data Uplink



lpGBT Protocol



Downlink

Line Rate: **2.56 Gbps**
32 out of 64 bits are data:
Payload = **1.280 Gbps**

Data Uplink

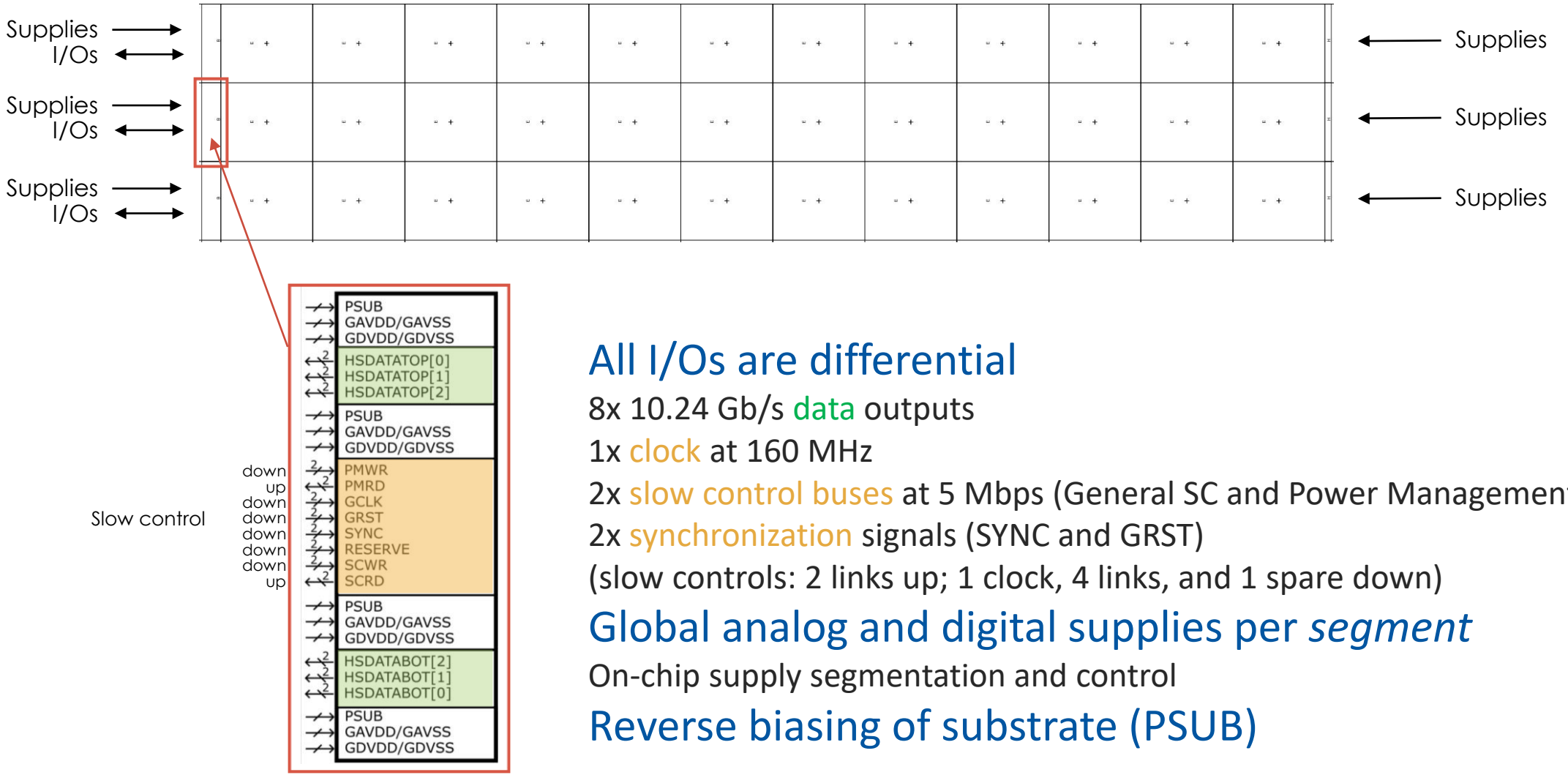
192 out of 256 bits are data:
Payload = **7.680 Gbps**

- Front Ends connect to “e-links”
- The fiber protocol includes “Forward Error Correction”
- Downlink runs at 2.56 Gbps
  - Downlink frame is 64bit wide, of which 32 bits are payload
  - 1.28 Gbps payload
  - Up to 16 e-links @ 80 Mbps
- Uplink runs at either 10.24 Gbps or 5.12 Gbps
  - Uplink frame is either 128bit or 256bit
  - 256bit frame contains 192bits of payload (7.68 Gbps)
  - Up to 24 e-links at either 160 Mbps or 320 Gbps

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Field	5.12 Gbps FEC5	5.12 Gbps FEC12	10.24 Gbps FEC5	10.24 Gbps FEC12
Frame [bits]	128		256	
Header [bits]	2		2	
IC [bits]	2		2	
EC [bits]	2		2	
D [bits]	112	96	224	192
FEC [bits]	10	24	20	48
LM [bits]	0	2	6	10
Correction [bits]	5	12	10	24
# of eLink groups	7	6	7	6

MOSAIX Interfaces in the Left End Cap (LEC)



All I/Os are differential

8x 10.24 Gb/s data outputs

1x clock at 160 MHz

2x slow control buses at 5 Mbps (General SC and Power Management)

2x synchronization signals (SYNC and GRST)

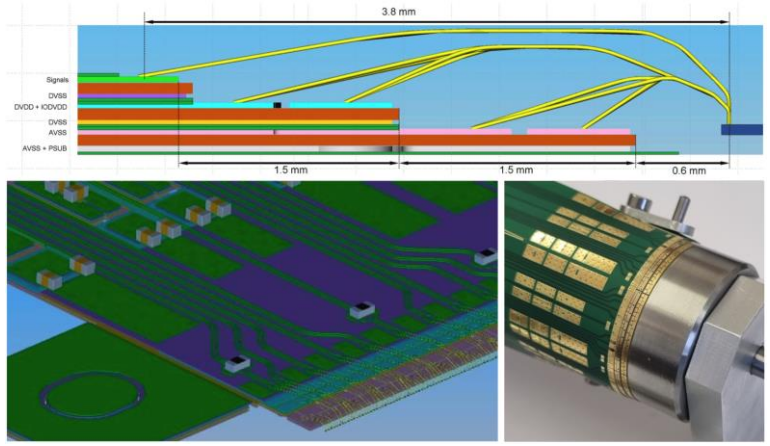
(slow controls: 2 links up; 1 clock, 4 links, and 1 spare down)

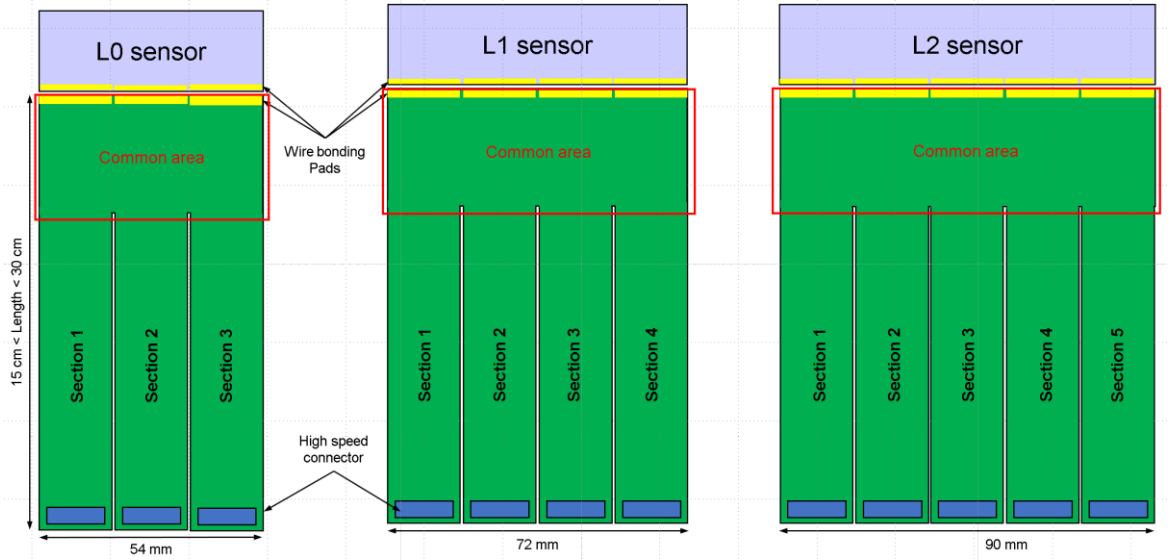
Global analog and digital supplies per *segment*

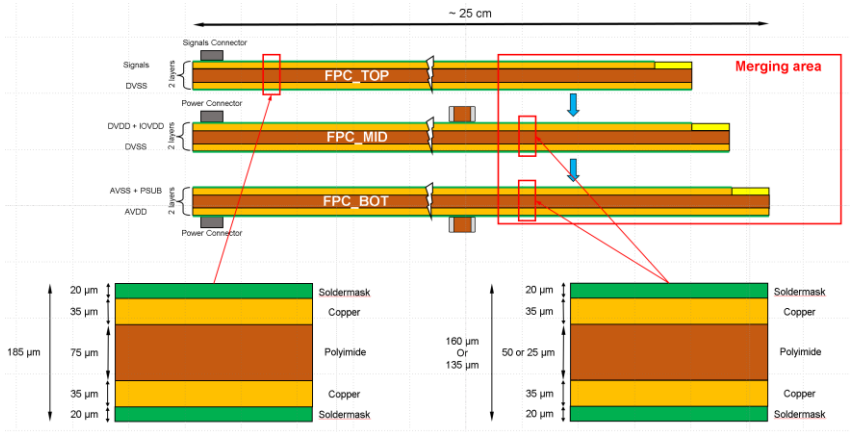
On-chip supply segmentation and control

Reverse biasing of substrate (PSUB)

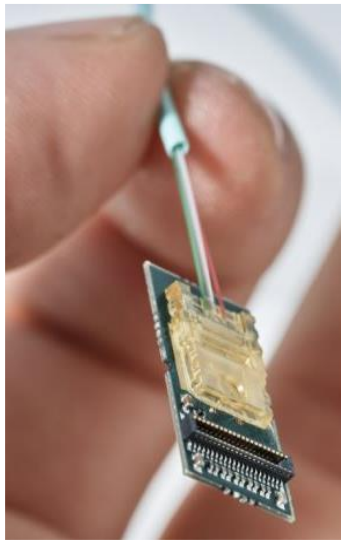
ITS3 Flex PC Design: Inspiration for SVT IB FPC design





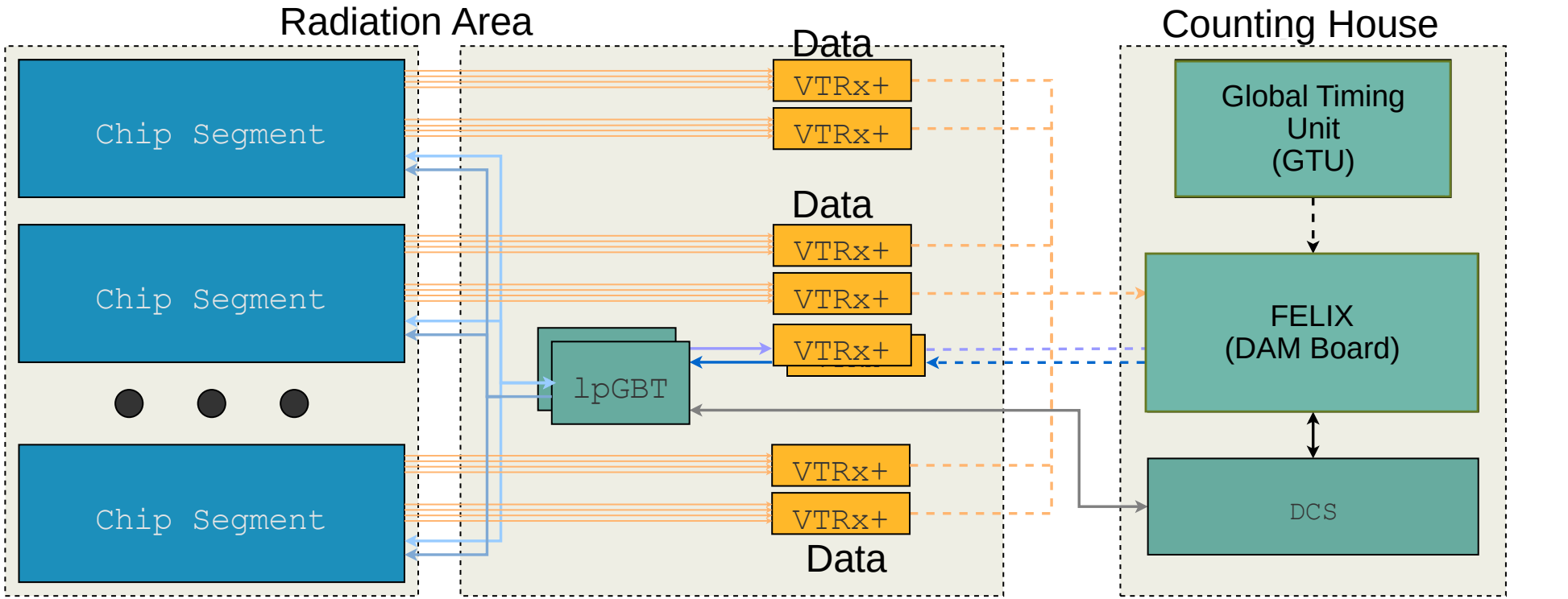


Inner Barrel Readout Electronics (inspired by ITS-3 DSE)



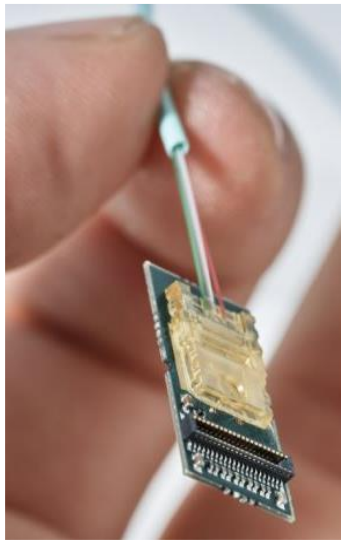
VTRx+

lpGBT



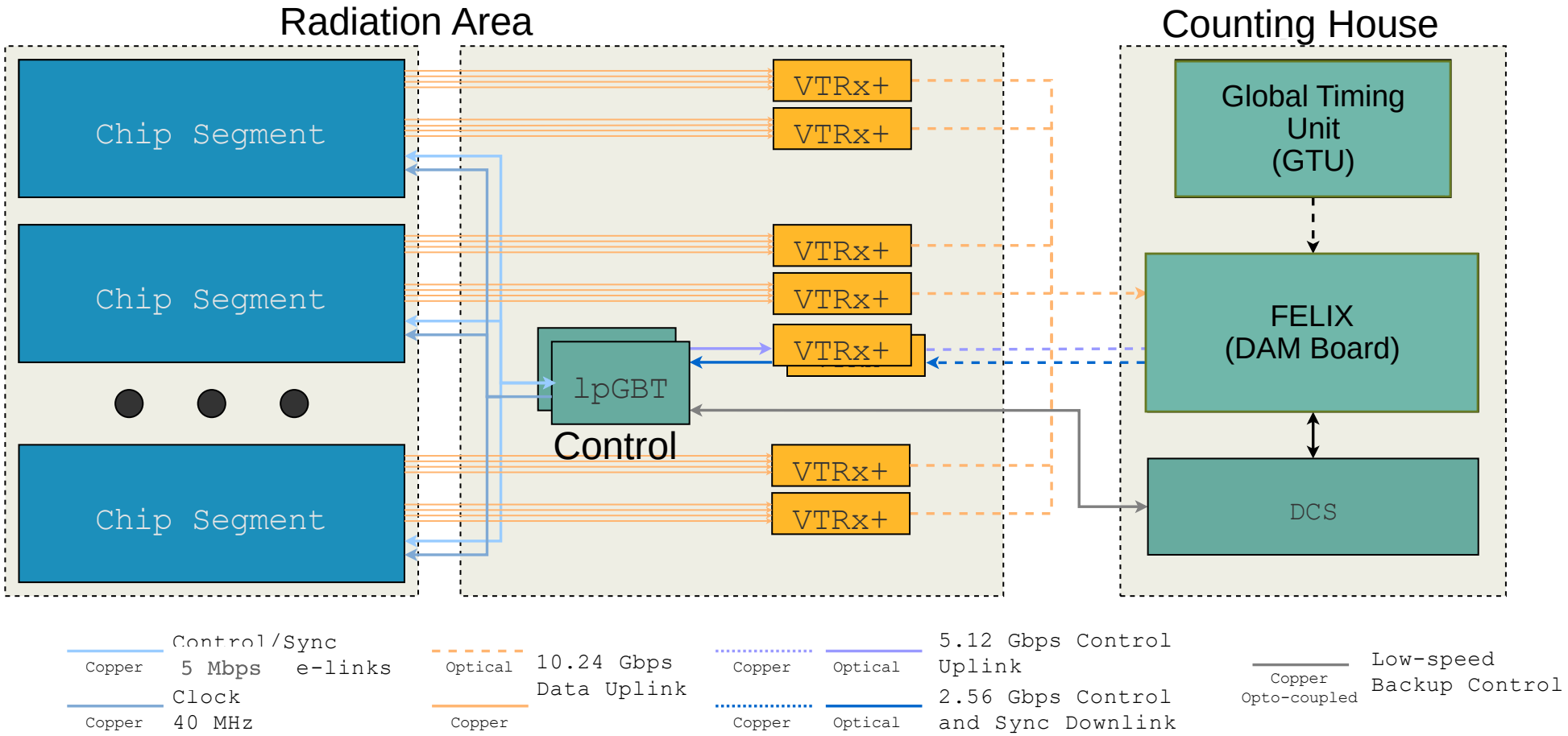
Data : 4 HS lines connected to 1 VTRx+ -> Fiber bundle

Inner Barrel Readout Electronics (inspired by ITS-3 DSE)



VTRx+

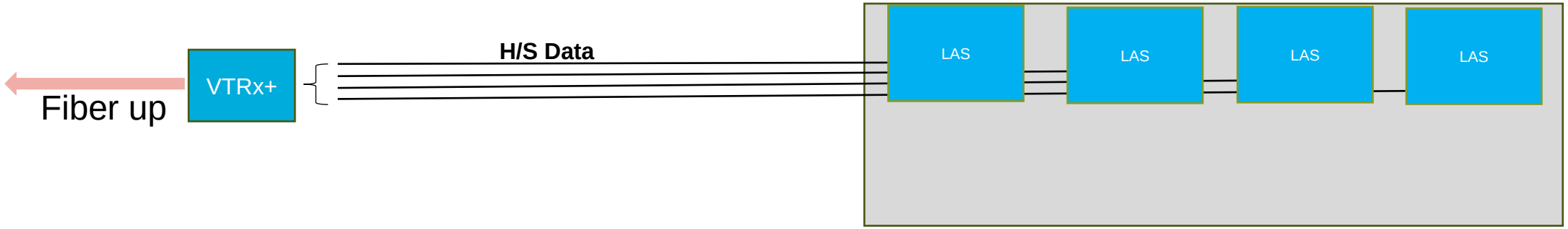
lpGBT



Data : 4 HS lines connected to 1 VTRx+ -> Fiber bundle
Slow Controls: uses lpGBT e-links for one-to-one connection with the LEC SC signals
lpGBTs are also used to control and monitor RDO electronics itself
lpGBTs are connected to individual VTRx+ for fiber up and downlink

Outer Barrel & Disk LAS Readout

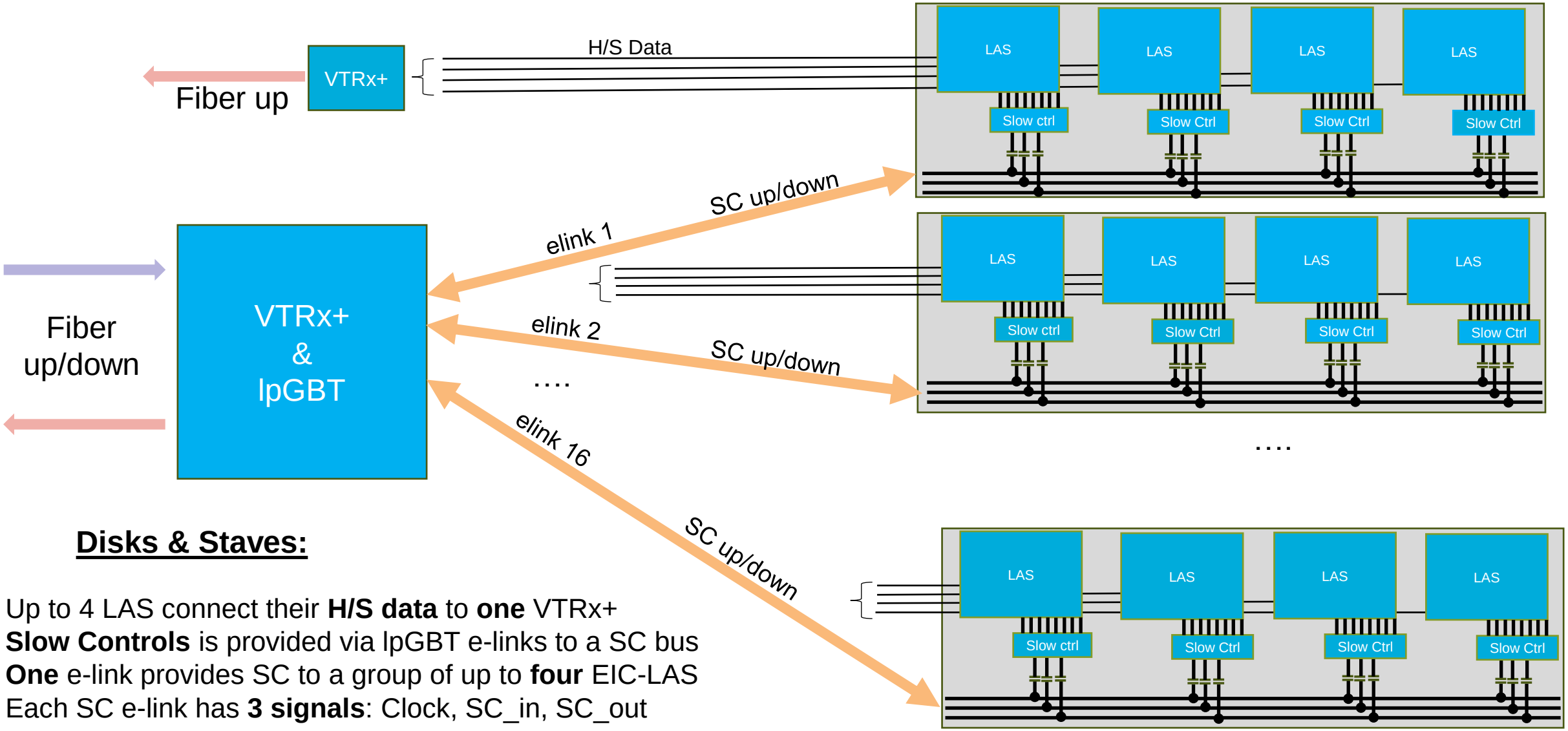
Outer Barrel and Disk Readout Electronics



Disks & Staves:

Up to 4 LAS connect their **H/S data** to **one** VTRx+

Outer Barrel and Disk Readout Electronics

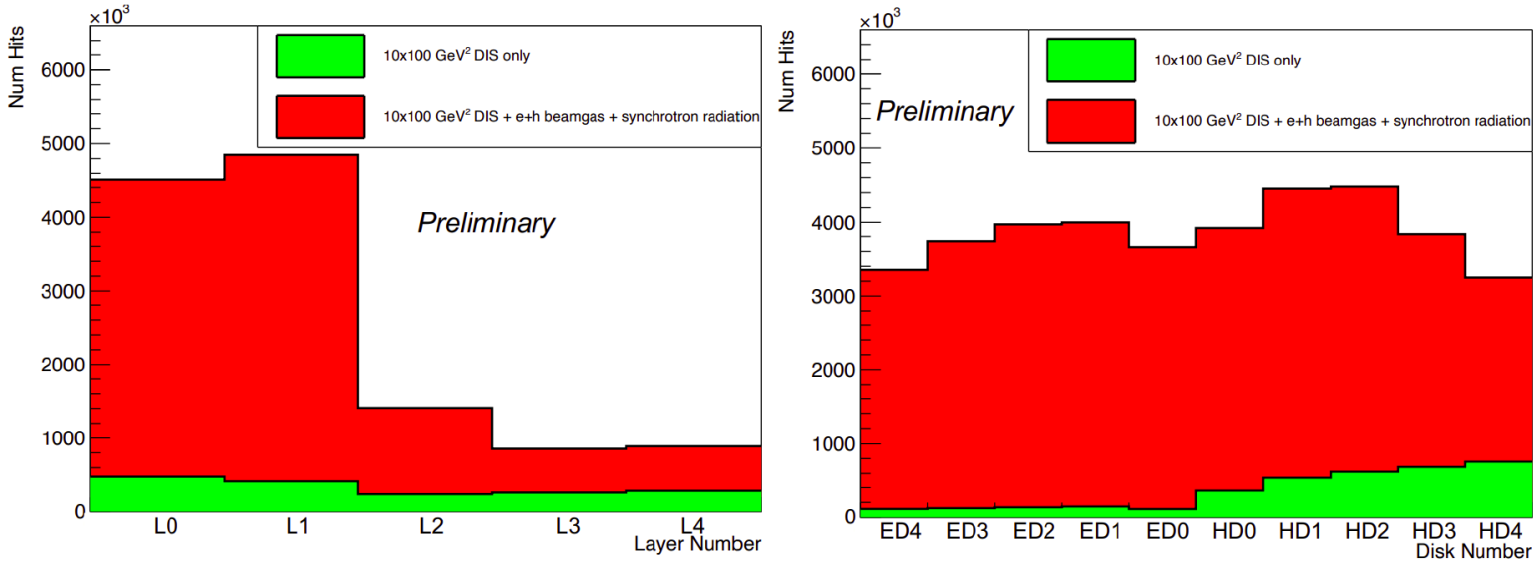


Disks & Staves:

Up to 4 LAS connect their **H/S data** to **one** VTRx+
Slow Controls is provided via lpGBT e-links to a SC bus
One e-link provides SC to a group of up to **four** EIC-LAS
Each SC e-link has **3 signals**: Clock, SC_in, SC_out

SVT Readout Numbers

SVT Hit Rate Simulations



- **10x100 GeV ep**, 4.48 x 10^{33} $cm^{-2}s^{-1}$, 184 kHz DIS event rate
- 10 GeV SR
- 10 GeV e-beam gas, 10000 Ahr
- 100 GeV proton-beam gas, 100 Ahr

	Hit Rate (Hz)	Area (cm²)	Hits/s/cm²
L0	4.50E+06	610.73	7.37E+03
L1	4.85E+06	814.30	5.96E+03
L2	1.41E+06	2035.75	6.93E+02
L3	8.55E+05	9160.88	9.33E+01
L4	8.89E+05	22167.08	4.01E+01

	Hit Rate (Hz)	Area (cm²)	Hits/s/cm²
ED0	3.66E+05	1767.11	2.07E+02
ED1	4.00E+06	5368.16	7.45E+02
ED2	3.97E+06	5536.32	7.17E+02
ED3	3.74E+06	5532.26	6.76E+02
ED4	3.35E+06	5524.62	6.06E+02

	Hit Rate (Hz)	Area (cm²)	Hits/s/cm²
HD0	3.92E+06	1767.11	2.22E+03
HD1	4.45E+06	5368.16	8.29E+02
HD2	4.48E+06	5533.75	8.10E+02
HD3	3.83E+06	5513.51	6.95E+02
HD4	3.25E+06	5486.76	5.92E+02

SVT by the numbers

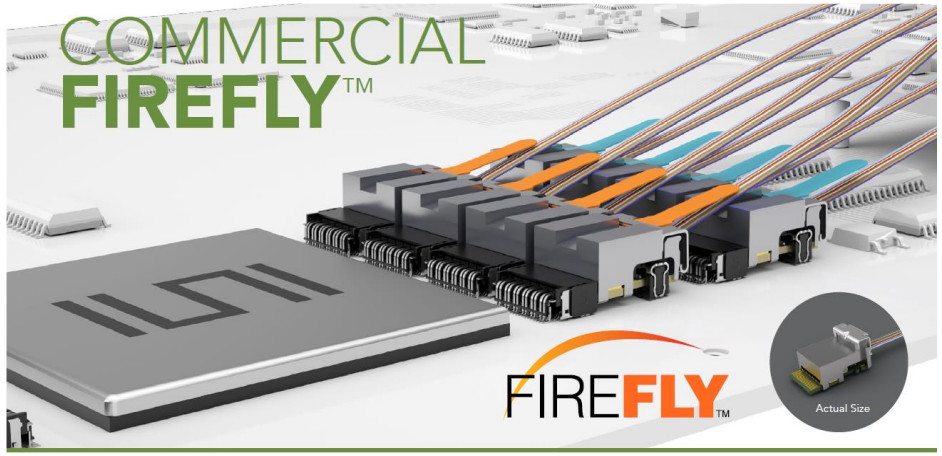
	width (mm)	length (mm)		# pixels per RSU													
Reticle size	19.564	21.666		827,424													
Pixel size	0.0208	0.0228															
Barrel					Sensor											10x275GeV	
Layer Index	radius (mm)	z (mm)		Area (mm^2)	reticles in width	reticles in length	# of sensors in r-phi	# of sensors in z	# pixels	# sensors	Notes	# Readout Links	# Staves	# Data VTRx+	# SC lpGBTs	Hit Rate / s	Hits/pixel/ 2us frame
L0	36	260		58,811	3	12	4	1	119,149,056	4	bent ITS3	96		24	5	2.73E+07	4.26E-07
L1	48	260		78,414	4	12	4	1	158,865,408	4	bent ITS3	128		32	7	2.94E+07	3.44E-07
L2	120	260		196,035	5	12	8	1	397,163,520	8	bent ITS3	320		80	17	8.55E+06	4.01E-08
L3	270	520		882,158	1	6	96	4	1,906,384,896	384	6 -RSU LAS	384	48	96	8	5.19E+06	5.06E-09
L4	420	840		2,216,706	1	5	148	8	4,898,350,080	1184	5-RSU LAS	1184	74	296	25	5.39E+06	2.05E-09
e-endcap																	
Disk index	z (mm)	inner r (mm)	outer r (mm)			5-RSU LAS	6-RSU LAS						Readout Groups				
ED0	-250	36.76	240	176,710		56	40		337,588,992	96	5-RSU LAS	96	26	26	3	2.22E+06	1.22E-08
ED1	-450	36.76	415	536,815		334	0		1,381,798,080	334	5-RSU LAS	334	96	96	8	2.43E+07	3.27E-08
ED2	-650	36.76	421.4	553,632		334	0		1,381,798,080	334	5-RSU LAS	334	96	96	8	2.41E+07	3.24E-08
ED3	-850	40.0614	421.4	552,835		334	0		1,381,798,080	334	5-RSU LAS	334	96	96	8	2.27E+07	3.05E-08
ED4	-1050	46.3529	421.4	551,127		334	0		1,381,798,080	334	5-RSU LAS	334	96	96	8	2.03E+07	2.74E-08
h-endcap																	
Disk index																	
HD0	250	36.76	240	176,710		56	40		337,588,992	96	5-RSU LAS	96	26	26	3	2.38E+07	1.31E-07
HD1	450	36.76	415	536,815		334	0		1,381,798,080	334	5-RSU LAS	334	96	96	8	2.70E+07	3.63E-08
HD2	700	38.52	421.4	553,216		334	0		1,381,798,080	334	5-RSU LAS	334	96	96	8	2.72E+07	3.66E-08
HD3	1000	53.43	421.4	548,909		334	0		1,381,798,080	334	5-RSU LAS	334	96	96	8	2.32E+07	3.13E-08
HD4	1350	70.14	421.4	542,422		334	0		1,381,798,080	334	5-RSU LAS	334	96	96	8	1.97E+07	2.65E-08
TOTAL				8,161,315					19,209,475,584	4448		4976		1348	132	2.90E+08	hits/s
																34.61	Gbps
									# of segments:	4500							
									# of SC links down	22500						… plus noise	
									# of SC links up	9000							

SVT Readout Prototype Developments

SVT Prototype Developments

- A full setup with lpGBT, VTRx+, and FPGA development boards (stand-ins for FELIX) exists at ORNL for evaluation of the various RDO components.
- Alternatives to CERN's lpGBT universe of components using commercial alternatives are being investigated.
- First results with these setups have been achieved in the context of an R&D project concerned with the Silicon using EIC project funds.
  - Evaluation of the Samtec Optical FireFly as an alternative to VTRx+
  - Evaluation of the Microchip PolarFire FPGA as a radiation-tolerant FPGA replacement of the lpGBT
- Evaluation of Aggregator Board architectures with commercial FPGA development boards has been started at MIT in the context of the Silicon R&D project.
- A test setup for the characterization of CERN Engineering Run chiplets to be used in the MOSAIX and LAS designs is under development.
- Investigations on Redundancy issues on the LAS design interfaces has started.
- Work is ongoing on defining the details of the LAS physical and protocol interfaces.

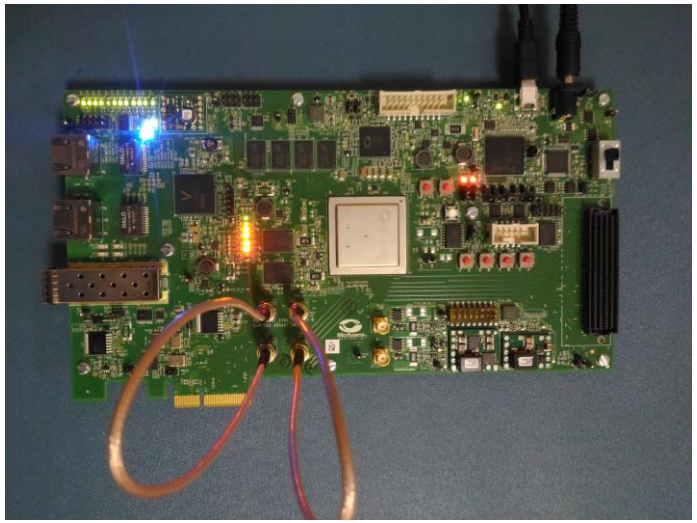
Commercial Alternatives: FireFly & PolarFire

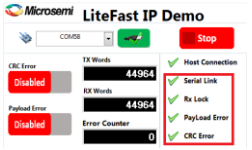


MICROCHIP
PolarFire®
FPGA

		MPF050	MPF100	MPF200	MPF300	MPF500
FPGA Fabric	Logic Elements (4LUT + DFF)	48K	109K	192K	300K	481K
	Math Blocks (18 × 18 MACC)	150	336	588	924	1480
	LSRAM Blocks (20 Kb)	160	352	616)	952	1520
	uSRAM Blocks (64 × 12)	450	1008	1764	2772	4440
	Total RAM (Mb)	3.6	7.6	13.3	20.6	33
	uPROM (Kb)	216	297	297	459	513
	User DLLs/PLLs	8	8 each	8 each	8 each	8 each
High-Speed I/O	250 Mbps–12.7 Gbps Transceiver Lanes	4	8	16	16	24
	PCIe® Gen 2 Endpoints/Root Ports	2	2	2	2	2
Total I/O	Total User I/O	176	296	364	512	584

eRD104 Test Setups

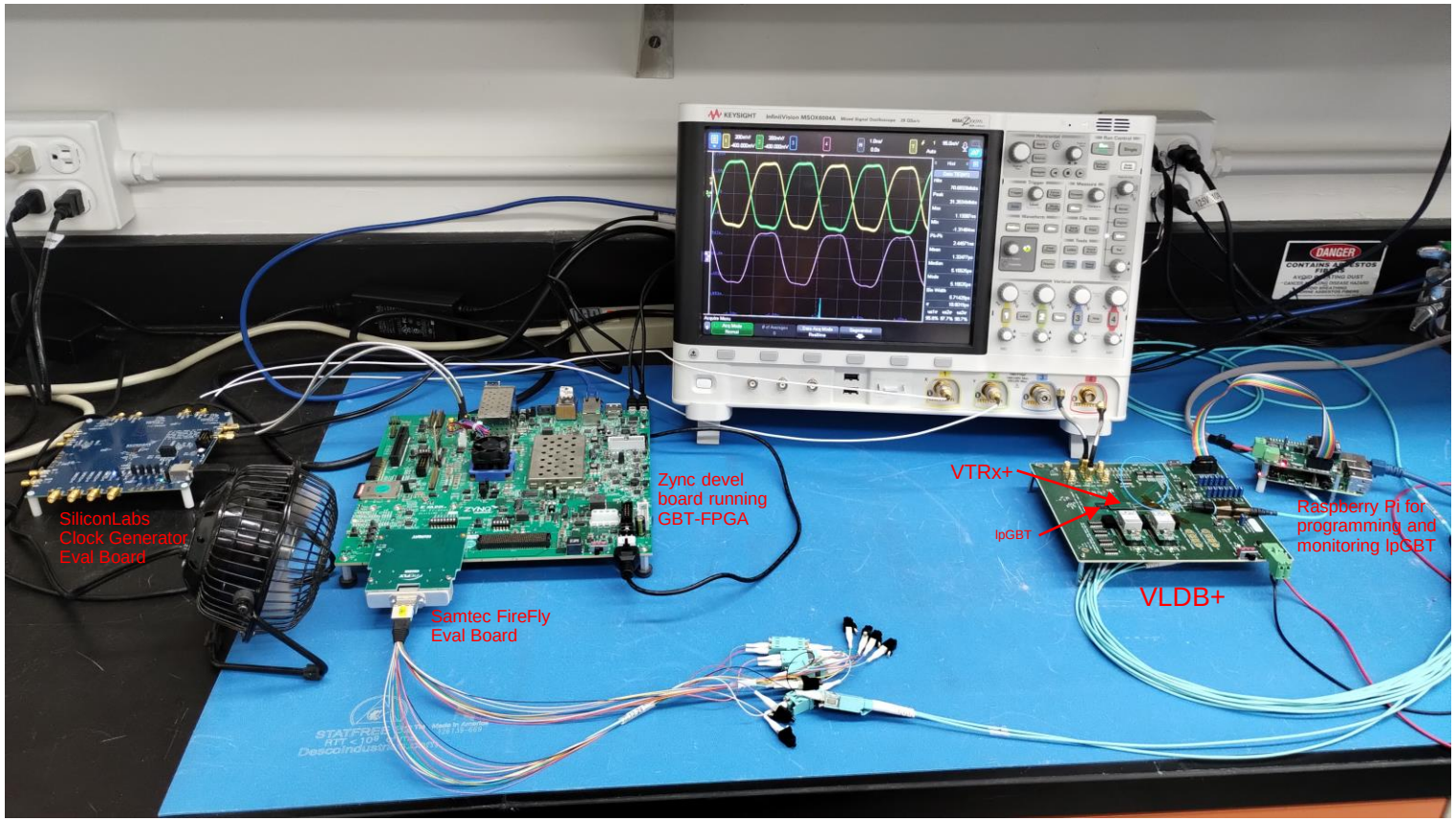




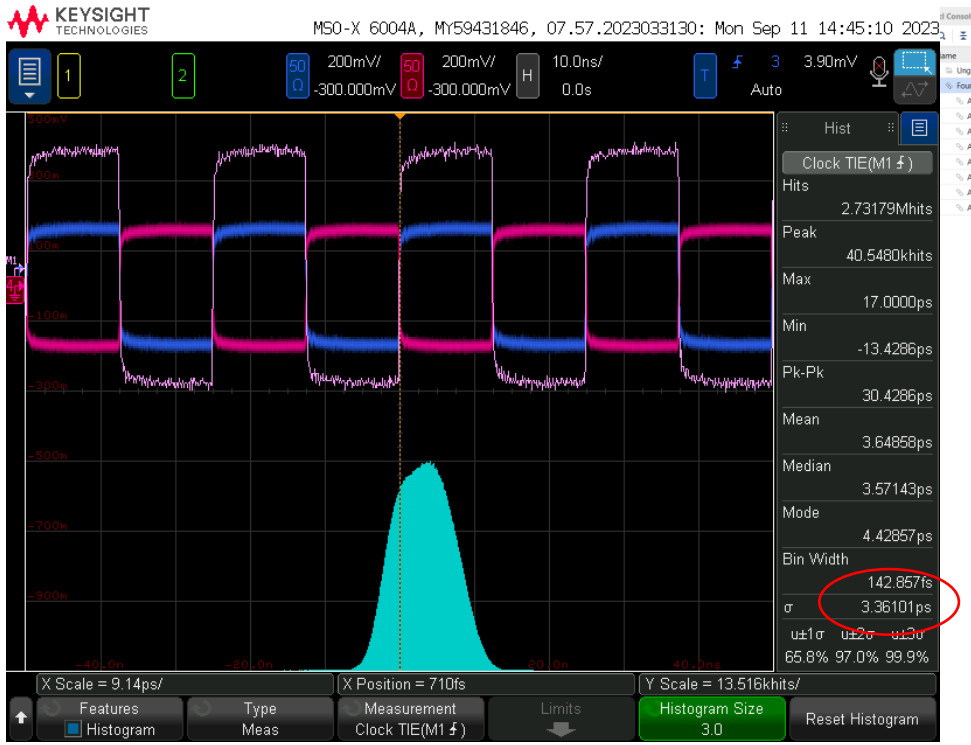
PolarFire Gigabit Transceiver Test Setup

Samtec FireFly Test Setup with Fiber Loopback

lpGBT Test Setup with Samtec FireFly (VTRx+ alternative), Xilinx Ultrascale FPGA evaluation board (“FELIX), and SiliconLabs Clock Generator Board (“GTU”)

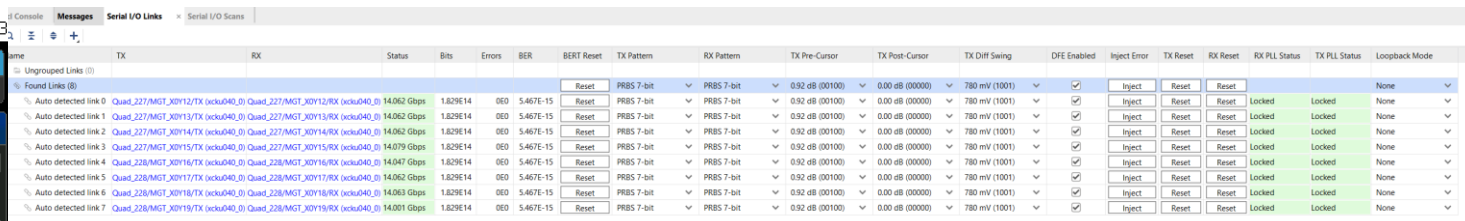


Selected Test Results:

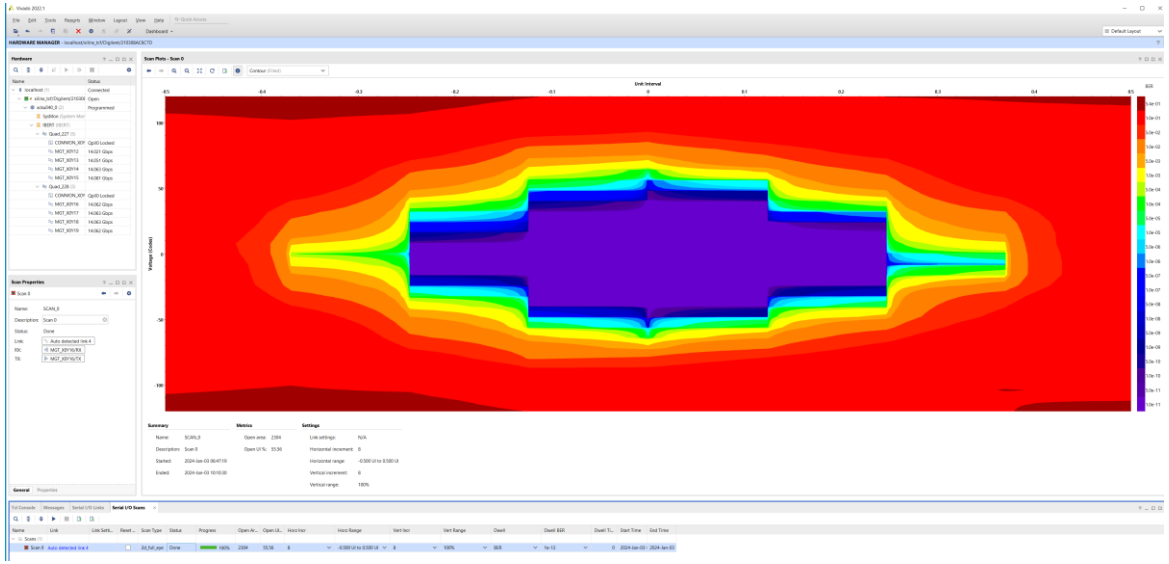


Scope Picture of "Phase Adjustable" recovered clock out of lpGBT

Purple: M1 = CLK+ (red) - Clk- (blue)
TIE Source : M1
Clock TIE measurement sigma = **3.36ps**



Bit Error Rate (BER) Measurements



FireFly "Eye" measurement @ 14 Gbps

Summary

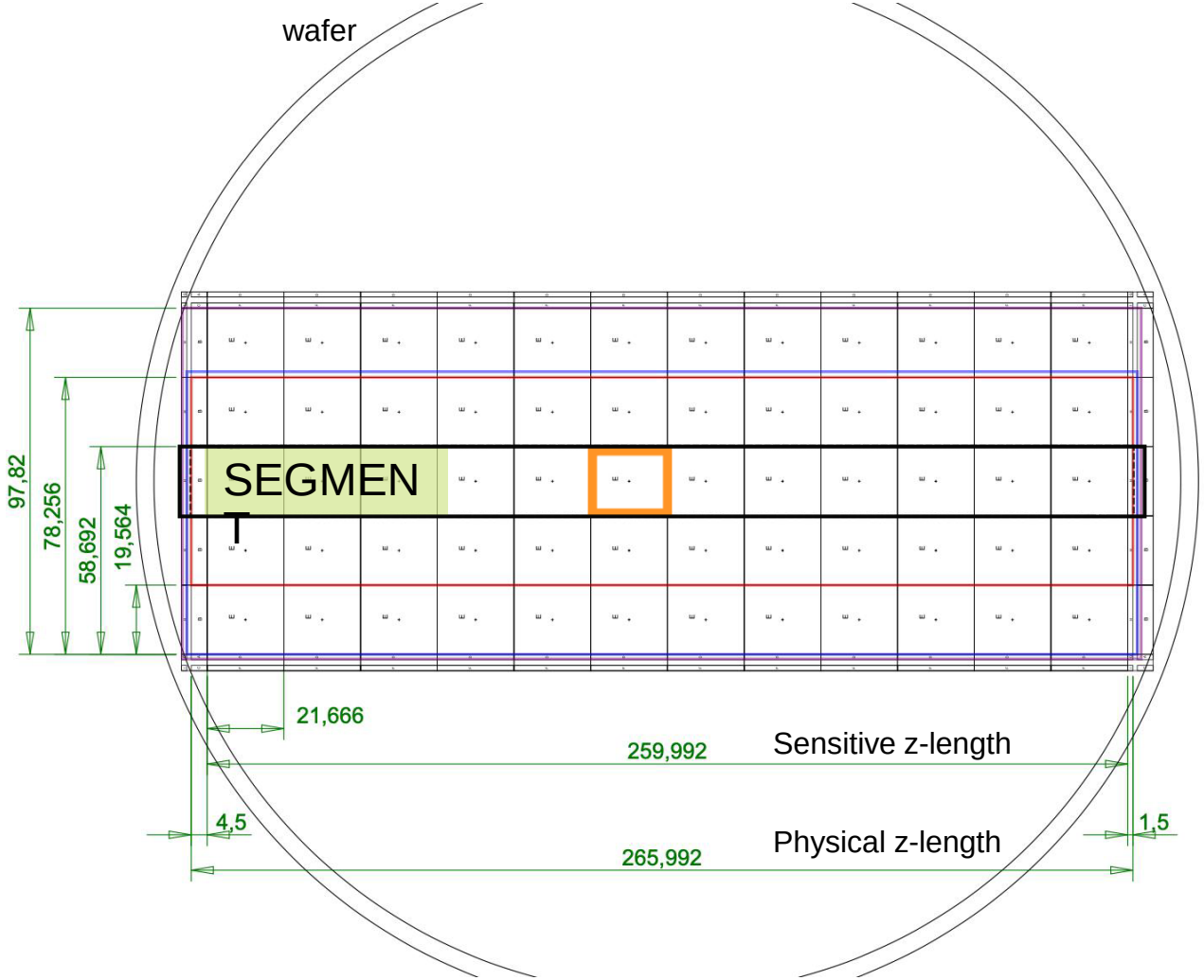
- An SVT Readout Design has been developed and demonstrated here
- Inner Barrel RDO based on ALICE ITS-3 Service Electronics Board Design
  - Direct connection of multiple HS data serializers per segment to VTRx+
  - One-to-One connection between lpGBT e-links and LEC signals for slow controls
  - Direct powering of wafer scale sensor
- Outer Barrel RDO concept uses a concept of LAS Readout groups
  - Group of up to 4 Single HS Data lines are directly connected to VTRx+
  - Slow Controls multiplexed between groups of 4 LAS via AncASICs on each LAS on a single bus
- Prototype Setups are being investigated with evaluation boards of various components
  - First results have already been shown running all components at the full desired speeds and show that sufficient performance is achieved

Backup Slides

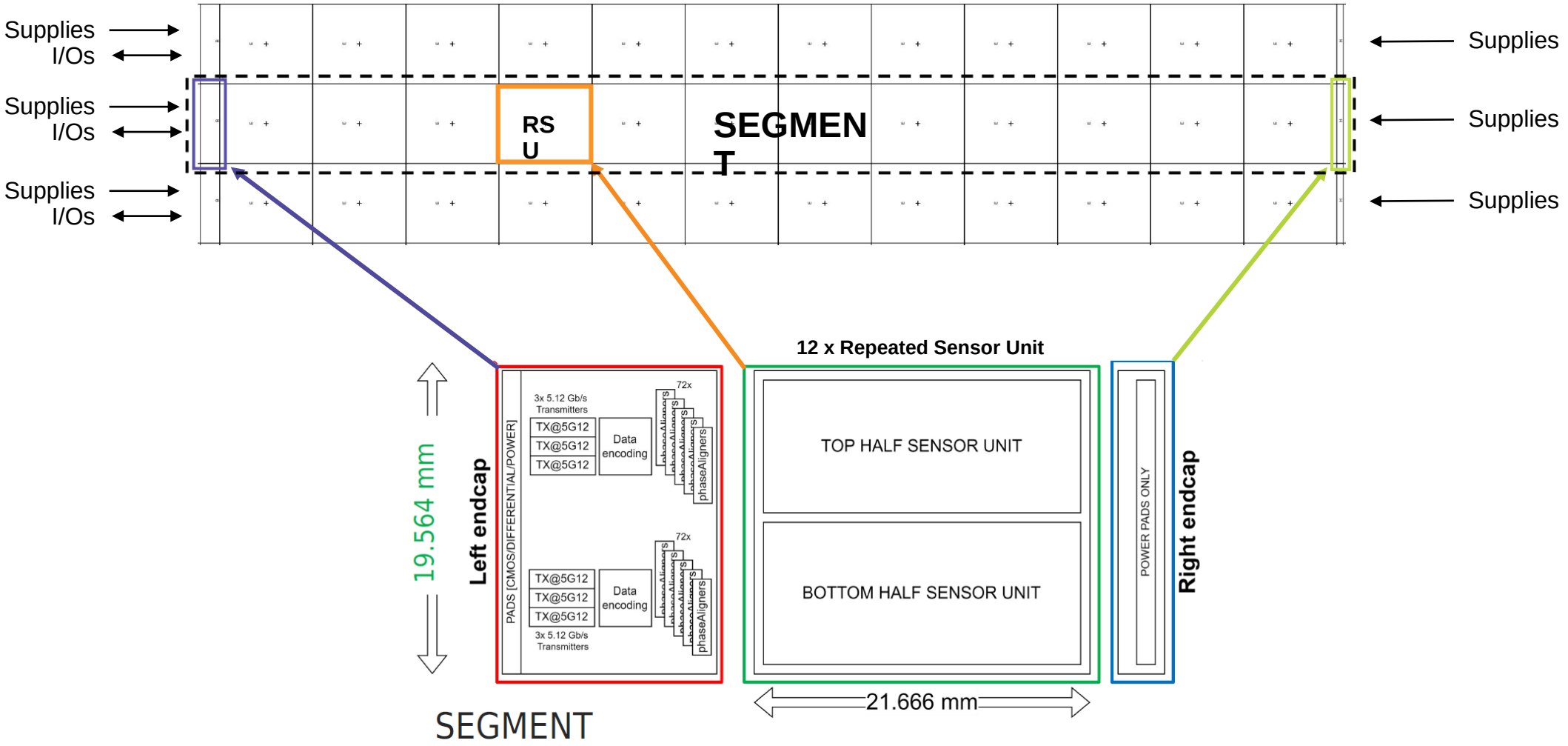
“MOSAIX” Stitched Sensor for SVT Inner Barrel

Layer 0: 12 x 3 repeated units + endcaps
Layer 1: 12 x 4 repeated units + endcaps
Layer 2: 12 x 5 repeated units + endcaps

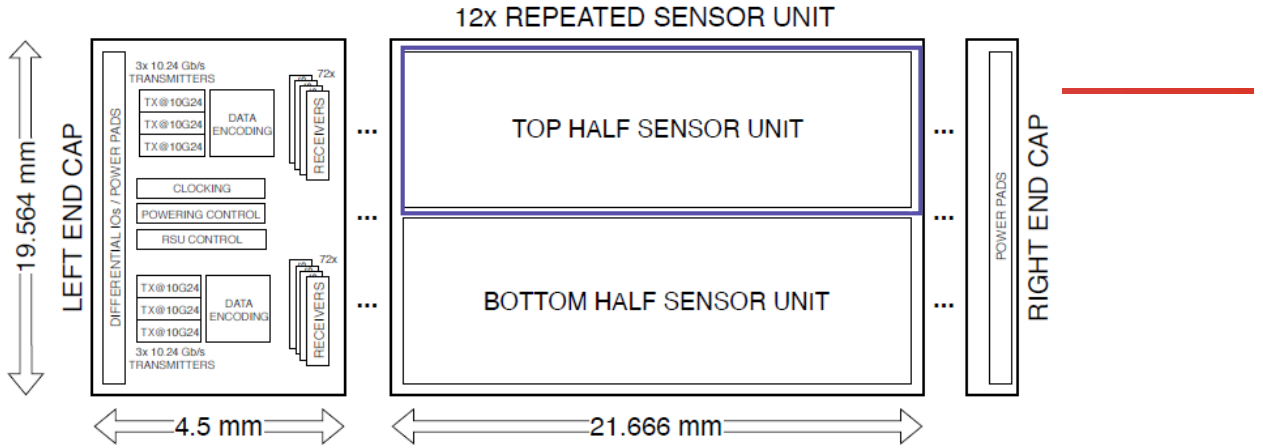
Repeated (Stitched) Sensing Unit (RSU)



MOSAIX Stitched Sensor Detail

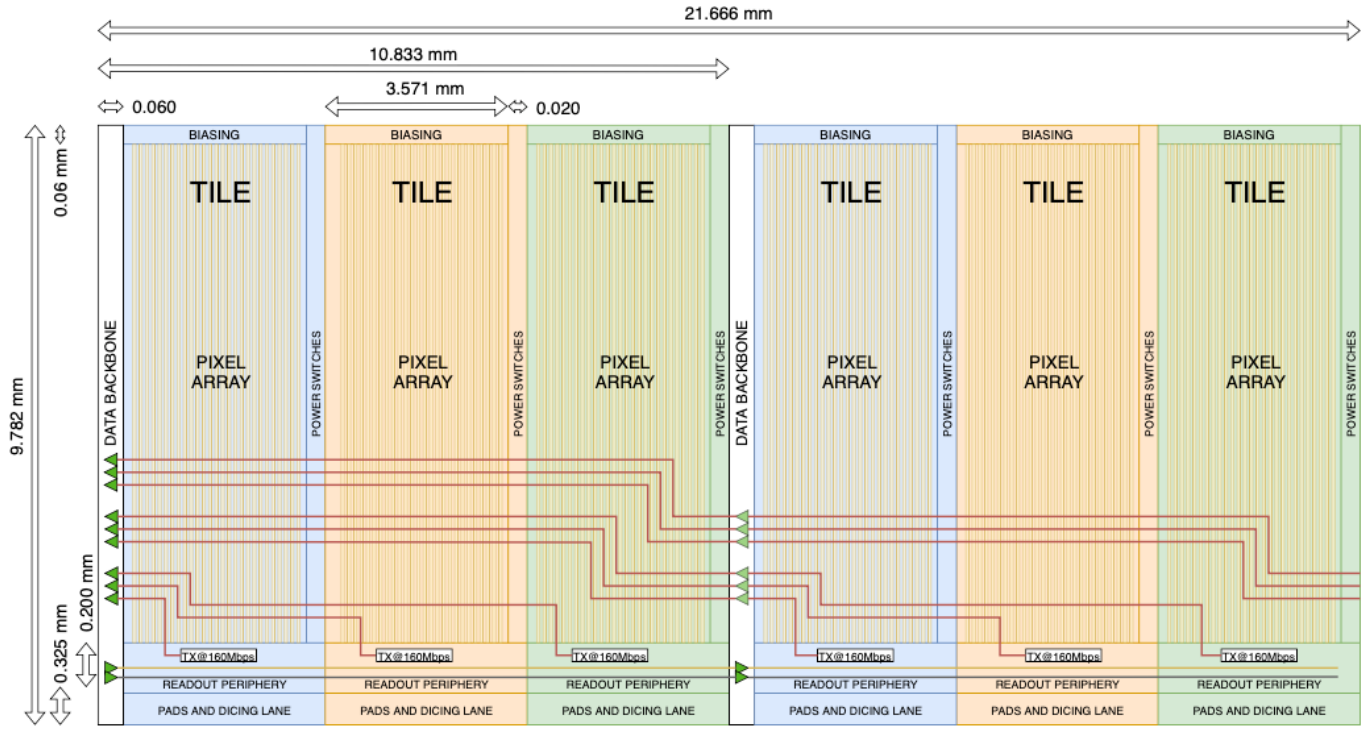


Half Repeated Sensor Unit

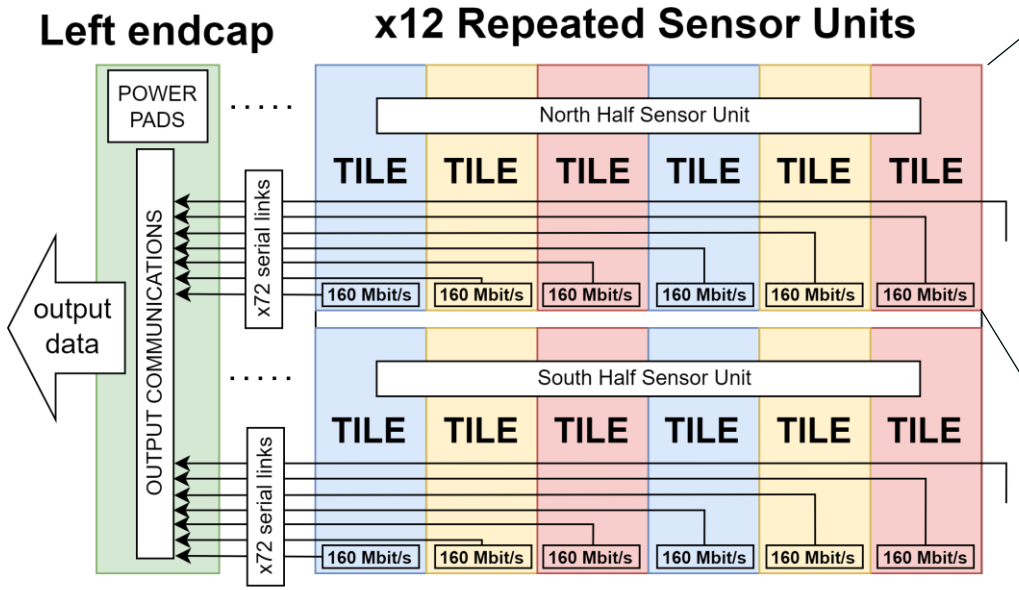


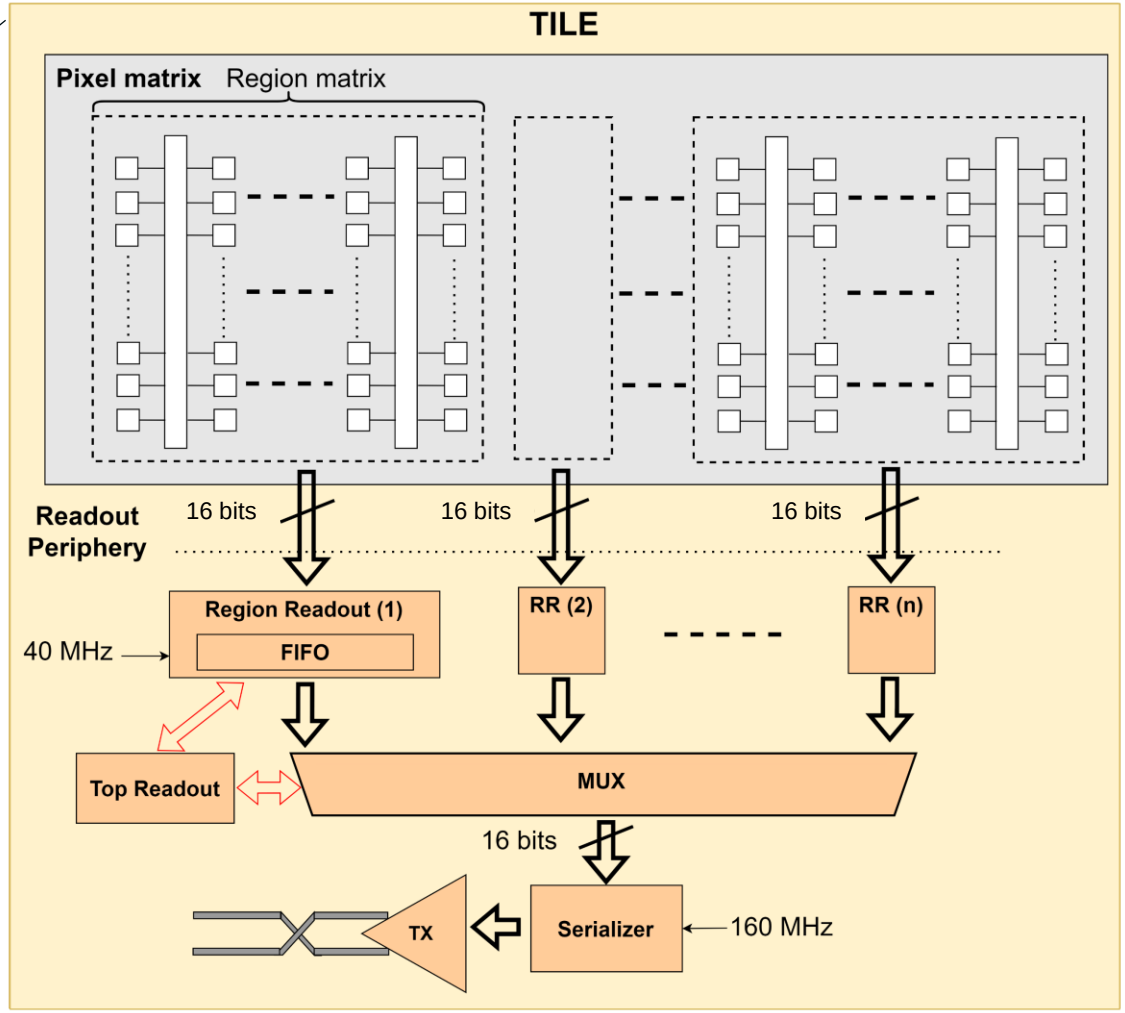
Each Half Unit is segmented in **Tiles** (Domains)

Each **tile** acts as an **independent sensor**
Separate Local Power
Configuration
Readout Link (160 Mb/s)
Each **Tile** data output has direct connection to the **left endcap**

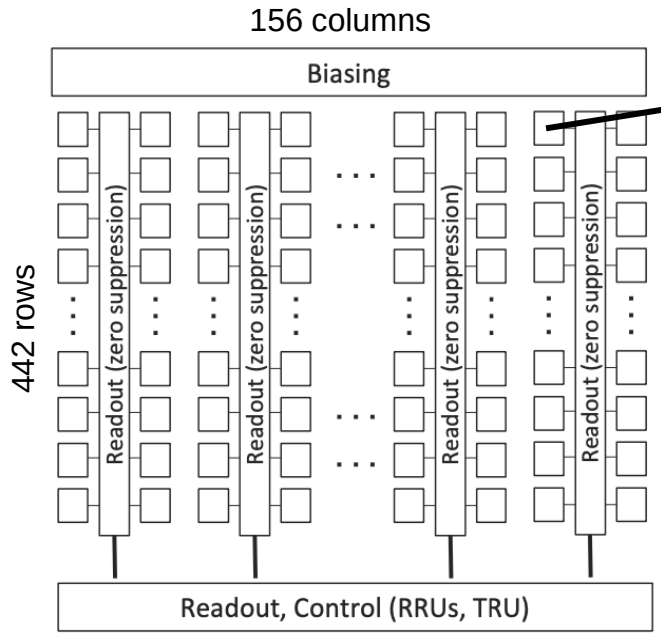


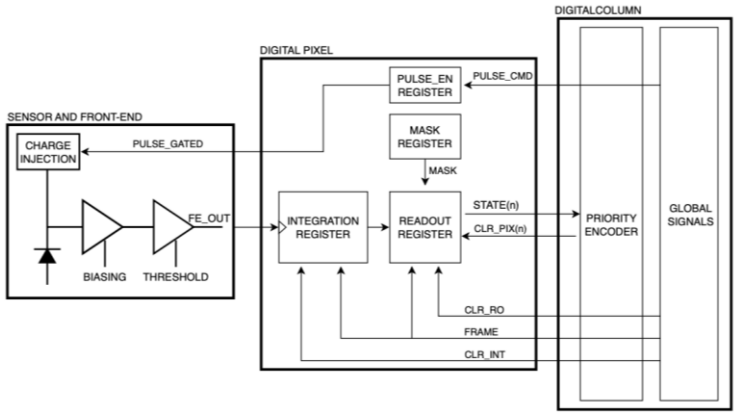
Tile Readout Scheme





Pixel Array Readout Architecture





442 x 156 pixels / domain
827,424 pixels per RSU
144 domains / segment
9.929 Mpixels / segment

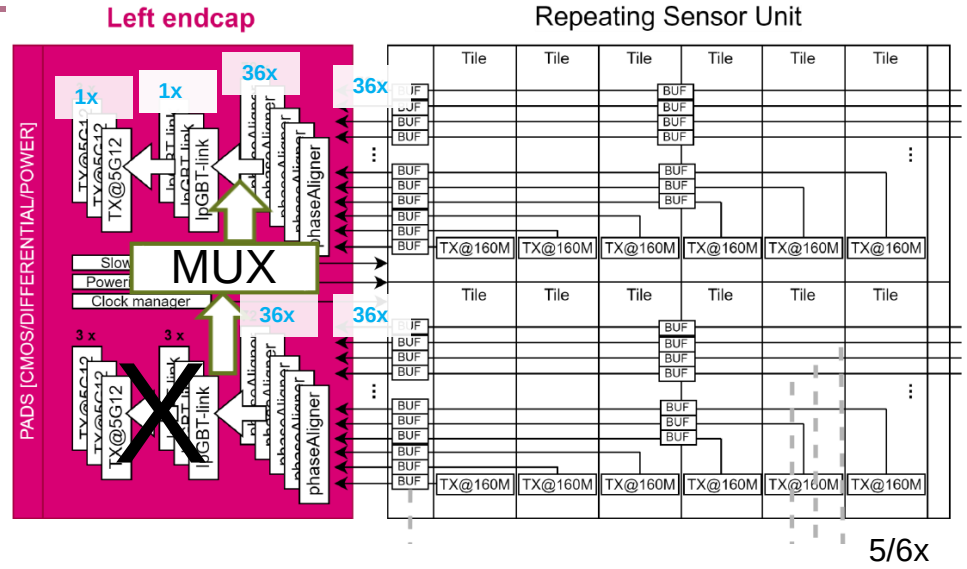
20.8 µm x 22.8 µm pixel pitch
Continuously active front-end (40 nW typ.)
Global shutter
Zero-suppressed matrix readout
Continuous readout mode
Integration time: 2 / 5 / 10µs

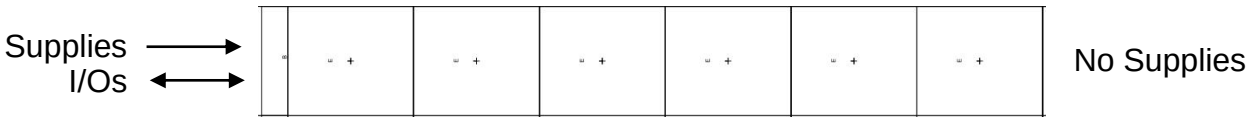
In pixel:
- Amplification
- Discrimination
- Hit integration register
- readout register
- Test charge injection
- Digital pulsing
- Masking

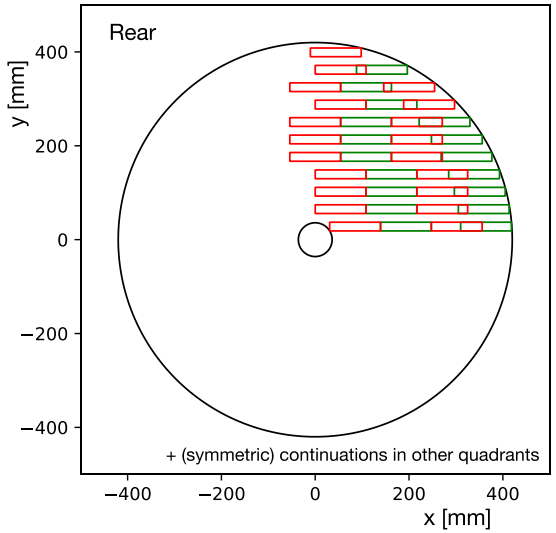
ePIC SVT: “Large Area Sensor” (LAS)

- **Inner Barrel** (Layers 0,1,2) will reuse ITS3-like sensors as is
  - **Layer 0:** 4 sensors in r-phi, 3 segments of 12 RSU
  - **Layer 1:** 4 sensors in r-phi, 4 segments of 12 RSU
  - **Layer 2:** 8 sensors in r-phi, 5 segments of 12 RSU
- EIC **variant** for the **Outer Barrel** (Layers 3,4) and **Endcap Disks**
  - “Large Area Sensor” (LAS)
  - Will be stitched, but not to wafer scale
  - Likely 1 Segment of 5 or 6 RSU (no need for right endcap)
  - The intention is to multiplex Tile data lines to **1** High-Speed output
  - More conventional carbon composite mechanical support with integrated cooling

6-RSU LAS







Backup

VTRx+ Front-end Module

- **Versatile**
  - Up to 4 Tx + 1 Rx, configurable by masking channels
- **Miniaturised**
  - 20 x 10 x 2.5 mm
- **Pluggable**
  - Electrical connector
- **Data-rate**
  - Tx: up to 4×10 Gb/s, Rx: 2.5 Gb/s
- **Environment**
  - Temperature: -35 to + 60 °C
  - Total Dose: 100 Mrad
  - Total Fluence: $1x10^{15}$ n/cm^2 and $1x10^{15}$ hadrons/cm^2
- **Status**
  - Pre-production ongoing
  - Solving problems with module assembly
    - Alignment of optical components
  - Ramping up to 2k modules/month in 2023