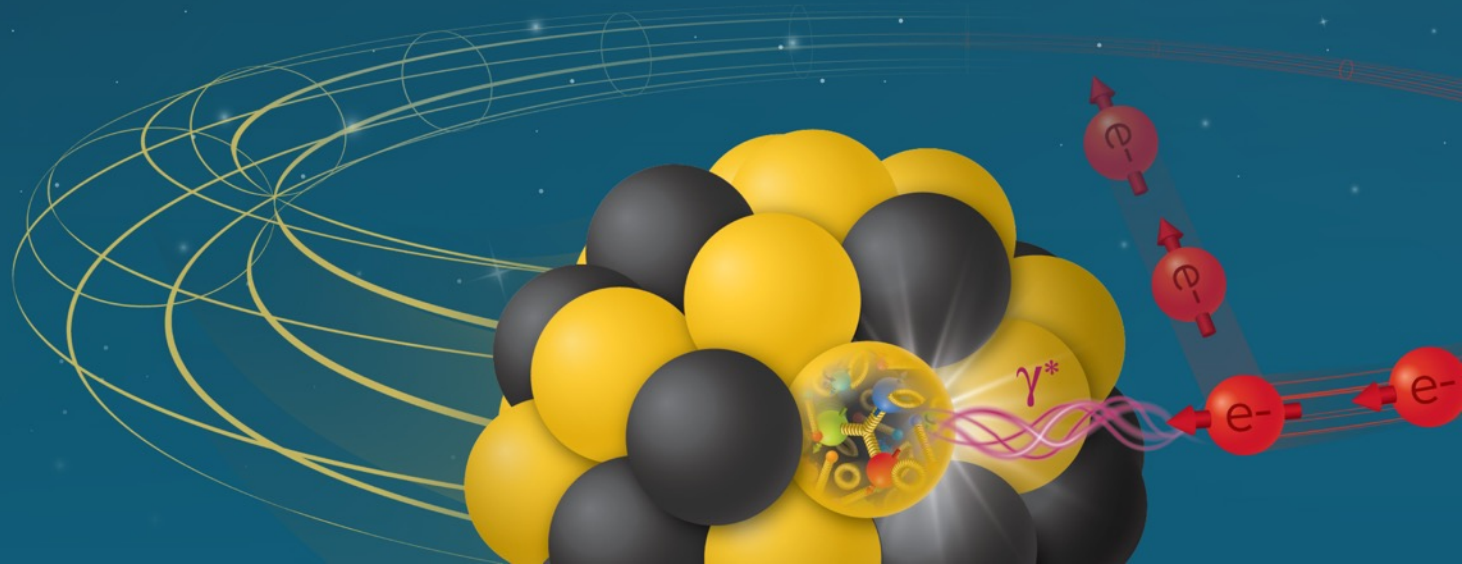
Tracking Systems Overview and Requirements

Brian Eng
L3 CAM
Jefferson Lab

Incremental Design and Safety Review
of the EIC Tracking Detectors
March 20-21, 2024

Electron-Ion Collider



Charge Questions Addressed

1. Are the technical performance requirements appropriately defined and complete for this stage of the project?
2. Are the plans for achieving detector performance and construction sufficiently developed and documented for the present phase of the project?
3. Are the current designs and plans for detector, electronics readout, and services sufficiently developed to achieve the performance requirements?
4. Are plans in place to mitigate risk of cost increases, schedule delays, and technical problems?
5. Are the fabrication and assembly plans for the various tracking detector systems consistent with the overall project and detector schedule?
6. Are the plans for detector integration in the EIC detector appropriately developed for the present phase of the project?
7. Have ES&H and QA considerations been adequately incorporated into the designs at their present stage?

Outline

- Requirements
- Interfaces
- Tracking Detector Layout
- Risks
- Safety
- Summary

Requirements

Charge 1

- https://eic.jlab.org/Requirements/index.html

	Momentum Resolution	Spatial Resolution
Backward (-3.5 to -2.5)	~0.10%×p⊕2.0%	~ 30/pT μm ⊕ 40 μm
Backward (-2.5 to -1.0)	~ 0.05%×p⊕1.0%	~ 30/pT μm ⊕ 20 μm
Barrel (-1.0 to 1.0)	~0.05%×p⊕0.5%	~ 20/pT μm ⊕ 5 μm
Forward (1.0 to 2.5)	~0.05%×p⊕1.0%	~ 30/pT μm ⊕ 20 μm
Forward (2.5 to 3.5)	~0.10%×p⊕2.0%	~ 30/pT μm ⊕ 40 μm

Interfaces

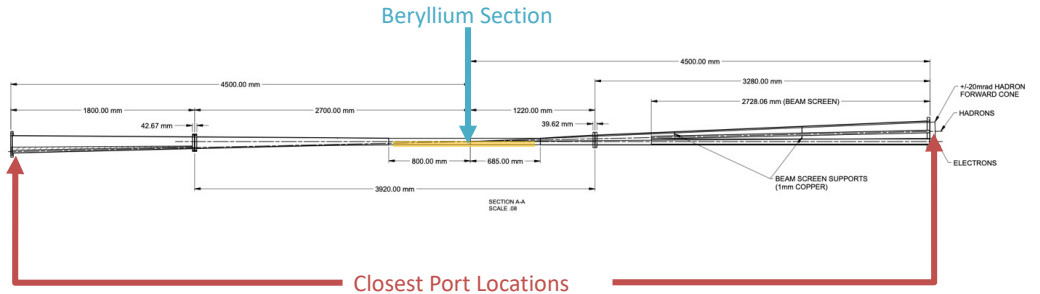
Charge 1

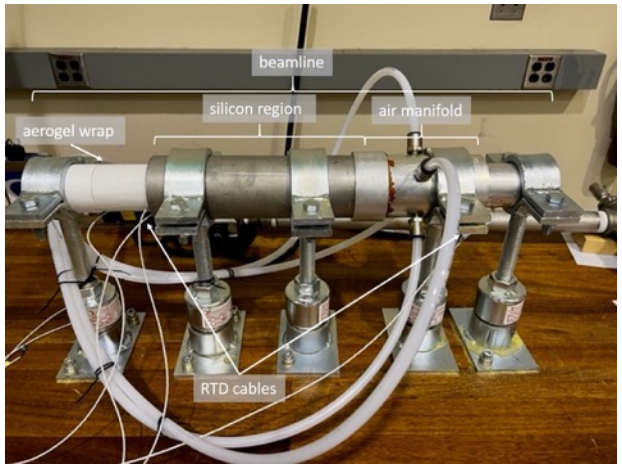
- https://eic.jlab.org/Interfaces/InterfaceMatrix.html
  - Outer barrel limited by DIRC
  - Disks limited by pfRICH/AC-LGAD
  - Inner Barrel first vertex layer 5mm from beampipe

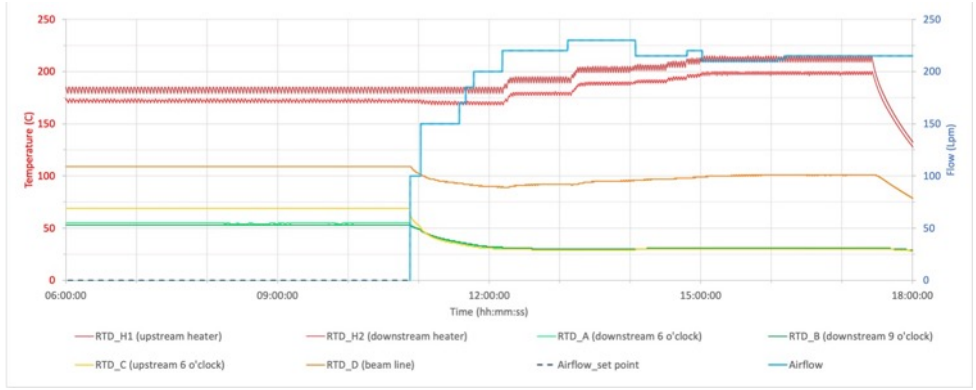
Interfaces – Beam Pipe

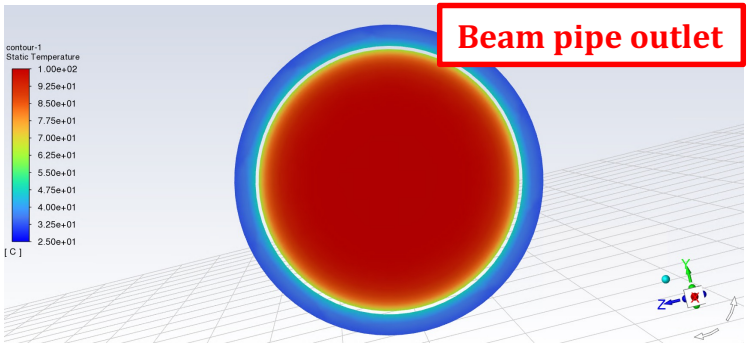
Charge 1

- Unique beampipe
  - Tapered beampipe, tracking detectors must be installed prior to beampipe installation in central detector
  - Beampipe exposed to ambient prior to installation
  - Need min 100°C in beampipe to break H_2O bonds
    - Silicon detector epoxy limited to ~30°C due to CTE





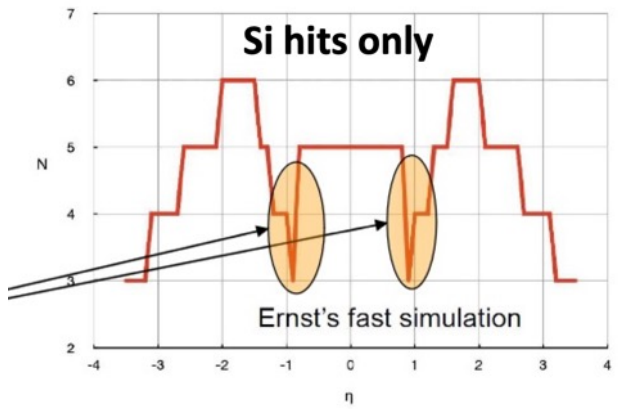




Tracking Detector Layout Modifications

Charge 2, 3

- Low number of hits in certain rapidity ranges
  - Need more planes

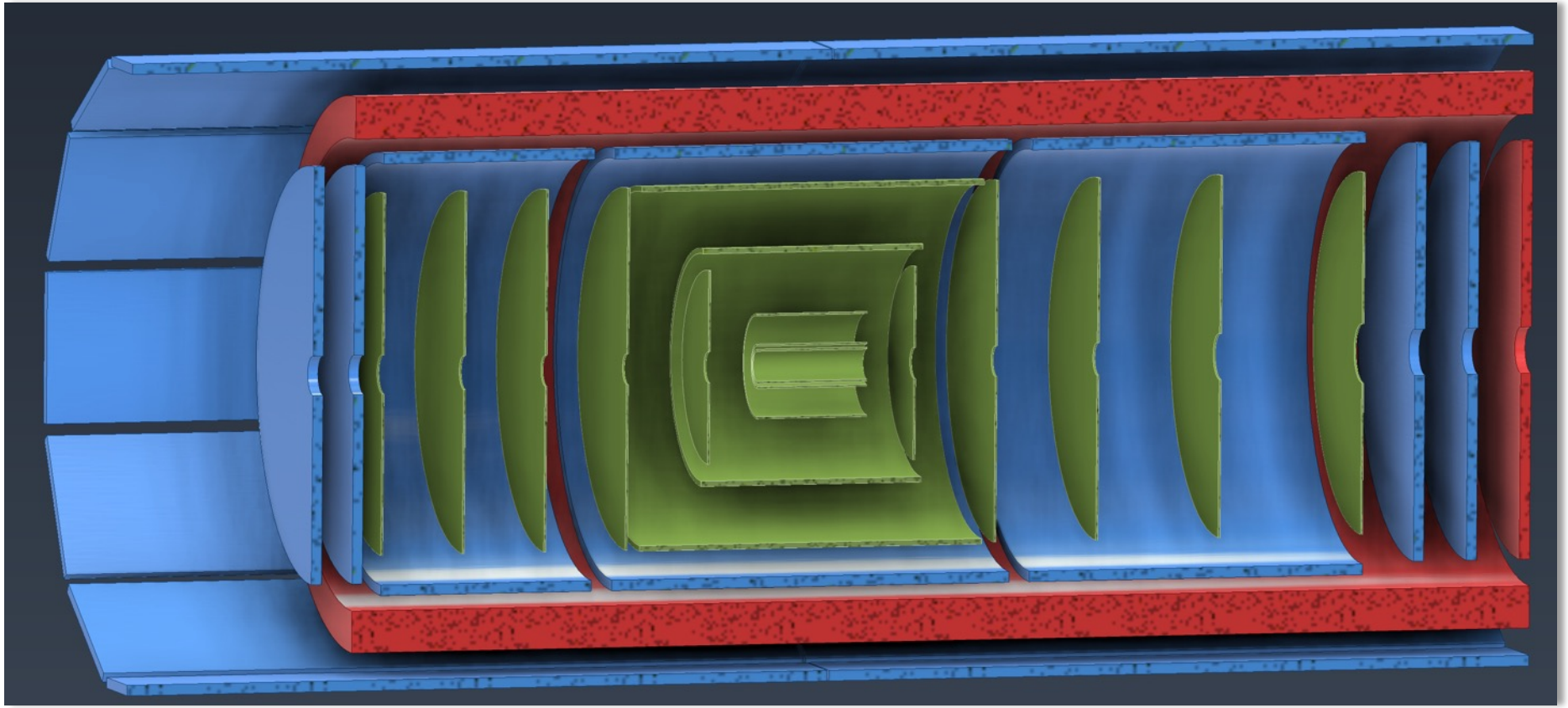


- Solve impact from 5 (2) μs MAPS frame accumulation time
  - Need enough hits from fast detectors to form a tracklet with a good pointing resolution
  - Need to utilize ToF and maybe Barrel-ECal AstroPix as possible
    - Note: Barrel ToF has good time resolution but not spatial resolution

- Current layout finalized in June 2023

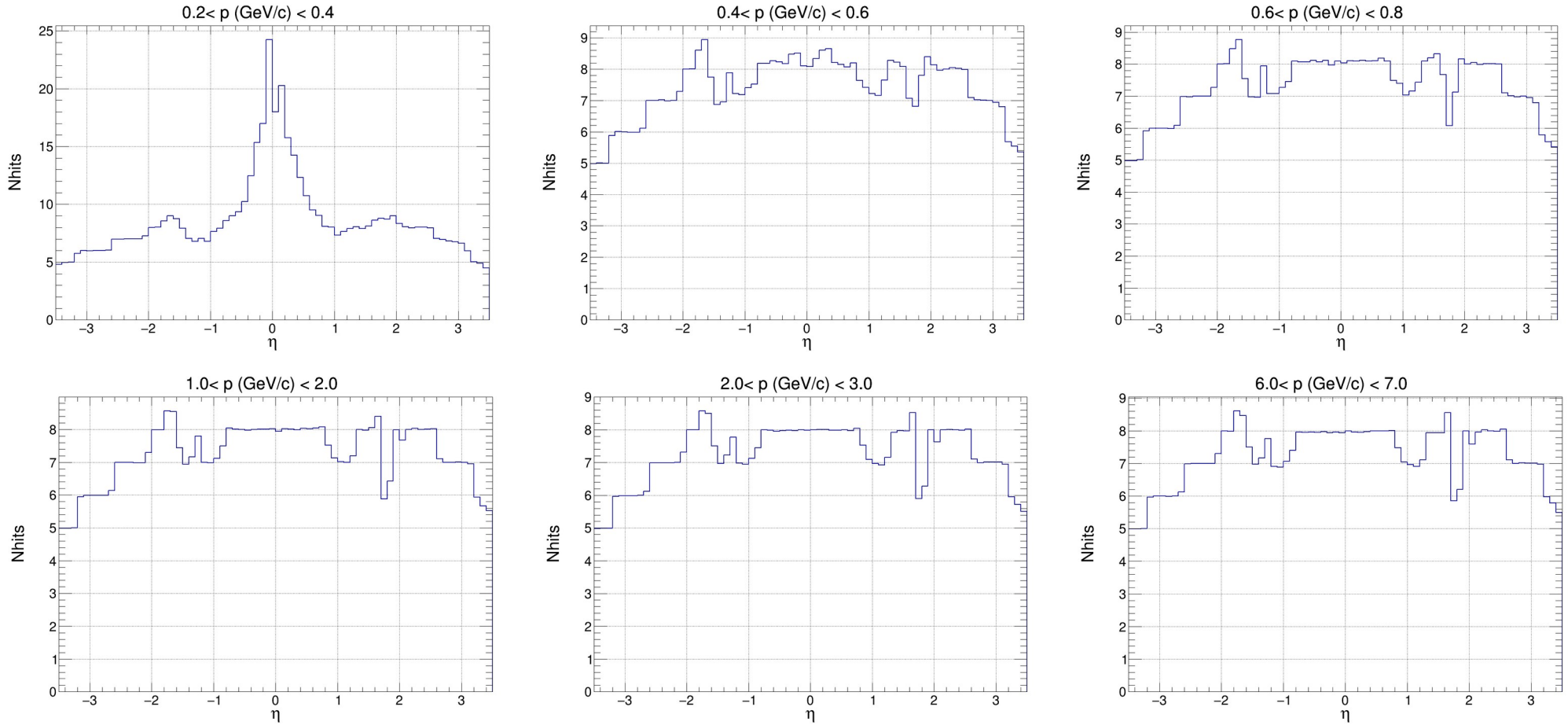
Tracking Detector Layout

- Silicon
- MPGD
- ToF
  - Part of PID



Simulation – Nhits vs η

- Only tracking detectors included, will improve further once calorimeters included which should remove dip at rapidity ±1



Silicon

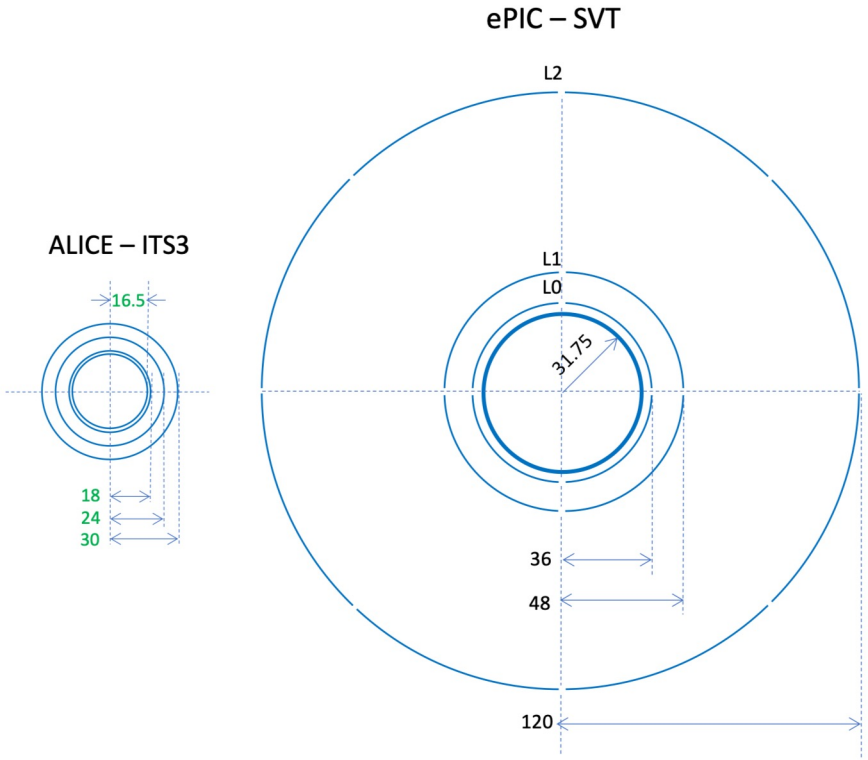
- MAPS (monolithic active pixel sensors) in 65 nm CMOS technology, developed with ALICE ITS3 collaboration
  - Inner Barrel: Directly use ITS3 wafer scale sensor
  - Outer Barrel: EIC Large Area Sensor (LAS), modification of ITS3 sensor

- EIC Project, Silicon Consortium and CERN ALICE/ITS3 meeting in Q2 23
  - Path forward on collaboration (paperwork in process), EIC hiring 2 engineers to work directly with ALICE team on sensor development

Silicon – Inner Barrel

- Three layers of thin, bent, wafer scale ITS3 based sensors
- ITS3 concept adapted to ePIC radii
- X/X0 % = 0.05

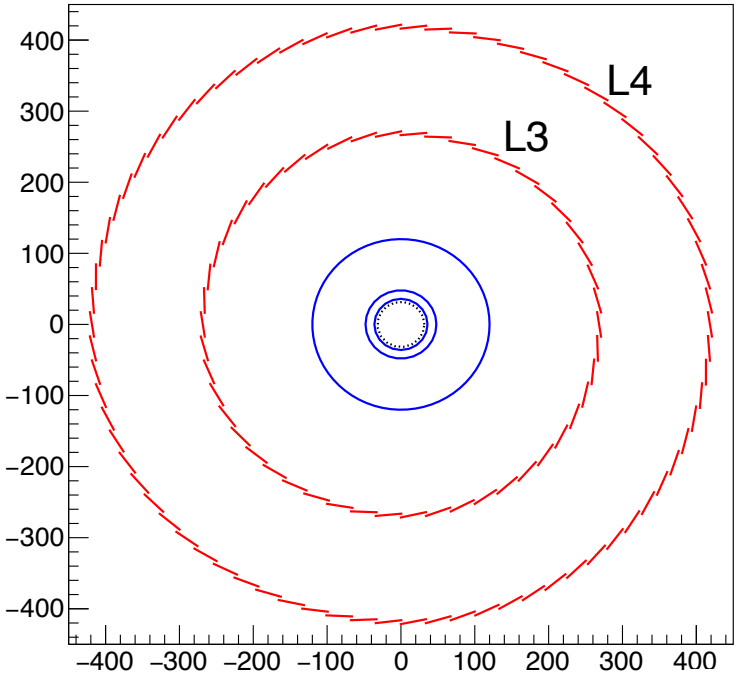
Layer	Radius (mm)	Length (mm)	Segments
L0	36	270	3
L1	48	270	4
L2	120	270	5



Silicon – Outer Barrel

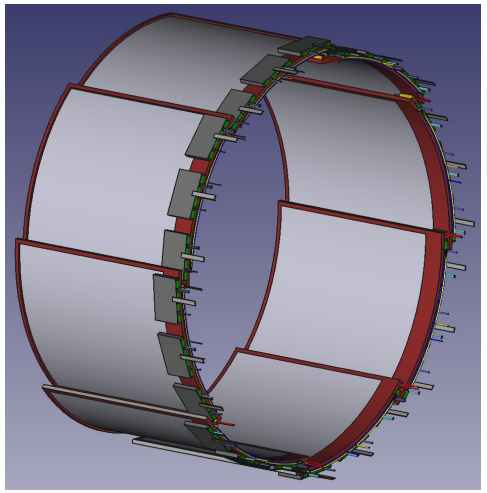
- Traditional stave design

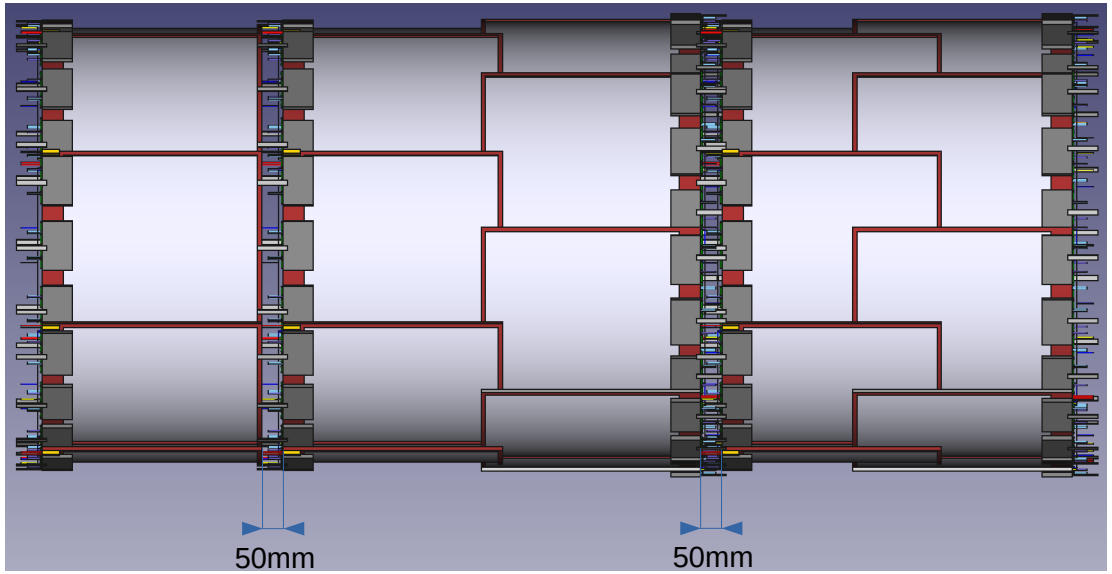
Layer	Radius (mm)	Length (mm)	X/X0%
L3	270	540	0.25
L4	420	840	0.55



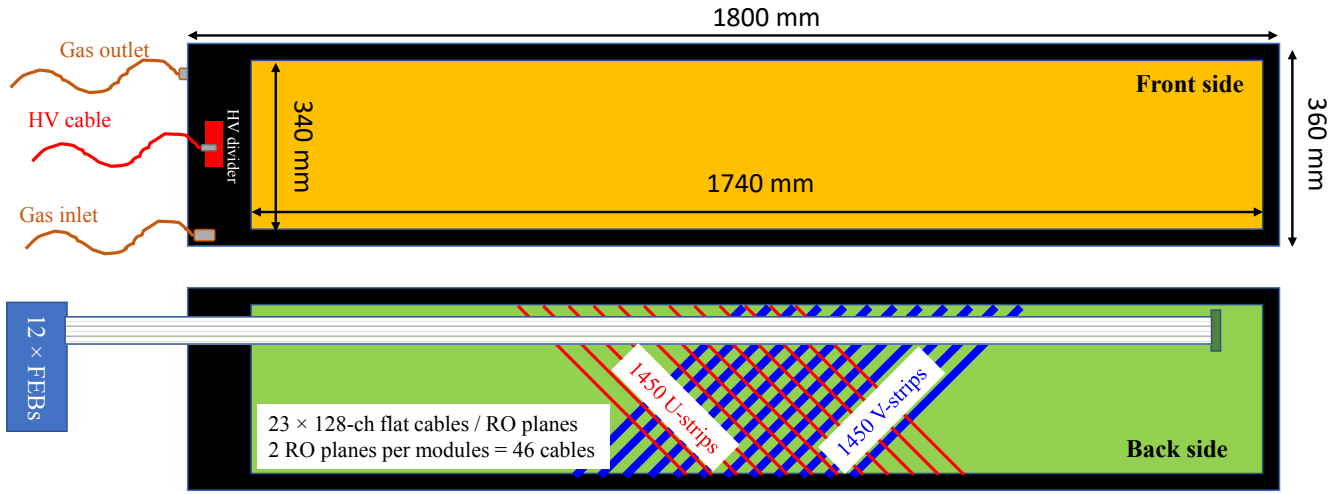
Outer Barrel – MPGD

- Micromegas
  - Additional Tracking Points
- Single Tile
  - 51.25 x 44 cm
  - Simplifies production
  - 40 Tiles Total
  - ~30k Channels





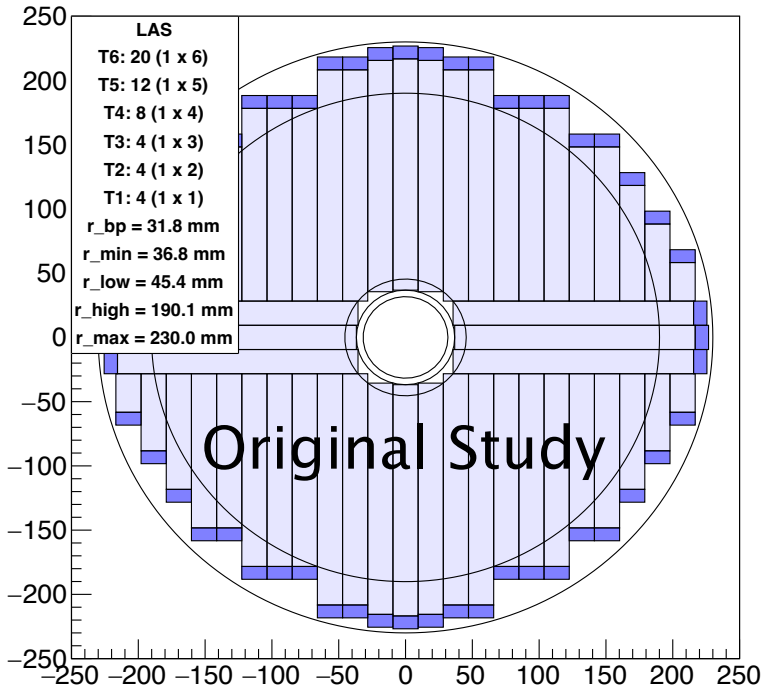
- uRWELL
  - Provides hits for DIRC
- Capacitive-sharing 45° U-V strips
  - Pitch: 1.2 mm pitch
  - ~140k Channels



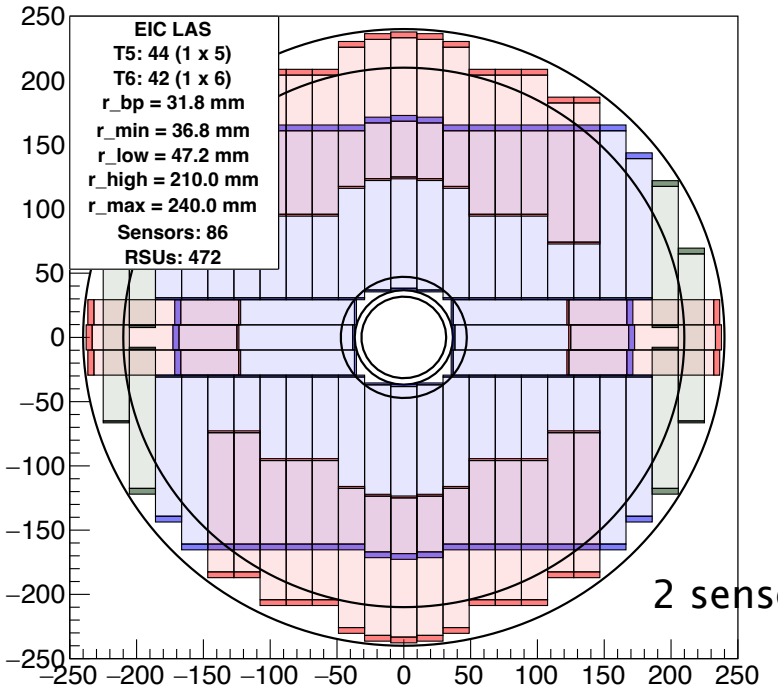
Forward / Backward Disks – Silicon

- Foundry rule/limitation, need to limit number of sizes (2-3 total)
  - Direct outcome from meeting with ALICE

EIC-SVT Disk-1 Tile



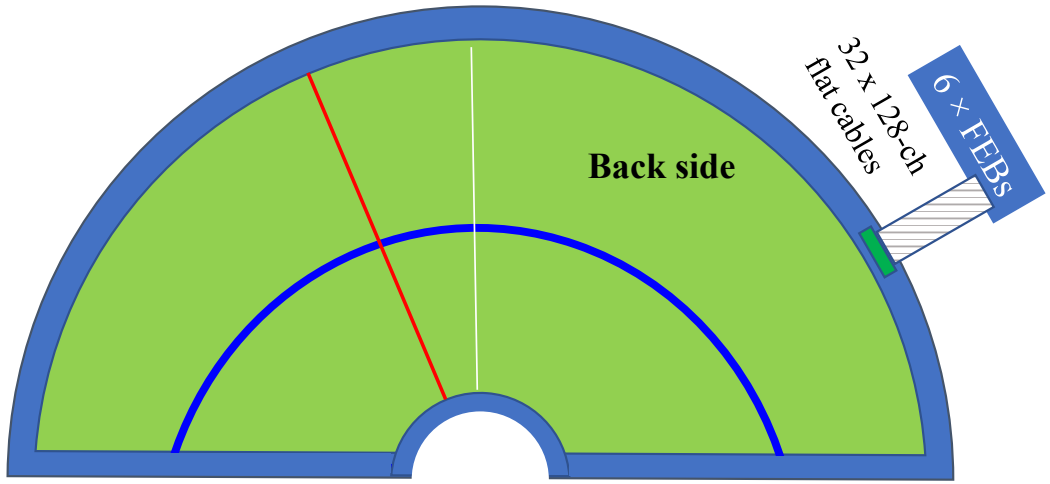
ePIC-SVT ED0/HD0 z=-/+250 cm

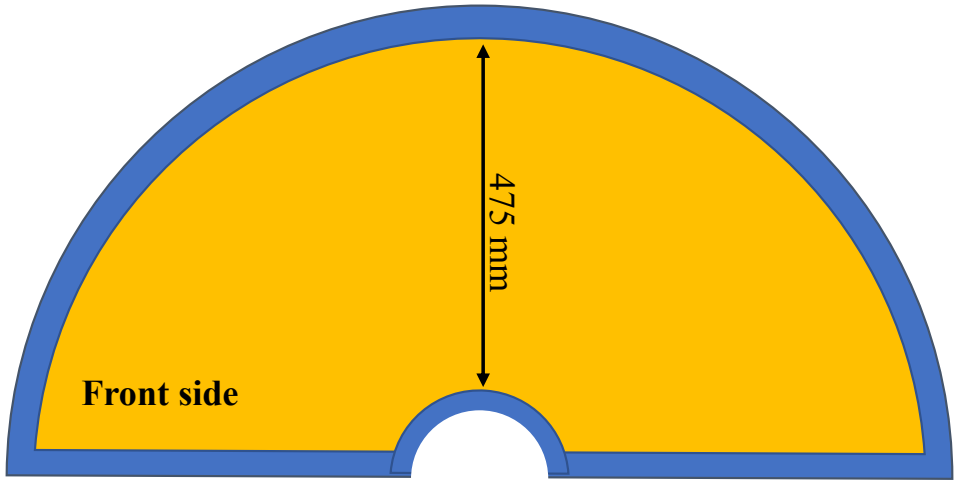


2 sensor layers

Forward / Backward Disks – MPGD

- uRWELL Capacitive-sharing 45° r-phi strips
- Pitch: 1.2 mm pitch
- ~2 × 1570 phi-strips + ~ 2 × 400 r-strips
  - ~4k strips per disk (32k channels for 8 disks)

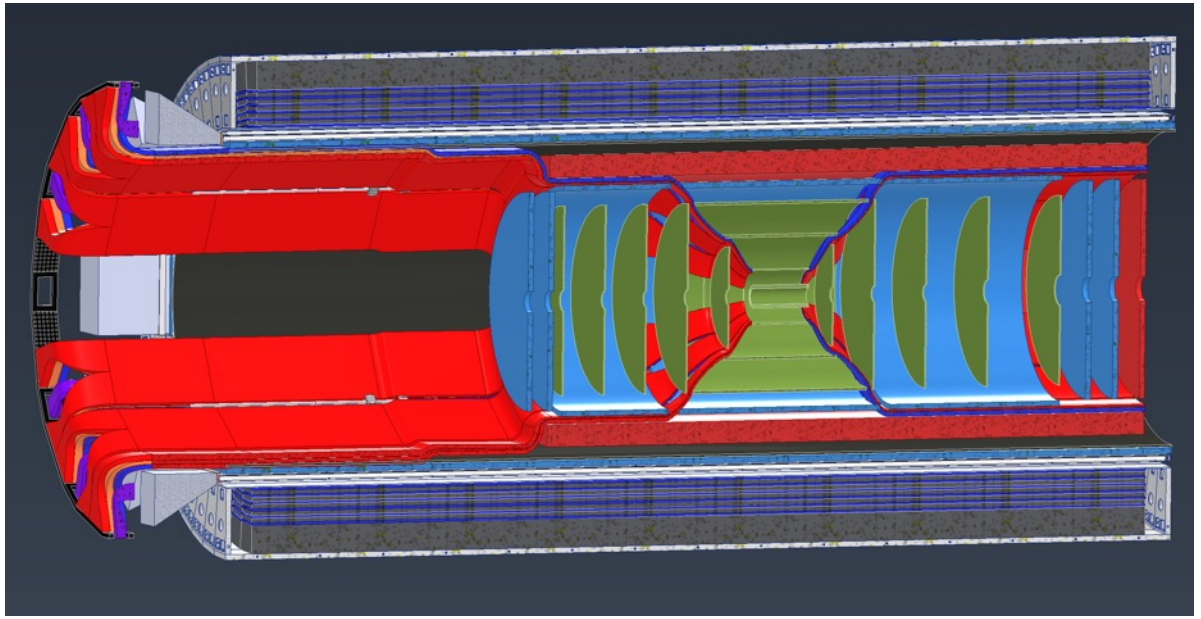


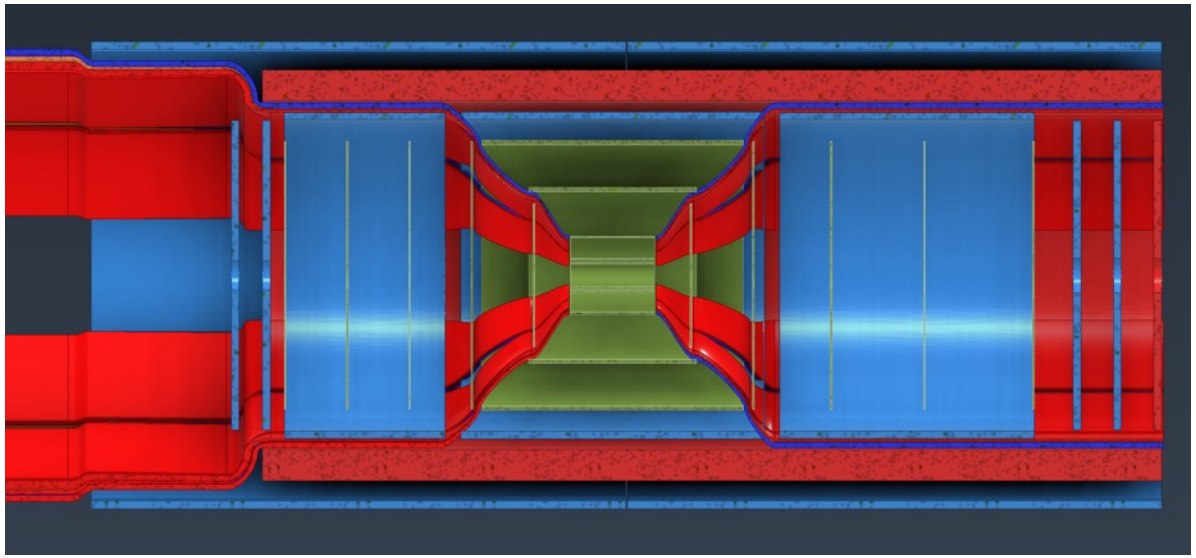


Services

Charge 3

- RED = power
- BLUE = cooling/gas
- ORANGE = signal





Services

Charge 3

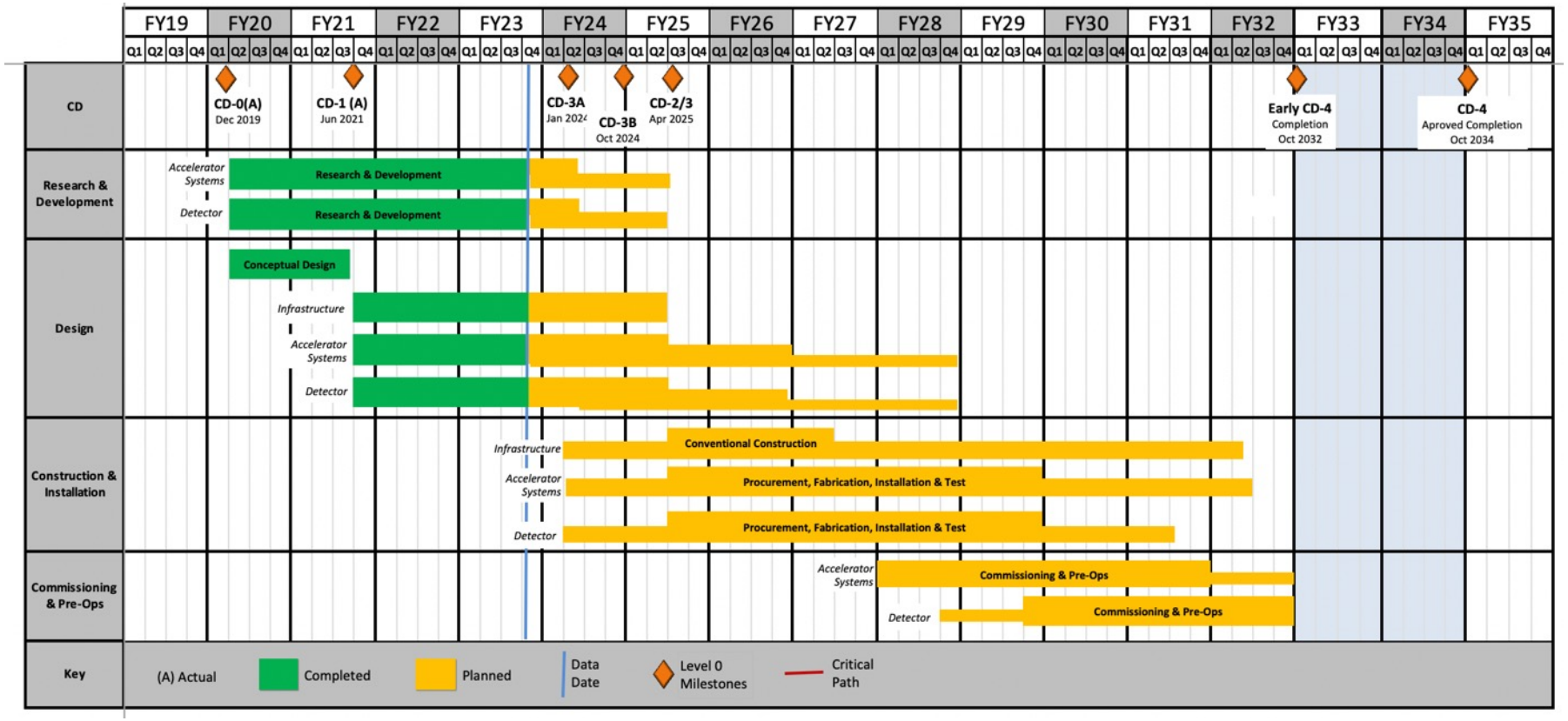
Subsytem	Type	Item	Material	Quantity	Diameter (cm)	Cross Area (cm^2)	+50% Packing for Bundles	Average Length (in)
Red Path IP to pfRICH Inner face								
Vertex Silicon	Power	18 awg LV Sagita	Aluminium	12	0.8	6.03	9.05	120.00
	Signal	Signal Bias		34	0.2	1.07	1.60	120.00
	Signal	Data *		204	0.6	57.68	86.52	120.00
	Cooling	*		12	0.3	0.85	1.27	
Sagita Silicon	Power	LV serial power		29	0.9	18.45	27.67	
	Signal	Signal Bias		771	0.3	54.50	81.75	
	Signal	Data *		771	0.2	24.22	36.33	
	Cooling	Cooling Pipes *		356	0.3	25.16	37.75	
Silicon Disks	Signal	Sensor Bias	Aluminium	1100	0.3	77.75	116.63	120.00
	Cooling	cooling	tygon	550	0.63	171.45	257.17	120.00
	Power	LV current	Aluminium	92	0.9	58.53	87.79	120.00
	Signal	Data		1100	0.3	77.75	116.63	
Inner MPGD	Signal	FEE Data	Firefly	60	1	47.12	70.69	120.00
	Power	Hv		40	0.32	3.22	4.83	120.00
	Power	Lv		20	1.163	21.25	31.87	120.00
	Cooling	Gas	Polyethylene	20	0.4	2.51	3.77	120.00
	Cooling	Cooling	Polyurethane	33	0.63	10.29	15.43	120.00
EE MPGD Disks	Power	FEE PWR	20 awg (3 pair)	11	1	8.64	12.96	120.00
	Signal	FEE data	Fibers	128	0.32	10.29	15.44	120.00
	Power	2kv Hv	Coax	4	0.24	0.18	0.27	120.00
	Signal	Flat Signal Cables		128	0.3	76.80	115.20	120.00
	Cooling	Gas	Tygon	8	0.4	1.01	1.51	120.00
	Cooling	Cooling	Tygon	16	0.63	4.99	7.48	120.00

- Inner most trackers cable path towards Lepton end
- ~71% space used

Cost / Schedule

Charge 5

- Cost / Schedule is based on engineering estimates from detector experts



- Inner Barrel Silicon (ITS3)
  - ER2 – Q1 24
- Outer Barrel/Disk Silicon (LAS)
  - 2025-2027
- Stave/Disk Construction Complete
  - Q4 28
- Ready for integration
  - Q2 29

Risks

Charge 4

- Currently for the silicon trackers there is a planned engineering run during R&D with the production run taking place during PED
- Benefit from ALICE ER1 and ER2 runs and that the EIC runs would be based on the final ER3 design
- However, if unforeseen issues arise another engineering run for the sensors might be needed
  - The risk register has a proposed risk (ID RT-6-10-014) if a second engineering run is needed which would use contingency

- CD-3A Director's Review comment:
  "Upfront discussion of risks of R&D not coming to a favorable conclusion, and mitigation plans in this case, should be more clearly documented and presented. Where appropriate, for example for the tracking detector, more detailed plans should be developed."
  - Silicon detectors have external dependency on ITS3 sensors
  - See backup slides for alternative layout discussion

Safety

Charge 7

- Generally the tracking WBS is in the design phase and and such doesn't have any safety issues

- However, there are a few test stands being developed which follow their institution's safety protocols
  - Protocols include required training
  - LBNL testing carbon foam cooling: ISM, documented in Work Planning & Control
  - JLAB testing beampipe bake-out: ISM, Task List and ePAS (JLab-PR-725)

- Equipment going in the BNL Experimental Hall must follow NEC/NFPA 70E, 2021 and electrical safety guidelines: DOE-HDBK-1092-2013
  - Defines voltage hazards, cable type requirements, circuit protection, etc
  - Equipment must be NRTL listed or approved by BNL Electrical Equipment Inspection program

Summary

- Recent design change to address performance issues, which has been incorporated into the ePIC collaboration's latest models
- Cost and schedule developed with input from ePIC collaborators and ALICE/ITS3 efforts
  - Scope change request for additional personnel based on discussions from CERN visit in progress.
- Tracking WBS is in the final design stage no major ES&H issues
  - Test stands follow the relevant institution's policies.
- Proposed risk added to register for additional engineering runs of silicon sensors

Backup

Collaboration

Alternative Tracker

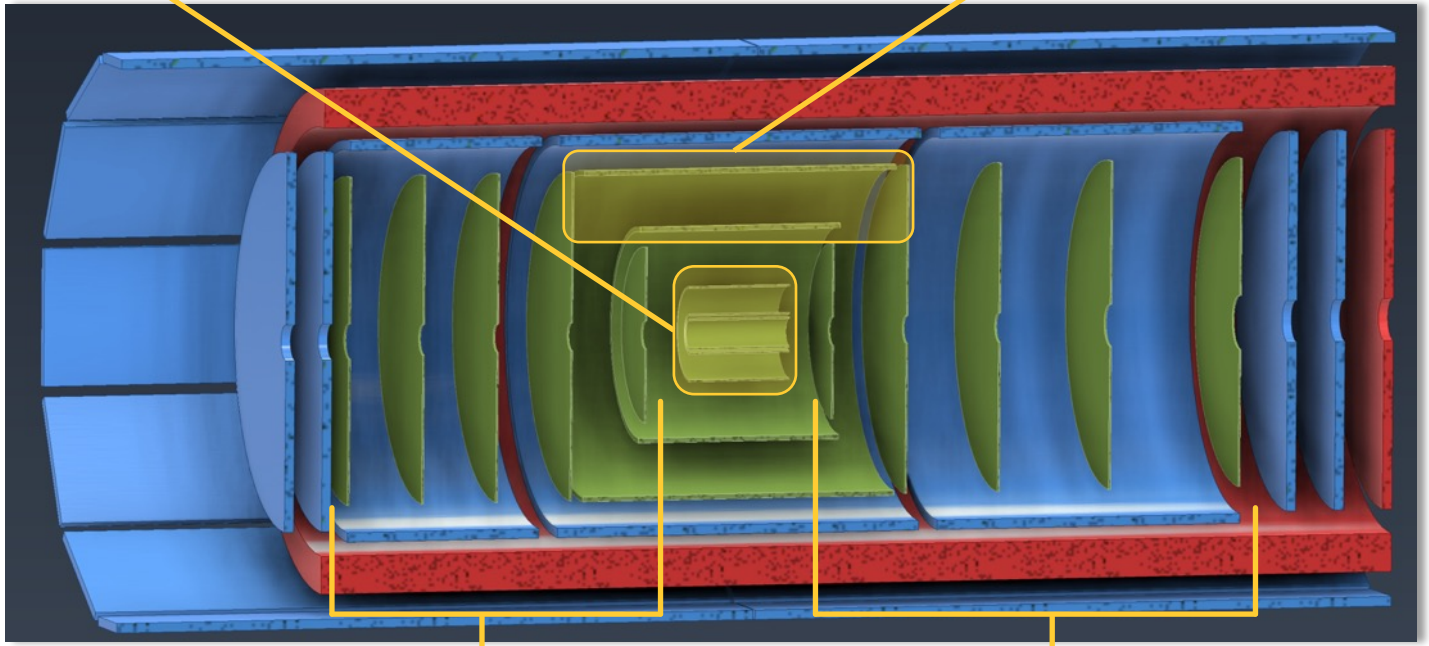
- Goal is always to progress towards using ITS3 based sensors
  - Only way to meet full performance requirements

- Branchpoints – both based on schedule delays

1. ITS3 (inner barrel) schedule remains compatible with project schedule but LAS (outer barrel & disks) development is delayed
2. ITS3 (inner barrel) schedule becomes incompatible with project schedule

Alternative Tracker – Layout

Replaced by two or three layers based on the existing ITS2 sensor, as used in ALICE and sPHENIX without EIC specific modifications
Branchpoint 2 only



Replaced with two MPGD barrel layers derived from the outer MPGD tracker, specifically its innermost (Micromegas) layer
Branchpoint 1 & 2

Replaced with (in total up to) seven near-identical MPGD disks on each side, specifically based on existing uRWELL disks
Branchpoint 1 & 2

Alternative Tracker – Schedule

- Will be further refined leading up to CD-2 based on ITS3 development

Branchpoint	Date	Milestones
1 (LAS Delay)	Q2/Q3 2026	1 year for MPGD foils + 3 years construction
2 (ITS3 Delay)	Q3/Q4 2027	Same 3 years construction as current IB