ePIC Tracker PDR: MPGD electronics

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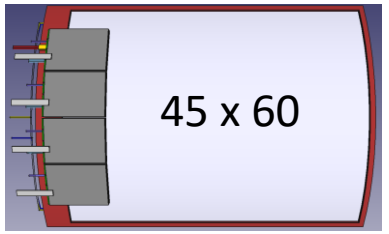
Outlook

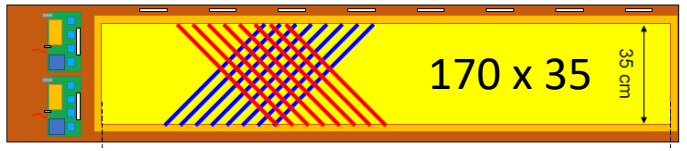
- Requirements
- Architecture
  - → Salsa ASIC
  - → FEB
  - → Data
  - → Services
- Organization
  - → Production startegy
  - → Planning
  - → QA and risk mitigation
- Summary

Reminder on MPGD sub-systems and channel counts

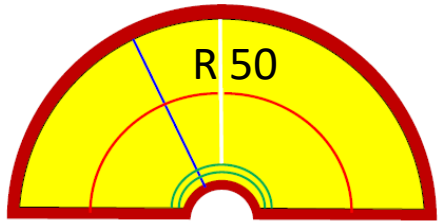
- Cylindrical Micromegas Barrel Layer : CyMBaL : ~32k channels
  → 32 tiles of 1024 channels each



- µRWELL Barrel Outer Tracker : µRWell-BOT : ~100k channels
  → 24 modules of 4 096 U-V strips each

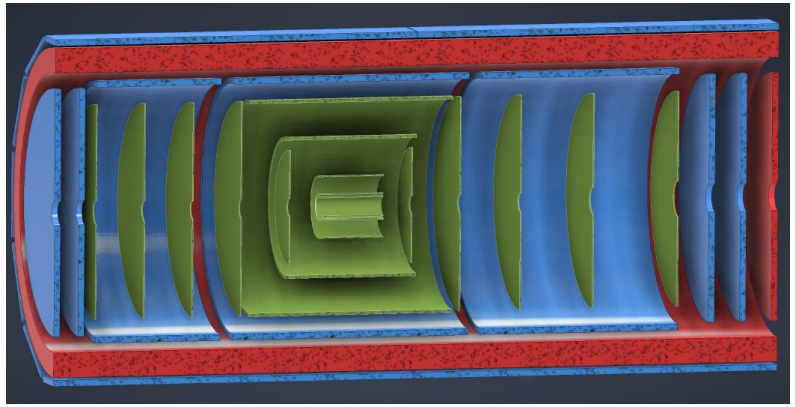


- µRWell End Cap Tracker : µRWell-ECT : ~20k channels
  → 8 DEEs of 2 400 R-Phi strips each

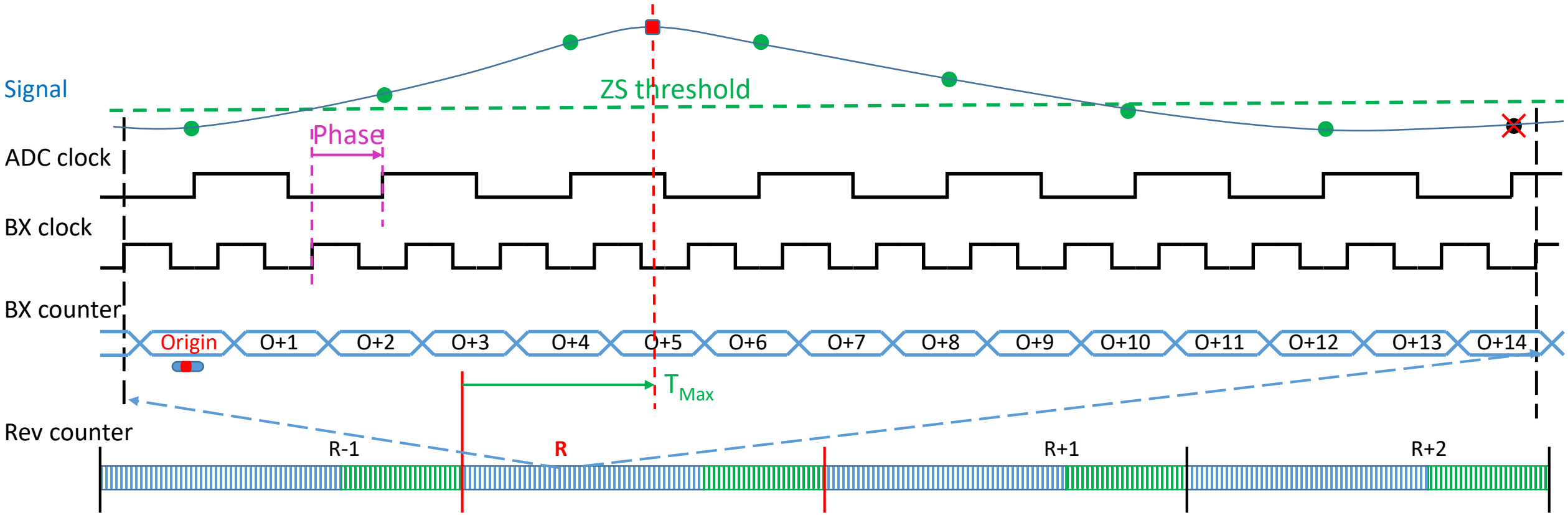


- ~160k-channel heterogeneous system
  → Micromegas, µRWell, barrel, endcap, curved, planar, circular

- Common approach to acquire data from different types of ePIC MPGDs
  → Use same frontend ASIC
  → Share frontend design between groups
  → Adapt FEB form factor and channel count



Readout strategy: signal shape sampling with ADC



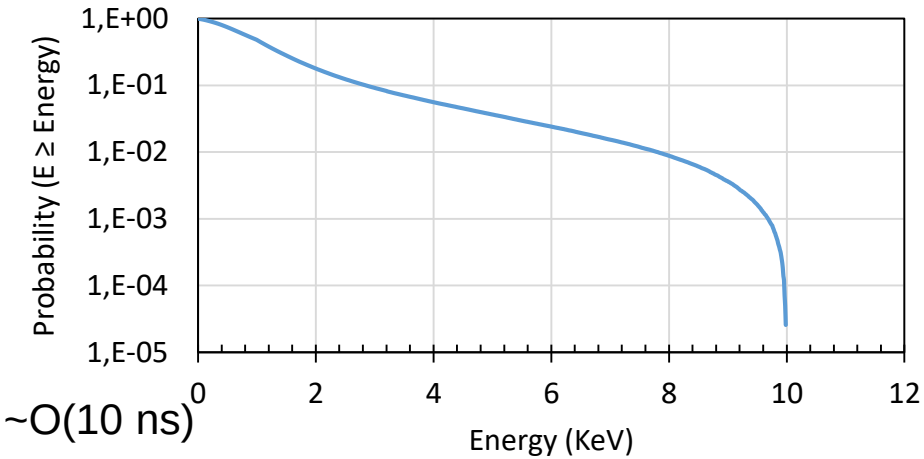
- ADC clock is derived from bunch crossing clock and is its (sub)multiple (e.g. ~50 MHz)
  → Known frequency and phase relationship exists between the two clocks

- Signal above threshold is tagged by a timestamp relative to revolution tick
  → Max (as on example) or time of arrival (fitting samples on rising edge)
  → Timing association with data from other sources possible

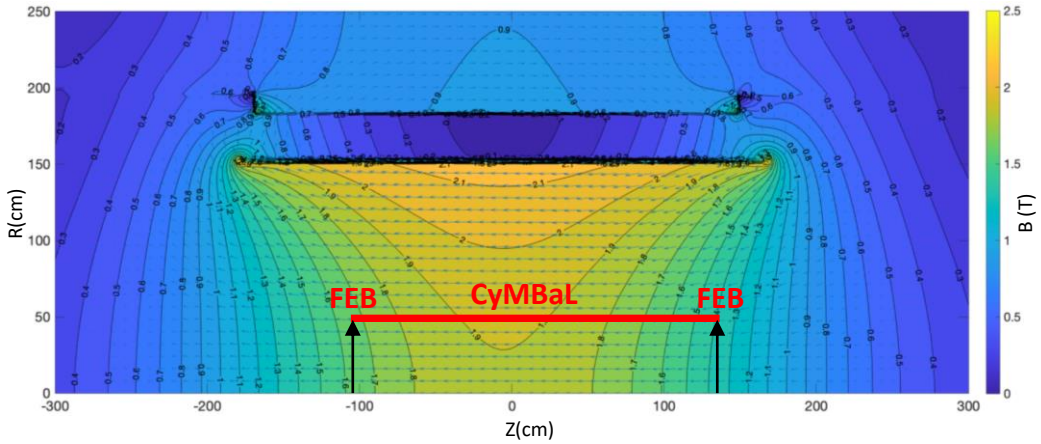
Requirements

- Typical signal 1-1.5 keV resulting to 15-30 fC per channel
  - → Cluster sizes, detector gains, charge collection
- Aimed dynamic range of 10-bits
  - → Signal / noise of ~60
    - S/Th =~10 and Th/N = ~6
  - → Max / signal of ~10
- Timing precision of few ns
  - → Low contribution to the aimed overall time measurement accuracy of ~O(10 ns)
- Channel occupancies of ~10 kHz
  - → Including factor π of safety margin
- Streaming readout
  - → With support of *in-situ* calibration and of on-demand readout
- ~1.8 T magnetic field
- Mild radiation environment
  - → TID and neutron fluence after 10 years: 10 krad and 10^{11} n_{eq} / cm^2
  - → 20 MeV proton flux: 100 particle / cm^2 / s
- Stringent space for detector readout and services

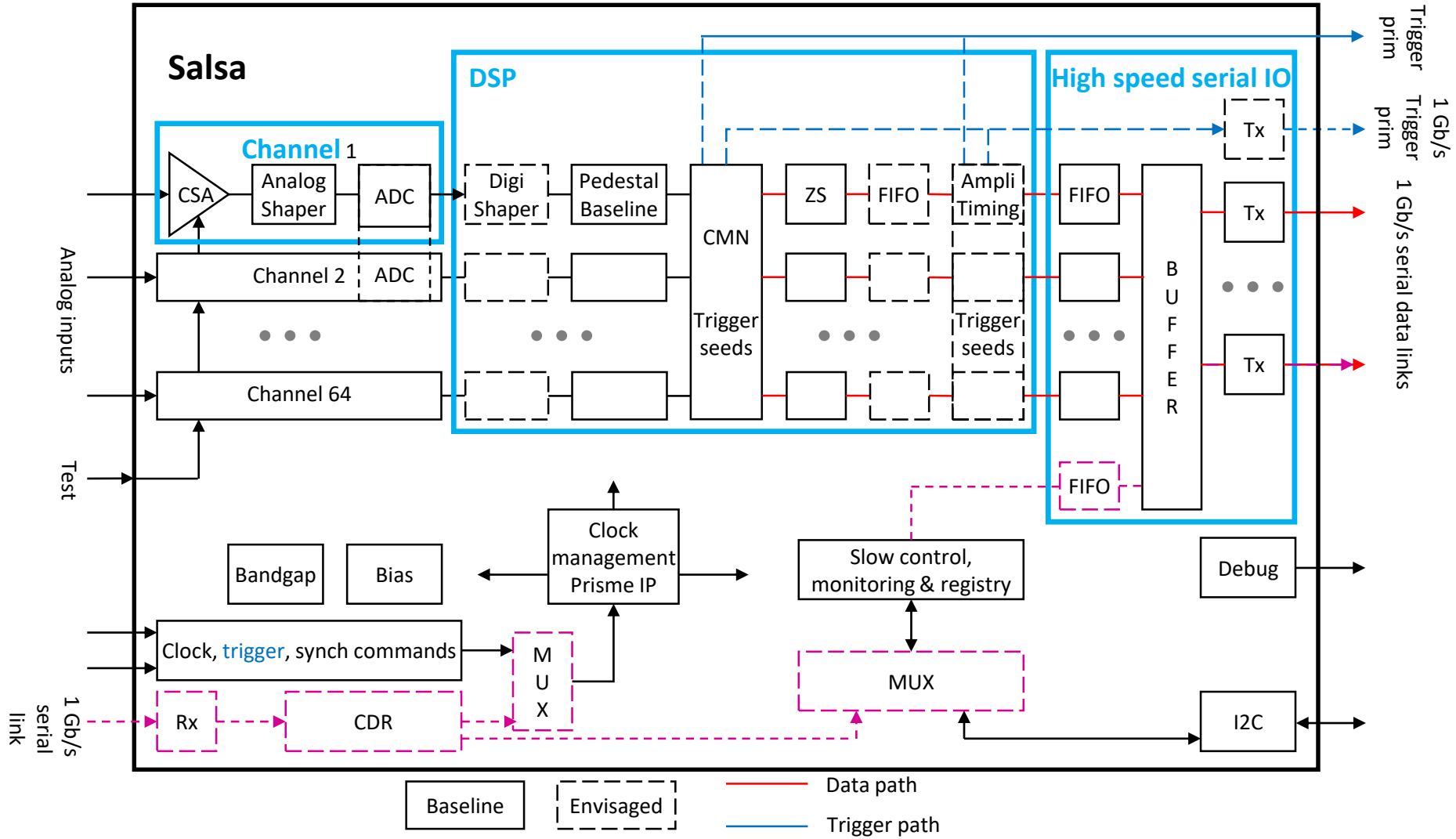
Energy deposit in CyMBaL tracker



Magnetic field map



Salsa : a 64-channel versatile MPGD readout ASIC



- Currently under development by a collaboration from Irfu, CEA Saclay and University of Sao-Paolo
  → Support from eRD109 for Salsa prototyping including clock management IP Prisme

64-channel Salsa : brief recap of specifications

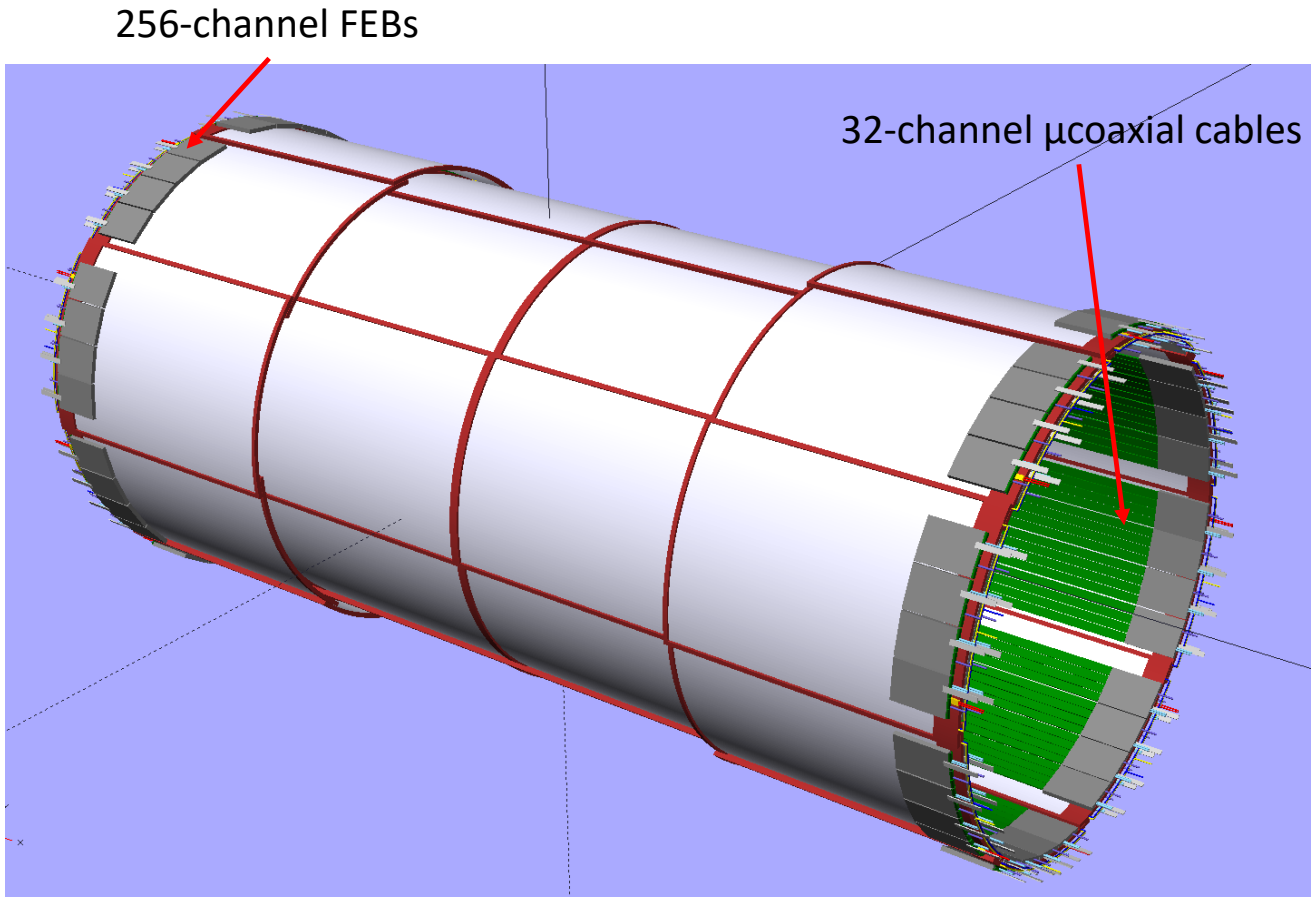
	ePIC MPGDs
• **Channel features**	
→ 4 dynamic ranges : 50 fC, 250 fC, 500 fC, 5 pC	250 fC
→ 10 peaking times : from 50 ns to 500 ns	200 ns
→ Support for high input capacitances up to 1 nF and beyond	~200 pF
→ Both signal polarities	Negative
→ Rate per channel : up to 100 kHz	<10 kHz
→ Sampling rate : programmable, up to at least 50 MSPS	50 MSPS
→ 12-bit ADC with >10-bit ENOB	>9.6 bits
• **Digital stage programmable features**	
→ Pedestal equalization, common mode noise subtraction, zero suppression	
→ Baseline tracking	
→ Signal amplitude and timing extraction	
• **Clock management with Prisme IP :**	
→ Wide range jitter cleaner PLL, 4 clock frequency synthesizer, phase adjustment	100 MHz
• **Streaming readout**	
→ 4 Gbit/s serial links	Single Gbit/s link
→ Non-ZS, signal shape or time-amplitude readout	All
• **Backend**	
→ Traditional interface with separated clock, sync command and control ports	
→ Innovative unified interface over 1 Gbit/s input link	Baseline
• **Implementation**	
→ 65 nm TSMC	
→ 10-15 mW/ch @ 1.2V	
→ Radiation hardened : SEU, > 300 Mrad, > 10^{13} n_{eq} / cm^2	10 krad, 10^{11} n_{eq} / cm^2

MPGD FEB with optical interface: aimed baseline

- FEB
  - → ASICs directly connected to 4-lane bidirectional parallel optic FireFly transceivers
    - Single Rx line encoding clock, sync run-control and asynchronous slow control and monitoring commands
  - → Low active component count
    - Easier to adapt to challenging on-detector environment
    - Samtec FireFly : reported to stand TID of 50-100 krad and neutron fluence of at least 5×10^{11} n_{eq} / cm^2
- RDO : mostly common hardware with minimal adaptation
  - → Can be placed anywhere in experimental hall with no particular environmental restrictions
- An optimal tradeoff between the complexity of the on-detector electronics and its power consumption

Example of CyMBaL: one of the possible configurations under study

- Still under torment of optimization
  - → Just a snapshot to give an idea
- 32K channels
- 128 256-channel FEBs
  - → 4 Salsa-s per FEB
  - → Only central detector FEBs visible
    - Peripheral FEBs in a row bellow
    - Or in a second row
- 32 1024-channel RDOs
  - → 4 FEBs per RDO
- Place for RDOs
  - → Electrical FEB-RDO interface : 5-6 m
    - Can probably be placed further away using driver-buffers but potential issues of ground loops and noise pickup
  - → Optical FEB-RDO interface : no limit
    - Targeted baseline option
- FEB – RDO mapping for other MPGDs yet to be defined



FEBs and Salsa-s for MPGDs

- Estimates for MPGDs assuming 256-channel FEBs

	CyMBaL		µRWell-BOT*		µRWell-ECT*	
	Tile	Sub-detector	Module	Sub-detector	DEE	Sub-detector
FEB	4	128	16	384	10	80
Salsa	16	512	64	1536	40	320
RDO	1	32	4	96	2.5	20

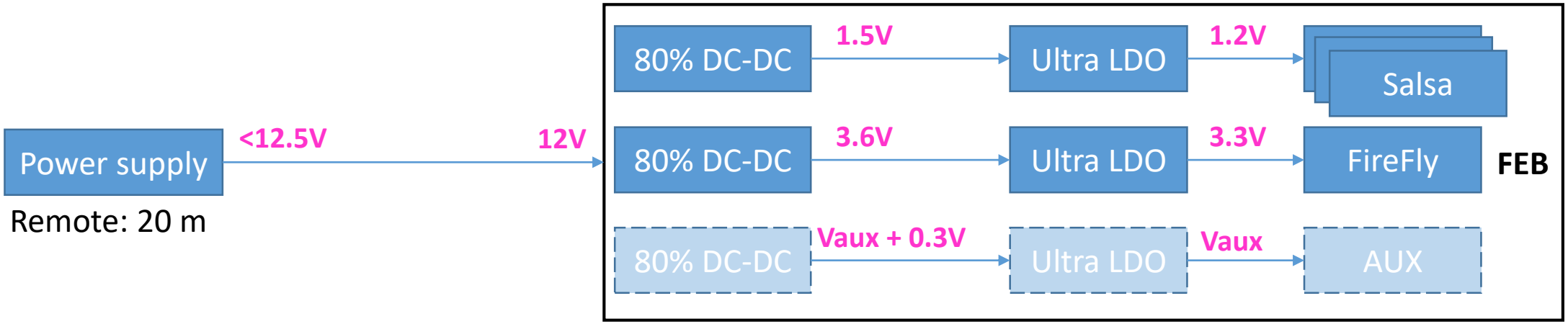
*FEB form factor and number of channels to be defined

- Total quantities including
  - → 750 FEBs including ~10% quality assurance quantities and test-bench needs
  - → 3 000 Salsa-s including prototyping needs
  - → 200 RDOs including ~10% quality assurance quantities and test-bench needs

- NB : FEB design requires better understanding of mechanical constraints

LV power distribution for MPGD frontends

- Based on magnetic field tolerant DC/DC converters
  - → Remote power supply distributes 12V with < 0.5V voltage drop over 20 m cables



- Powering 256-channel FEB with a bidirectional 4-lane FireFly optical interface
  - → 9 W per FEB
  - → 35 mW / channel
  - → LV wire cross-section : 1 mm^2

- NB : In absence of DC-DC converters, LDO-based power distribution will require 5.5 mm^2 wires
  - → Availability of small form factor magnetic field tolerant DC-DC converters is crucial

LV power distribution for MPGD frontends

- Estimates of MPGD sub-detector power needs assuming 256-channel FEBs

	CyMBaL		µRWell-BOT*		µRWell-ECT*	
	Tile	Sub-detector	Module	Sub-detector	DEE	Sub-detector
Power(W)	36	1.2k	144	3.5k	90	0.8k

*FEB form factor and number of channels to be defined

- Total of ~5.5 kW power

- NB : design of frontend power distribution and cooling requires better understanding of mechanical constraints
  → In coordination with other sub-detectors

Frontend data volume estimates for CyMBaL tracker

- Physics: zero suppression
  - → Case 1: Sampling readout
    - 500 ns readout window when signal is above threshold
      - 50 MSPS
      - 12-bits per sample, 50 MSPS, 25 samples
  - → Case 2: Peak-finding readout
    - 12-bit amplitude, 12-bit time of max, 8-bit ToT
- Calibration : on demand non ZS readout
  - → One of the Possible scenario
    - Calibration data requested every 100 Hz
    - 50 consecutive sample readout
    - 50 x 1000 samples per channel
- Data volume determined by physics
  - → Calibration can even be done regularly on-line
    - *e.g.* during the revolution gaps
- Still background generated data has to be taken into account
  - → Hens safety factor of 5

Estimated **physics** data bandwidth per Salsa ASIC

Channel rate kHz		Sampling Mbit/s	Amplitude - Time Mbit/s
2	(physics)	53	8.2
10	**(safety)**	**264**	**41**
50	(Clas12)	1 318	205

Estimated **calibration** data bandwidth per ASIC
~6 Mbit/s

Frontend data volume estimates

- CyMBaL :
  → Assuming 10 kHz hit rate per channel

	Sampling Gbit/s	Amplitude - Time Gbit/s
256-channel FEB	1.2	0.25
1024-channel RDO = 1 tile	5.0	1.0
Sub-detector	160	35

- MPGD sub-detectors
  → Accurate estimates still to be done
  → Crude summary

	CyMBaL		µRWell-BOT		µRWell-ECT	
	Sampling	Amp-Time	Sampling	Amp-Time	Sampling	Amp-Time
Data (Gbit/s)	160	35	500	100	100	20

- NB: these are frontend data estimates, not the data to tape

Design and production strategy

- Salsa will be produced and tested in quantities that will cover the needs of all ePIC MPGDs

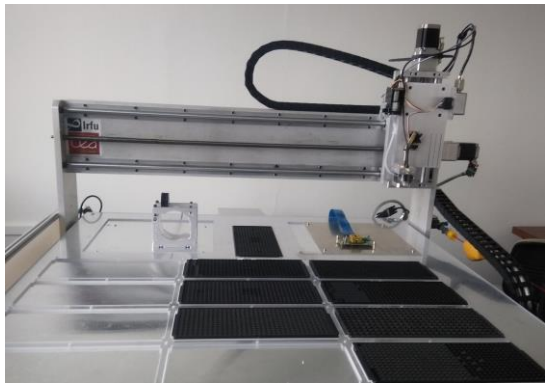
- The FEB design will be shared with all MPGD groups
  - → Including detector interface studies
    - Connectors, micro-coaxial cables
- Feb design adaptation for particular geometry will be under sub-detector responsibility
- Common effort to adapt FEB-RDO-DAM interface, RDO and DAM fw / sw
  - → Adaptation of RDO hardware may need per sub-group efforts
- Common effort on services
  - → LV and HV distribution, interlock, slow control and cooling
  - → Common concern of several sub-detector systems in magnetic field

- FEB production and qualification tests will be shared between several sites
  - → Required quantities exclude single site responsibility
    - Especially in case of different form factor boards

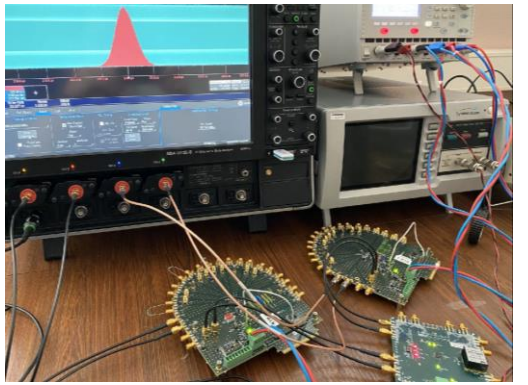
- RDO production responsibility to be understood

Quality Assurance

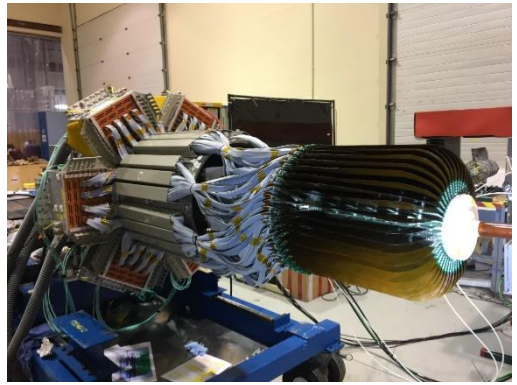
- Expertise in large scale production of ASICs and frontend boards
  - → In-house : automated ASIC tester robots and FE production test benches
  - → In industry : providing turn-key test benches
  - → Ex: Rafael (40 000) and Catia (80 000) ASICs for CMS Ph2 upgrade
  - → Ex: Alice Solar (700), Clas12 FEU (150)



- Rich set of equipment
  - → High-end LeCroy and Tectronix oscilloscopes
  - → High performance phase noise analyzer
  - → Low jitter clock sources
  - → Climate chamber
  - → Bonding machines



- Expertise in system-level validation
  - → Detector – readout electronics – acquisition software – analysis
    - Clas12 MVT, T2K TPCs, Asacusa tracker, …



- Expertise in radiation hard ASIC design and validation techniques
  - → Access to CERN, French and European facilities
- Access to high magnetic field facilities
  - → At CERN and at Saclay

Planning

- Salsa
  - → 2024 : Salsa1
    - Several fully instrumented channels including analog very fronted and 12-bit MSPS ADC
    - Clock management circuitry based on Prisme IP
  - → 2025 : Salsa2
    - A 32-channel prototype with main DSP functionalities and serial link interfaces targeting final packaging
    - Prototyping of unified backend interface based on a serial link
  - → 2026 : Salsa pre-series
    - A 64-channel fully functional prototype
  - → 2027 : Mass production

- FEB
  - → 2024-2025 : small prototype developments
    - Assessment of COTS components – *e.g.* power and monitoring solutions for radiation and magnetic field environment
    - R&D on detector – FEB interface connectors
    - FEB form factor and Salsa integration studies for different MPGDs
    - Validation of unified interface with ASICs
  - → 2026 : advanced prototype development
    - Based on Salsa2
  - → 2027 : Pre-series production
    - Based on pre-series Salsa
  - → 2028 : Mass production

Planning

- RDO
  - → 2024 – 2025 : FEB – RDO interface specification and validation, plus adaptation hardware design
  - → 2026 : FEB-RDO communication validation based on Salsa2 prototype systems
  - → 2027 : RDO production if attributed to sub-groups
- Services
  - → 2024 : Identify clearly keep-in-out zones
  - → 2025 : Validate LV distribution & come out with cooling scheme, plus interlocks
    - Profit from rich expertise within the ePIC groups on magnetic field tolerant DC/DC regulators
  - → 2026-2027 : production
- Detector R&D
  - → Detector R&D will require readout during 2024-2025
    - Large scale Salsa-based electronics will not be available until 2027
      - Though there will be some access to Salsa2 (32-channel) and Salsa pre-series systems
    - Irfu, CEA Saclay poses Dream-based electronics in quantities to satisfy its needs for local cosmic tests and beam tests
    - To be understood for other groups
- System
  - → 2027 : Fully instrumented slice for every group
    - including FEB prototypes, at least two RDOs and a DAM
  - → 2028 : Full system chain validation
    - Including slow control and monitoring

Risk mitigation

- Risks are related to unexpected Salsa behavior or performances issues
  - → Diagnostic-correction-production-validation cycle may require 1 year
    - Though can be faster if a single mask needs to be changed
- To be continued…

Summary

- Envisaged solutions for the ePIC MPGD readout are viable and cover performance requirements
- Engaged groups have necessary experience for large scale system design, production and commissioning
- R&Ds are on-going
  - → Detector – FEB connectivity
  - → Integrated ASIC interface
  - → COTS components validation for ePIC environment
- Design on Salsa ASIC follows its uncompressible phases

- Collaboration-wide efforts are needed
  - → Precise identification of keep-in-out zones between the sub-detectors
  - → Efficient low form factor magnetic-field tolerant powering means
  - → Precise identification of run-control state machine and set of rules that detector partitions need to obey
  - → Error detector and recovery strategy

- At least one more FEB (design-)production site needs to be identified
  - → In addition to Irfu, CEA Saclay

- Planning is stringent

Some references

- Salsa - https://indico.bnl.gov/event/22053/contributions/86152/attachments/52272/89395/SALSA_EPIC_electronics_DAQ_20240125.pdf
- MPGD LV - https://indico.bnl.gov/event/22316/contributions/87363/attachments/52727/90159/240215_IM_MpgdPower.pdf
- Signal - https://indico.bnl.gov/event/20965/contributions/82420/attachments/50649/86604/231026_IM_CyMBal_ExpectedSignal.pdf
- Calibration – https://indico.bnl.gov/event/16040/contributions/64090/attachments/41290/69185/220520_MpgdTrack_CalibRates_IM.pdf
- Data collection - https://indico.bnl.gov/event/18118/contributions/72179/attachments/45781/77366/221221_MpgdDataCol_IM.pdf
- FEB options - https://indico.bnl.gov/event/21104/contributions/83856/attachments/51197/87574/231127_IM_Mpgd_VtrxPlus.pdf

Backup