# eRD109 COTS Waveform Readout FEB – update Mar. 7 2024

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### Progress 2/1 – 3/6

- Further prototyping and evaluation of LTC3600 DC/DC circuit
- Discussion of DC/DC issues in Electronics/DAQ meeting
- Investigation of dynamic range issues & discussion in calorimetry meeting



- Meeting minimum signal readout requirements, e.g., 15 MeV, will be very difficult after radiation damage
- Designed a "dynamic range compressor" circuit & built prototype PCB, test in March
  - This is not in baseline plan for FEB but only a backup plan if needed...
- Reviewed available **floating** mezzanine connectors and made final selection for SiPM FEB interface
- Changes agreed to mechanical interface FEB SiPM boards and lightguide block
- Input given on power services planning (T. Camarda spreadsheet)
- Detailed design on signal path from SiPM to ADC pins, schematic 95% complete layout 40%
  - THS4551 prototyped on eval board and selected for ADC driver
- Some work (including discussion with vendors) on FEB PCB parameters (layer stack, via in pad details)
- FEB PCB design starting (see next slide)





8 x 4 channels (covering two 4 x 4 tower blocks, 8 SiPM boards (16 SiPM each)) Top layout view faces the SiPM boards & cooling tube, Two identical bias regulator mezzanine boards mounted on rear.

#### • Specifications/requirements documented

- Seems like close to finalizing rate requirements!
- FEB-detector integration: basically all finalized at this point
- Key parts procured: ADC, FPGA, DC/DC, preamp
  - Including more FPGA dedicated to bwd ECAL application
- Learning PolarFire FPGA details; *need to pick this up again...*
- Ready to design SiPM carrier / LED pulser board
- Lightguide improvements (→ Required for FEB mechanical, and possible light yield improvements are of the greatest importance for readout – min signal size challenge!)
- LTC3600 DC/DC circuits with air-core inductor low noise proto needed
- SiPM frontend prototyped / improved from STAR FCS → real FEB layout in progress
- Working to define FEB-RDO interface
  - Expect to make simple FMC board to interface to ppRDO (Tonko)
- Next steps / in-progress
  - Two channel signal path prototype to fit to PolarFire eval board
  - SiPM board layout & produce prototypes
  - FEB Main Board layout & produce prototypes
  - Considerations for application to bwd ECAL
- Other to-do:
  - Radiation testing
  - ePIC discussions on DC/DC, services, and SiPM bias schemes



PolarFire Eval Board – nice/simple/\$200

I've deviated somewhat from the sequence of milestones in contract. Trying to do always what is best to push forward the design.

So far have not really tackled comparisons to HGCROC nor waveform ASIC possibilities. These will be done, but I think the first emphasis has to be on design.

On the other hand, have put early effort into possible application to bwd ECAL.

### eRD109 status/plans

backup slides

#### **Block diagram**

#### COTS ADC + FPGA, or equiv. ASIC





ground for FEB (important for noise/EMI and safety)

2-block (32 tower) FEB





tungsten/scifi

block

(forced) air cooling option now

prototype FEB mounting standoff

all cables and water tubing route basically only horizontally on detector



(slide from Rahul & Oleg)

## **fEMCal Integration**



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