ALCOR - dRICH Readout

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INFN Torino

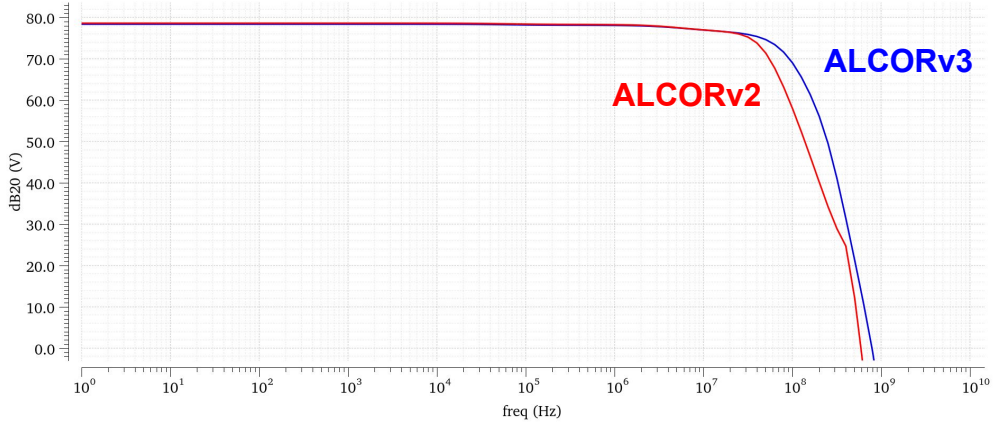
EPIC Electronics & DAQ WG meeting
eRD109 Monthly Progress Reports

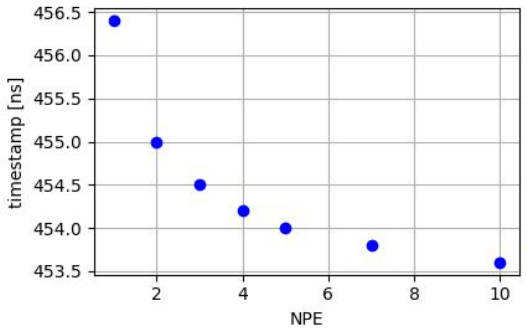
07.03.2024

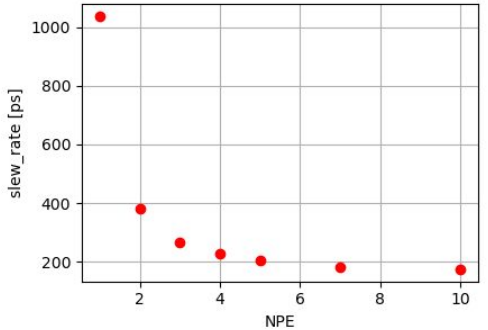
ALCOR v3 design

Small revisions on **ALCOR FE** design

- Increased amplifier bandwidth
- Hysteresis discriminator
- Studies on **time walk** correction
  - ***ToT** mode* already tested (Oct 2023 beam test) → ok, but not perfect due to *afterpulse* and *crosstalk* effects
  - ***Slew Rate** mode* also available in ALCOR v2 → to be tested in the next months (simulations, laser tests, beam test)



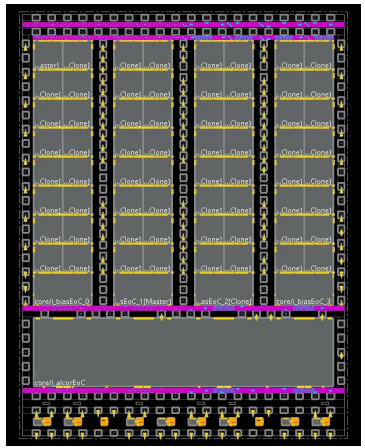




ALCOR v3 design

Digital logic new features and bug fixes

- **Digital shutter** for data reduction (EIC bunch crossing: 10 ns → 1-2 ns time window)
  - pixel-level implementation completed
  - 4-bit programmable delay (~200 ps step) to compensate pixel-by-pixel offsets
- New pixel implemented at **394.08 MHz** clock frequency (4 x 98.52 MHz)
- Identified and fixed **reset glitch** occurring on ALCORv2 (at low temperatures)



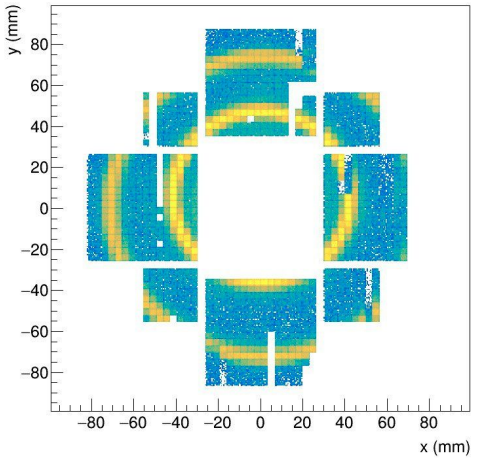
ASIC floorplan and **BGA packaging**

- Defined pads layout, assignment and coordinates for flip-chip bump-bonding
- Advanced discussions with BGA package and interposer designers

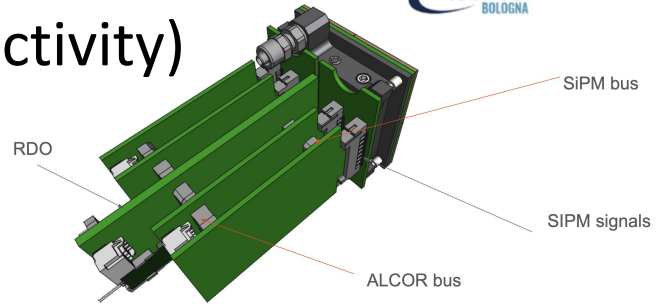
ALCOR v2.1 characterization

- INFN internal engineering run with small bug fixes w.r.t. ALCOR v2
- Diced chips received on Jan 29th 2024
  - High number of chips available
  - Will be used to extend setups used for 2024 activities
- First results confirm TDC bugs have been fixed
  - TFine (TDC output) *vs* clock ambiguity
  - ToT spurious data at very low rates
- Started tests for the validation of 20 new ALCOR FE DUAL boards (1280 channels) for Spring 2024 beam test to increase our SiPM active area

Oct 2023 beam test (R. Preghenella)



Update on dRICH RDO design (February activity)

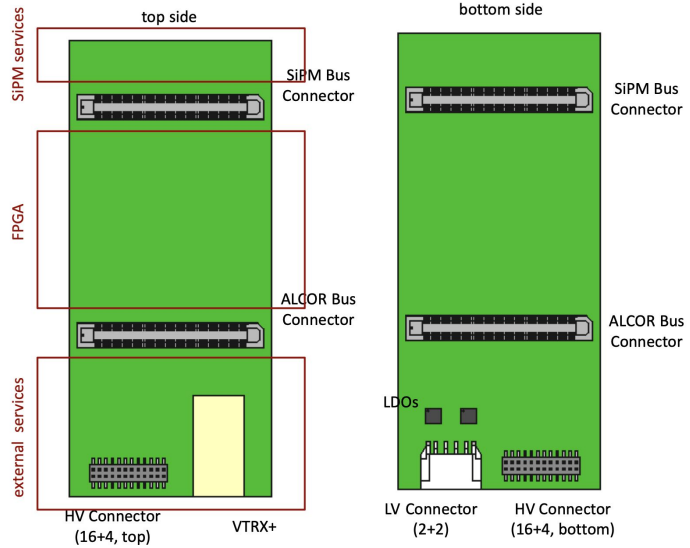


- challenging constraints on dimensions for dRICH (4x9 cm)
- design for schematics/selection of components **in progress**
- KC705 firmware “ported” to AUP15 FPGA for ALCOR readout
- **ordered 10 AU15P** (lead time 16 weeks!)

Current components candidates:

- Main FPGA: Xilinx AU15P-SBVB484
- Opt. tranc. VTRx+
- Scrubber FPGA: Microchip MPF050T-FCS9325
- QSPI Flash
- Samtec connectors (ALCORbus and SIPMbus): ERM5-050/020-XX
- Clock multiplier/jitter cleaner: SkyWorks SI5326
- T sensor: AD7416AR3 (close to LDOs and VTRX+)
- 1 MCU: see next slides
- LDOs and current monitor: see next slides
- I2C I/O expander TBC

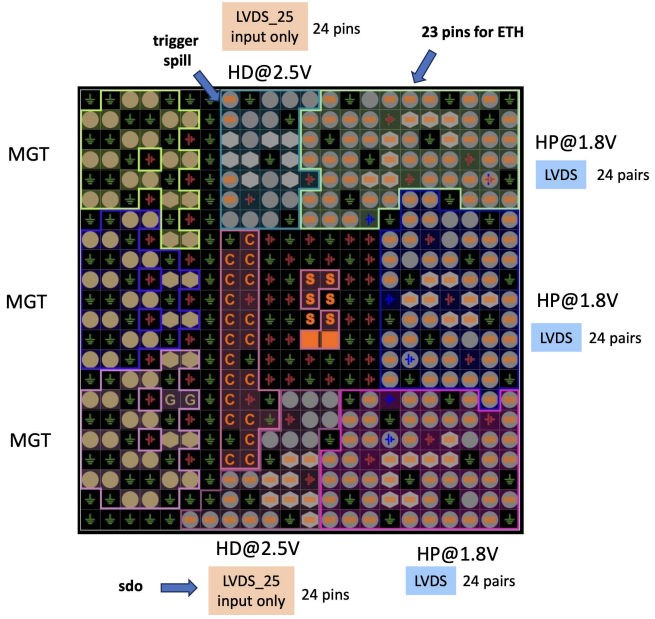
PolarFire scrubber implementation is next step



Submitted application to TIFPA PAC for access to proton in Trento for irradiation of components in July and December (ALCOR and FPGA)

- pin-plan study for Xilinx AU15P-SBVB484
- support connections for 4 ALCOR-64 (4 FEB)
- pins matched with KC705 use
- we kept pins for ETH (currently using IPBUS) they will be available
- found and implemented 24 LVDS pairs over banks to match with all FEB (ALCOR bus)

- timing closure at 320 MHz and 400 MHz
- power consumption estimates



@ 320 MHz

Power Supply

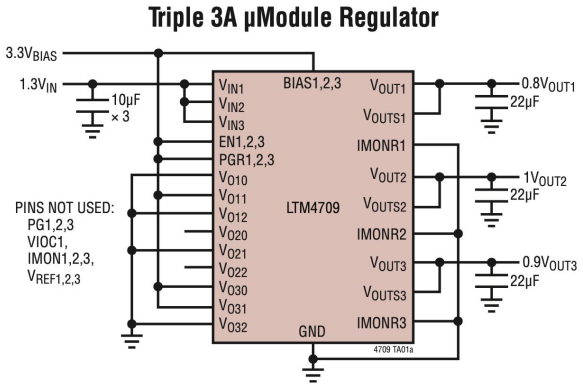
Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)	Budget (A)	Margin (A)
Vccint	0.850	1.031	0.973	0.058	Unspecified	NA
Vccint_io	0.850	0.095	0.068	0.027	Unspecified	NA
Vccbram	0.850	0.083	0.082	0.001	Unspecified	NA
Vccaux	1.800	0.114	0.050	0.064	Unspecified	NA
Vccaux_io	1.800	0.058	0.034	0.023	Unspecified	NA
Vcco33	3.300	0.000	0.000	0.000	Unspecified	NA
Vcco25	2.500	0.005	0.000	0.005	Unspecified	NA
Vcco18	1.800	0.181	0.181	0.000	Unspecified	NA
Vcco15	1.500	0.000	0.000	0.000	Unspecified	NA
Vcco135	1.350	0.000	0.000	0.000	Unspecified	NA
Vcco12	1.200	0.000	0.000	0.000	Unspecified	NA
Vcco10	1.000	0.000	0.000	0.000	Unspecified	NA
Vccadc	1.800	0.008	0.000	0.008	Unspecified	NA
MGTAVcc	0.900	0.000	0.000	0.000	Unspecified	NA
MGTAVtt	1.200	0.000	0.000	0.000	Unspecified	NA
MGTVccaux	1.800	0.000	0.000	0.000	Unspecified	NA

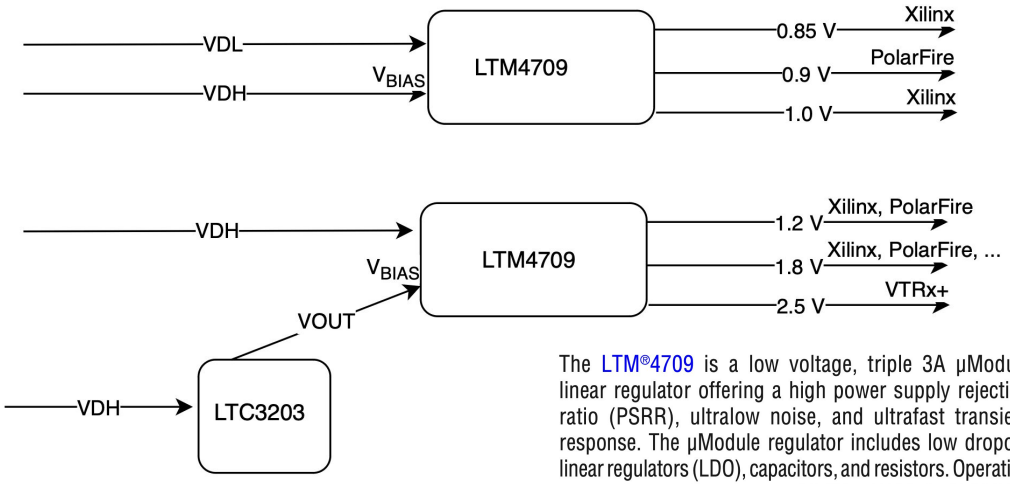
@ 400 MHz

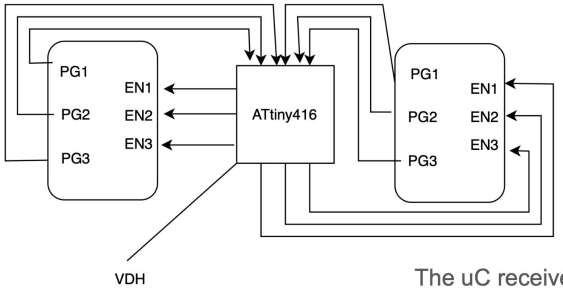
Power Supply

Supply Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)	Budget (A)	Margin (A)
Vccint	0.850	1.257	1.197	0.059	Unspecified	NA
Vccint_io	0.850	0.096	0.069	0.027	Unspecified	NA
Vccbram	0.850	0.103	0.102	0.001	Unspecified	NA
Vccaux	1.800	0.127	0.064	0.064	Unspecified	NA
Vccaux_io	1.800	0.058	0.034	0.023	Unspecified	NA
Vcco33	3.300	0.000	0.000	0.000	Unspecified	NA
Vcco25	2.500	0.005	0.000	0.005	Unspecified	NA
Vcco18	1.800	0.181	0.181	0.000	Unspecified	NA
Vcco15	1.500	0.000	0.000	0.000	Unspecified	NA
Vcco135	1.350	0.000	0.000	0.000	Unspecified	NA
Vcco12	1.200	0.000	0.000	0.000	Unspecified	NA
Vcco10	1.000	0.000	0.000	0.000	Unspecified	NA
Vccadc	1.800	0.008	0.000	0.008	Unspecified	NA
MGTAVcc	0.900	0.000	0.000	0.000	Unspecified	NA
MGTAVtt	1.200	0.000	0.000	0.000	Unspecified	NA
MGTVccaux	1.800	0.000	0.000	0.000	Unspecified	NA

MGTs not yet used in this test FW…







The uC receives the current monitors from the two LDOs and protect against SEL

- recent LDO useful for FPGA core
- optimization with **VDH=2.7 V** and **VDL=1.4 V**
- LTM4709 datasheet
- LTC3203 is a step-up charge pump (V_{OUT}=3.7V)

The LTM®4709 is a low voltage, triple 3A µModule linear regulator offering a high power supply rejection ratio (PSRR), ultralow noise, and ultrafast transient response. The µModule regulator includes low dropout linear regulators (LDO), capacitors, and resistors. Operating over an input voltage range of 0.6V to 5.5V, the LTM4709 supports an output voltage range of 0.5V to 4.2V for triple 3A channels with a typical dropout voltage of 45mV. The output voltage is digitally configurable in 50mV increments from 0.5V to 1.2V; 100mV increments from 1.2V to 1.8V; and discrete levels at 2V, 2.5V, 3V, 3.3V, and 4.2V. A precision current monitor provides accurate current monitoring for the energy management system and current limit. The LTM4709 is ideal for RF communication, noise-sensitive instrumentation, post-regulation for switching regulators, high-performance FPGAs, and microprocessors. Only input, output, and bias ceramic capacitors are needed for its application.

ATtiny416:
Product Selection Guide
Datasheet

Power consumption estimates for PDU (4 FEB + 1 RDO)

PRELIMINARY

	chip	LDO	Vin (V)	Vout (V)	Iout (A)	Vdrop (V)	Ptotal (W)	Pdevice (W)	Ploss (W)
ALCOR analog	0	ADP1761	1.4	1.20	0.556	0.20	0.778	0.667	0.111
	1	ADP1761	1.4	1.20	0.556	0.20	0.778	0.667	0.111
	2	ADP1761	1.4	1.20	0.556	0.20	0.778	0.667	0.111
	3	ADP1761	1.4	1.20	0.556	0.20	0.778	0.667	0.111
ALCOR digital	0	ADP1761	1.4	1.20	0.188	0.20	0.263	0.225	0.038
		APD1752	2.7	2.50	0.085	0.20	0.230	0.213	0.017
	1	ADP1761	1.4	1.20	0.188	0.20	0.263	0.225	0.038
		APD1752	2.7	2.50	0.085	0.20	0.230	0.213	0.017
	2	ADP1761	1.4	1.20	0.188	0.20	0.263	0.225	0.038
		APD1752	2.7	2.50	0.085	0.20	0.230	0.213	0.017
	3	ADP1761	1.4	1.20	0.188	0.20	0.263	0.225	0.038
		APD1752	2.7	2.50	0.085	0.20	0.230	0.213	0.017
ARTIX		LTM4709-1L	1.4	0.85	1.455	0.55	2.037	1.237	0.800
		LTM4709-2L	1.4	0.90	0.101	0.50	0.141	0.091	0.051
		LTM4709-1H	2.7	1.20	0.129	1.50	0.348	0.155	0.194
		LTM4709-2H	2.7	1.80	0.400	0.90	1.080	0.720	0.360
		LTM4709-3H	2.7	2.50	0.050	0.20	0.135	0.125	0.010
POLARFIRE		LTM4709-3L	1.4	1.00					
		LTM4709-2H	2.7	1.80					
VTRX+		LTM4709-1H	2.7	1.20	0.015	1.50	0.041	0.018	0.023
		LTM4709-3H	2.7	2.50	0.040	0.20	0.108	0.100	0.008
			2.7	2.50	0.015	0.20	0.041	0.038	0.003
MT25QU01		LTM4709-2H	2.7	1.80	0.055	0.90	0.149	0.099	0.050
ATtiny416		N/A							
TOTAL							9.16	7.00	2.16

FEB

RDO

Modelling of FPGA consumption + ALCOR

Still to be inserted: PolarFire!

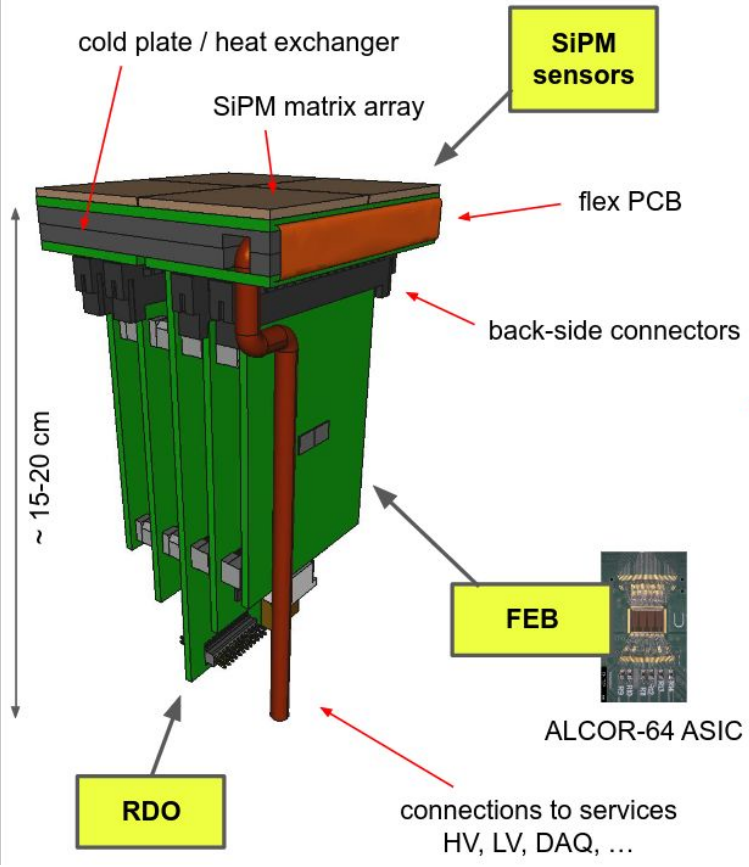
Plans for 2024

- Complete design of **ALCOR v3**: ASIC tape-out (Sep 2024) + package design (Fall 2024)
- Design of **RDO prototype,** as close as possible to final (Jun 2024)
- **RDO readout** using current ALCOR FE-DUAL board (Fall 2024)
- Preparation for Spring 2024 **beam test**
- **Irradiation tests** campaign (SEU and TID) at Centro of Proton-Therapy in Trento: ALCOR v2-v2.1 (Jul 2024) and RDO (Dec 2024)

Spare slides

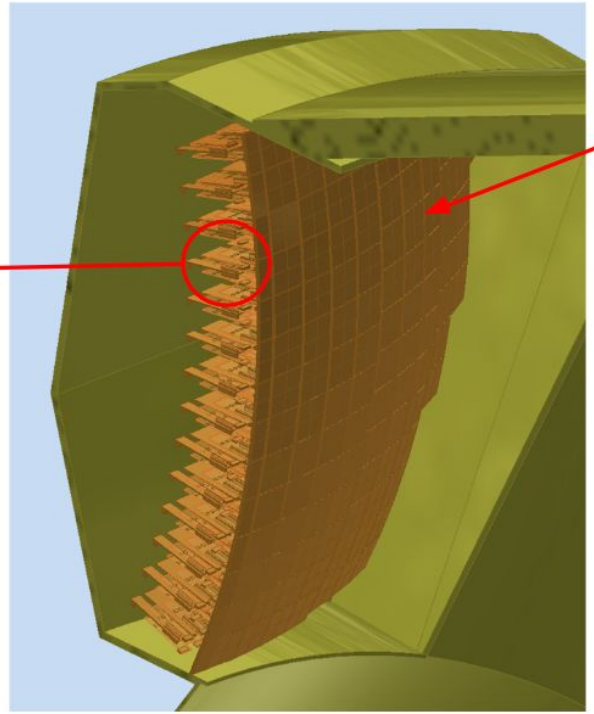
Photodetector unit

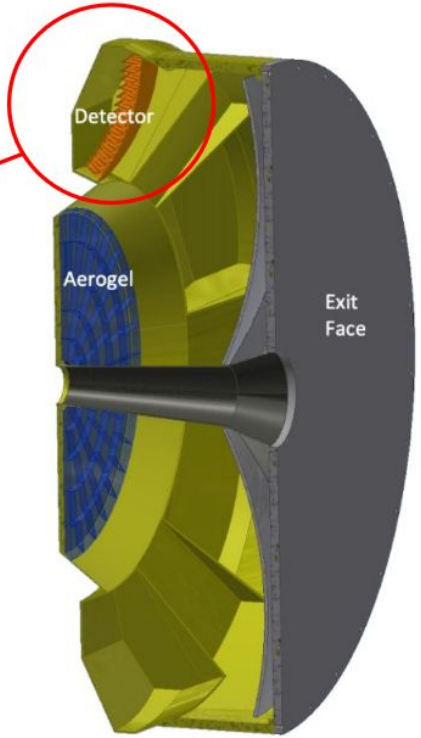
conceptual design of final layout



SiPM sensor matrices mounted on carrier PCB board

- 4x 64-channel SiPM array device (256 channels) for each unit
- 1248 photodetector units for full dRICH readout
  - 4992 SiPM matrix arrays (8x8)
  - 4992 ALCOR-64 chips
  - 319488 readout channels

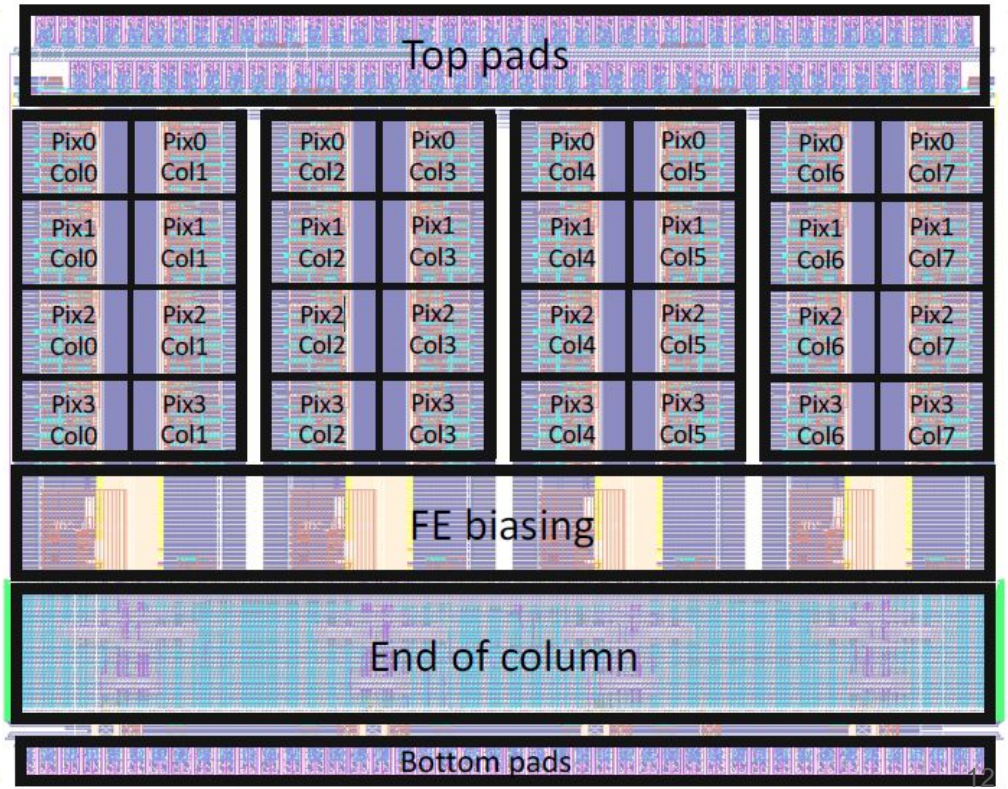




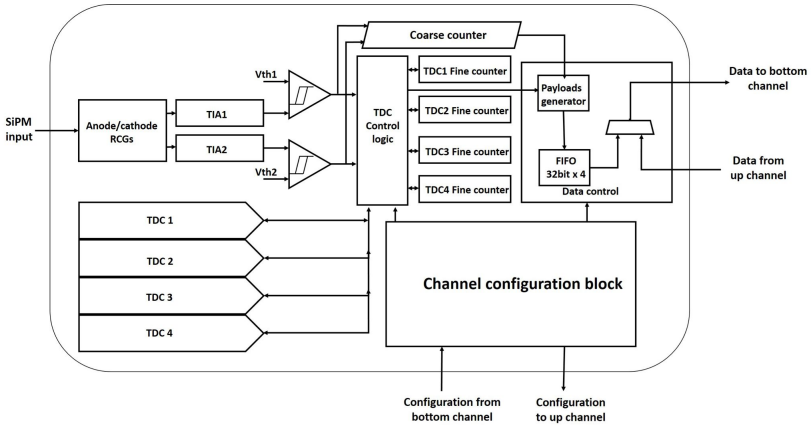
ALCOR (**A** **L**ow Power **C**hip for **O**ptical Sensor **R**eadout)

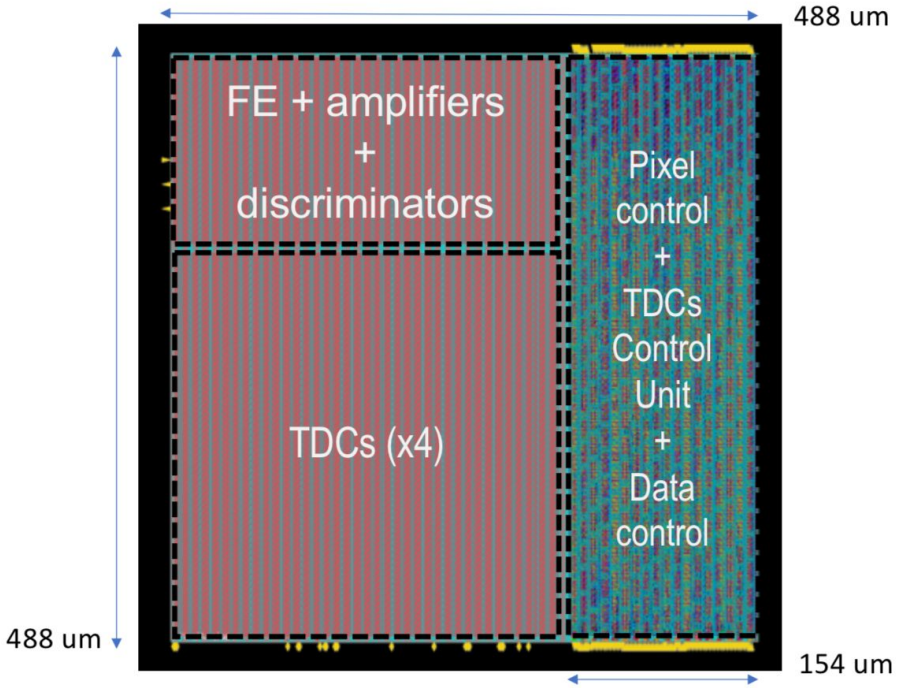
ASIC developed for the readout of the EIC dRICH SiPM sensors

- **32-pixel** matrix (8x4) mixed-signal ASIC
- **SiPM readout**: single-photon time tagging + Time-over-Threshold measurement
- 32-bit (64-bit in ToT mode) event word generated on-pixel and propagated down the column
- **Fully digital output**: 4 LVDS 320 MHz DDR Tx links



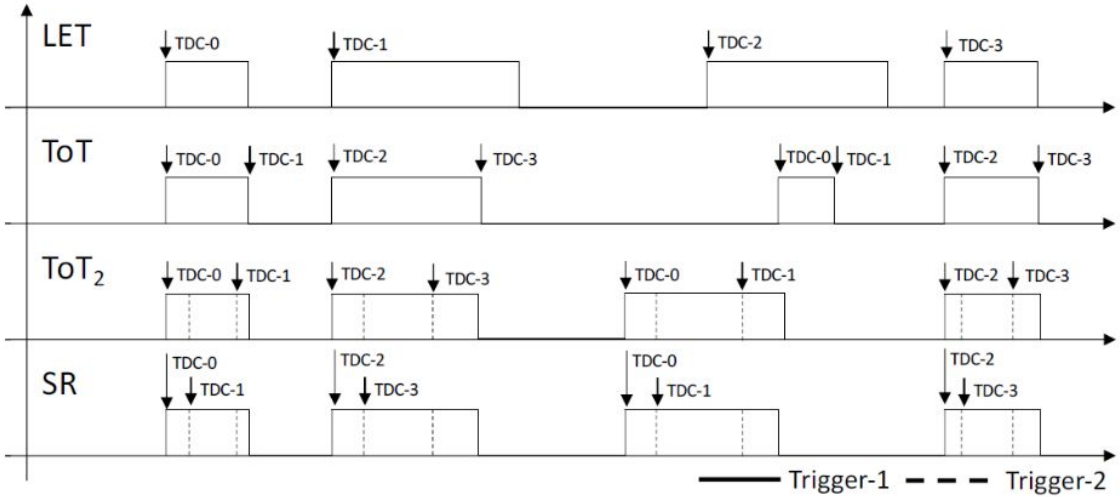
Pixel architecture





- **TIA amplifier** with RCG input stage
- 2 independent post-amp branches with 4 gain settings
- 2 **leading edge discriminators** with independent (and per pixel) threshold settings (6-bit DAC)
- 4 **TDCs** based on **analogue interpolation** with 25-50 ps time-bin (at 320 MHz clock frequency)
- Pixel control logic handles TDC operation, pixel configuration and data transmission

ALCOR pixel operating modes



4 operating modes:

- LET: leading edge measurement
- ToT: Time-over-Threshold measurement using the first discriminator for both edges
- ToT2: Time-over-Threshold measurement using both discriminators
- SR: slew-rate measurement

Each mode can be set to:

- FE: normal operation mode
- FE_TP: send test-pulse to analogue front-end
- TDC_TP: send test-pulse to pixel control logic to test and calibrate TDCs (bypass front-end)

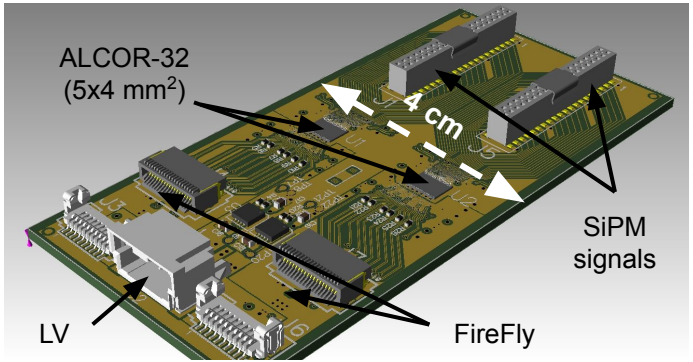
Each pixel can also be disabled

ALCOR v3 FEB

Start design of the EPIC dRICH Front-End Board (FEB), hosting the ALCOR v3 chip inside the BGA package

- Two ALCOR v2 (32 channels) replaced by one ALCOR v3 (64 channels)
- Firefly connectors replaced by connectors towards RDO board
- Add annealing Mosfets (currently mounted on adapter board)

ALCOR-FE-DUAL (2023-24 version)



Photodetector unit
(conceptual design
of final layout)