EICROC and CALOROC status and plans

eRD109 monthly report 7 mar 2024

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Organization for Micro-Electronics desiGn and Applications

EICROC0 : update from last month [S. Conforti, A. Verplanck et al.]

- Firmware update (old version @ Omega)
  - New version implemented ✓
  - Scripts corrected to work with new firmware ✓
- Code development for new firmware
  - Config files, test scripts, data processing scripts ✓
  - Code that allows to plot S-Curves, TDC, ADC, Hit automatically
  - Uploaded on GitLab
- Documentation write-up (updated over time)
  - User guide ✓
  - Code guide ✓
  - Datasheet
  - Uploaded on GitLab
- Tests on ASIC with new firmware and scripts
  - S-Curves ✓

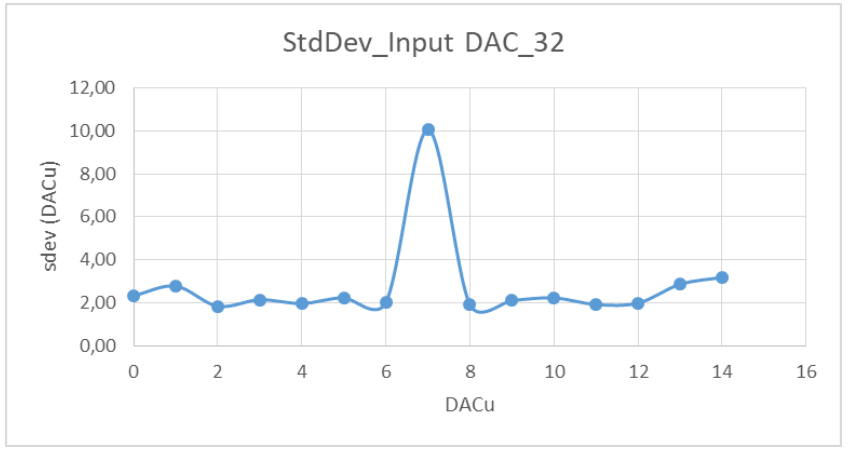
Ex : S-curves on 16 channels with threshold trimming

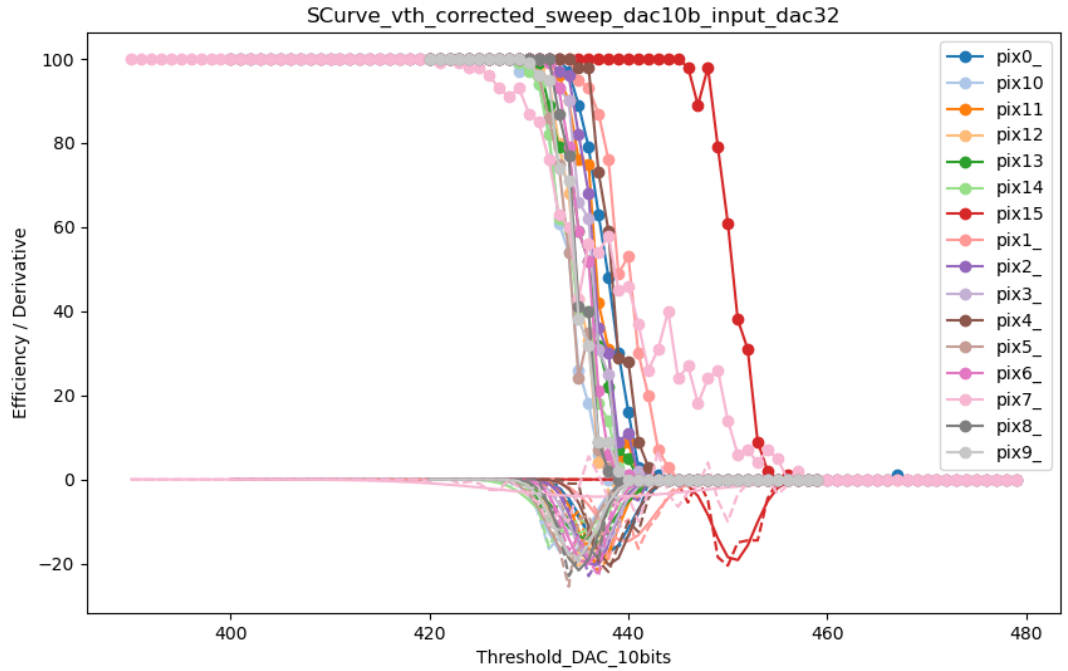
Input DAC_pulse 32: ~ 14 fC

Vth_correction fixed for each channel at the measured value

0,11 fC / DACu

Input DAC_32_vth_corrected_chbych		
	50% trigger efficiency	StdDev
Mean	437,1840275	2,778044388
min	433,8969726	1,848503507
max	450,6570696	10,04795084
delta	16,76	





EICROC Project: update [D. Marchand, L. Serin]

- **Studies of Probe PA jitter: on-going (BNL, Hiroshima Univ., IJCLab)**
- **Scrutinizing Discriminator Efficiency: Threshold Scan (varying charge injected): on-going (OMEGA, BNL, IJCLab)**
- **Scrutinizing TDC data shifting External Trigger for all 16 channels: on-going (IJCLab)**
- **EICROC0 chips**
  - Feb. 20th, 2024: **24 EICROC0** ASICs were delivered to BNL in view of hybridation (EICROC0+AC-LGAD)
- ~~**20**~~ **10** pieces **Updated EICROC0 PCBs (test boards) and Related topics**
  - Cabling is being performed at IJCLab: **finalized March 6th, 2024**
    [omitting crossing components to allow for the wire-bonding]
  - **3 PCBs** will be sent **shortly** to IPHC (Strasbourg, France) to wire-bond an EICROC0
    We propose to first test this configuration (board operational)
    * before wire-bonding EICROC0 & AC-LGAD
    * ordering 10 more PCBs
  - 3 PCBs will be sent **shortly** to BNL with associated crossing components
  - **Some AC-LGAD sensors** (from BNL) will be transferred to CERN **next week** to be given to IJCLab

[*2 PCBs are intended to be sent later on to IPHC (Strasbourg, France) to wire-bond an EICROC0 + AC-LGAD*]
(AC-LGAD sensors provided by BNL)
[*2 PCBs will wait for hybrids from BNL. They will be sent to IPHC (Strasbourg, France) for wire-bonding*]

EICROC Project: Update & Perspectives [1/2]

- Recurrent EICROC periodic meetings (every 2 weeks):
  Hiroshima University, BNL, IJCLab, OMEGA, CEA/Irfu/DEDIP **Update Reports**
  Gathering 12 persons (in average) involved in EICROC0 characterization
  https://indico.ijclab.in2p3.fr/category/538/

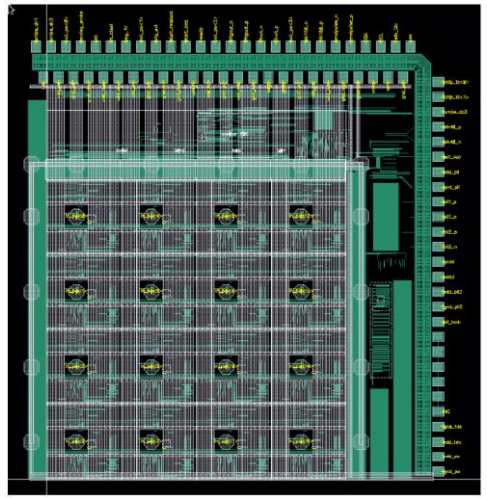
- Perspectives for ramping up on EICROC0 testing:
  - ➞ Exploiting EICROC0 analogical Probe PA output signals & digital outputs:
    - * **Laser test bench** (at BNL) requires synchronisation capabilities,
    - * **Beta source** (IJCLab & BNL) requires triggerless acquisition
    - * Strongly considering to take part **to the DESY test beam next June**
      (wire- & bump- bonded AC-LGAD & EICROC0 – Updated PCBs)
      Involvement of **BNL**, **IJCLab** and **OMEGA** teams

Status of EICROC

- EICROC0 is a testbeam prototype => sensor characterization
  - Triggered readout, all data shipped out : 16 ch * 8 samples ADC + TDC
  - Present power ~2 mW/ch + 4*20 mW « analog probe preamp »
  - Status : measurements in progress
  - ADC power + shaper/driver to be reduced from ~1 mW to 100 µW/ch => EICROC0A
  - EICROC0A : simulations in progress

- EICROC1 will address larger dimensions 4x16 or 8x16 or 4x32 or 8x32
  - Address floor planning and power distribution
  - Selective readout : hit + 9 neighbouring channels
  - Status : layout started based on EICROC0, adding more testability
  - Still EICROC0-like readout

- EICROC2 final size : 32x32



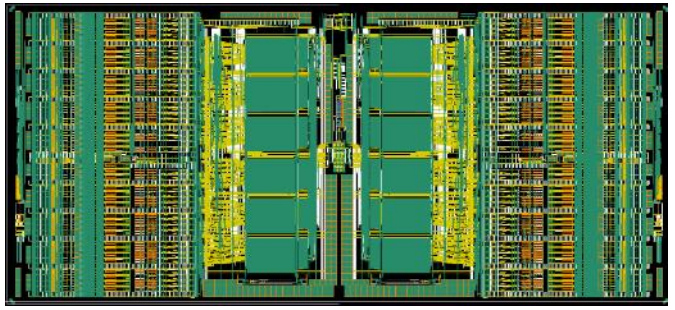
CALOROC1 [F. Dulucq, P. Dumas, C. Munoz, M. Nguyen, D. Thienpont et al.]

- SiPM readout calorimetry : CMS H2GCROC with EIC readout (200 MHz clock and fast commands)
  - SiPM from 500 pF to 2.5 nF (or 10 nF)
  - ~5-10 mW/channel

- 2 versions : conservative and exploratory
  - CALOROC1A : Conservative : uses H2GCROC (ADC, TOT) as it is and replaces the backend
  - Status : analog part complete, digital in progress
  - CALOROC1B : Exploratory : new analog part (dynamic gain switching).
  - Pin to pin compatible
  - Backend « à la HKROC » : auto-triggered, zero-suppressed
  - 40 MHz internal clocking (ADC, TDCs)
  - Status : simulations in progress

HKROC

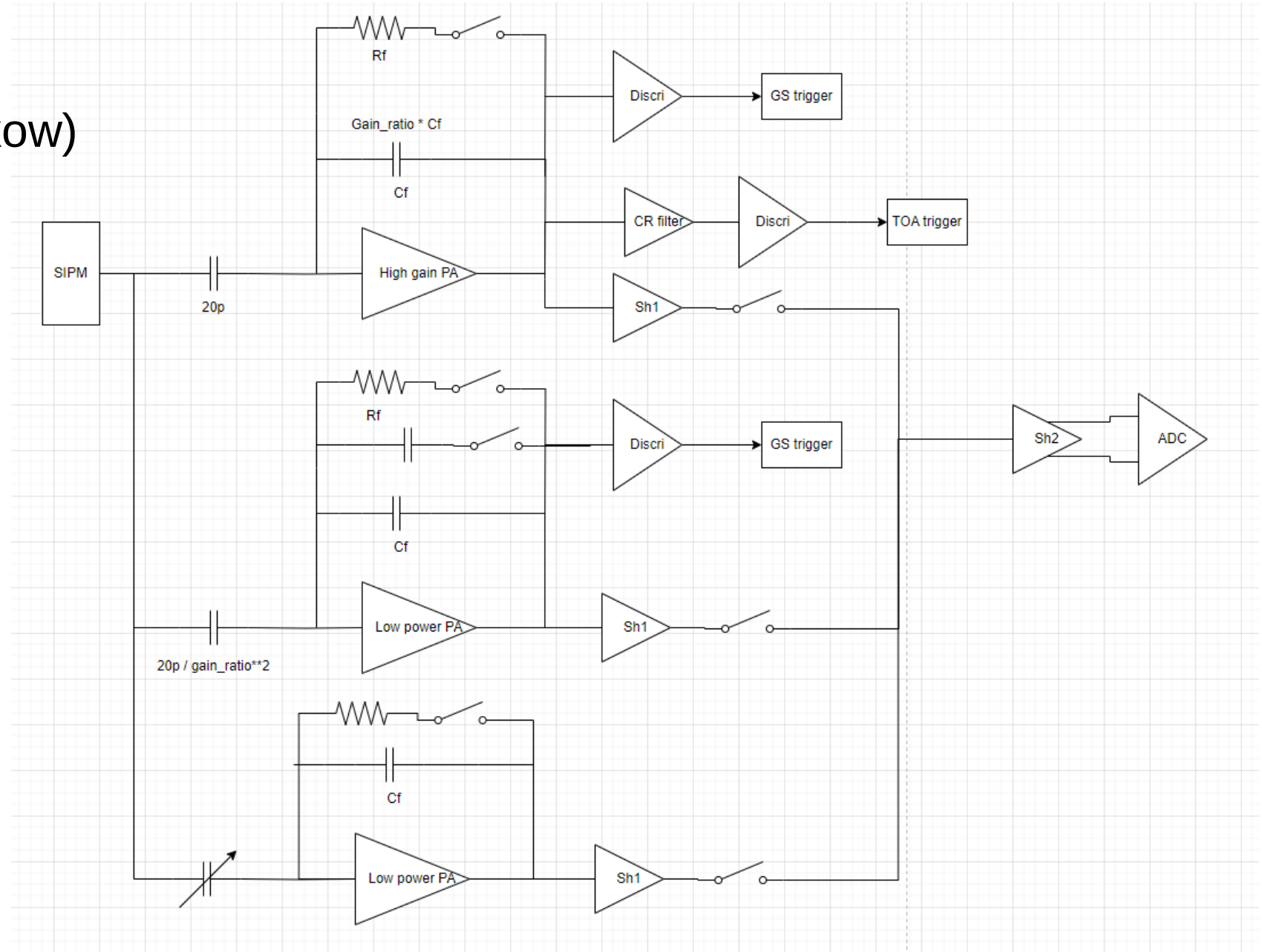
- Channel number tbd : 32 (HKROC) or 64 (HGCROC)
  - Cost issue and pin/pin compatibility with prototypes



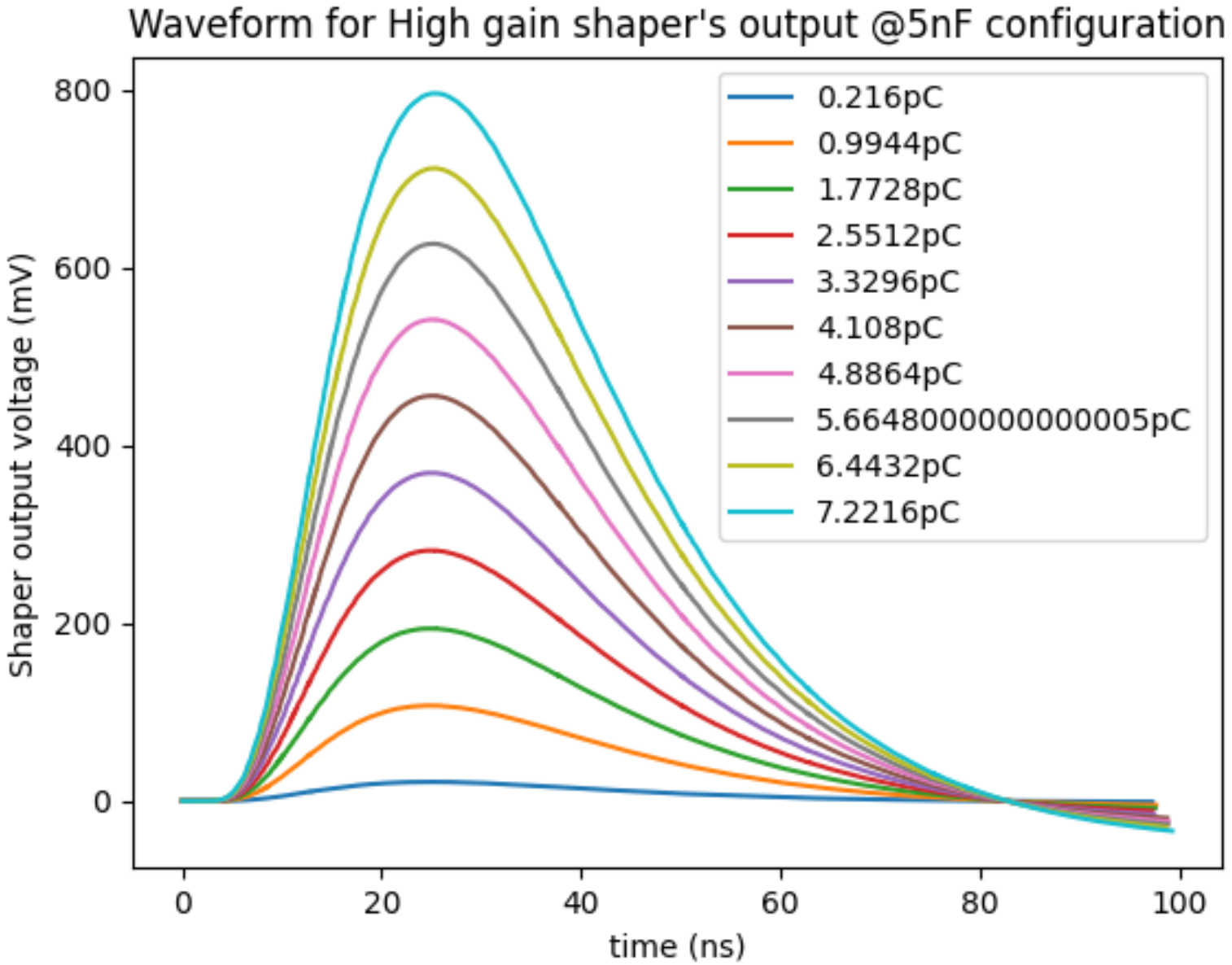
- « Si » version considered for HRPPD and/or strips

CALOROC1B : studied architecture [P. Dumas]

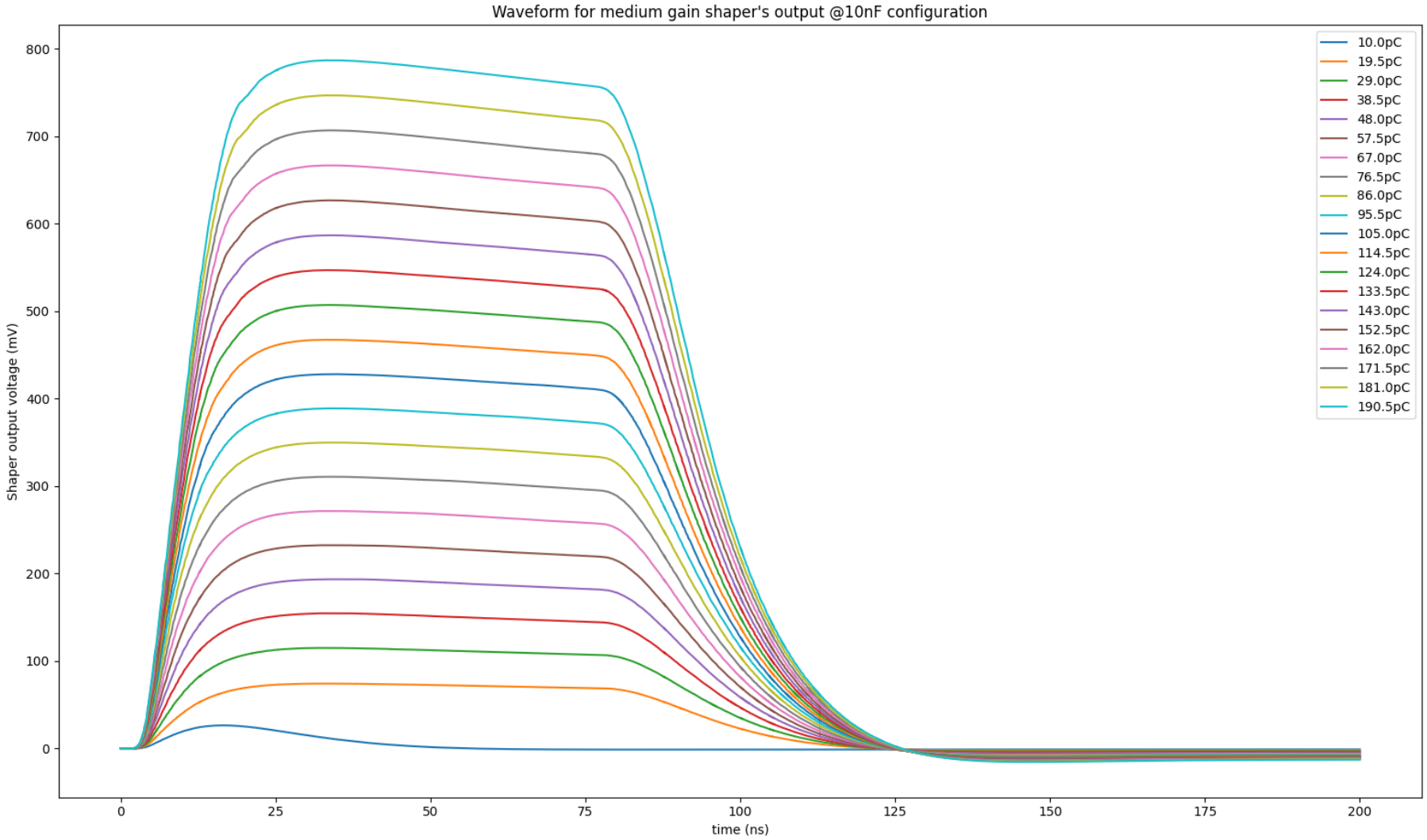
- 3 gains (possibly 4)
- 10b 40MHz ADC (Krakow)
- 25 ps TDC (Saclay)
  - Possibly 12.5 ps



Simulated waveforms (HG)



Simulated waveforms (LG)



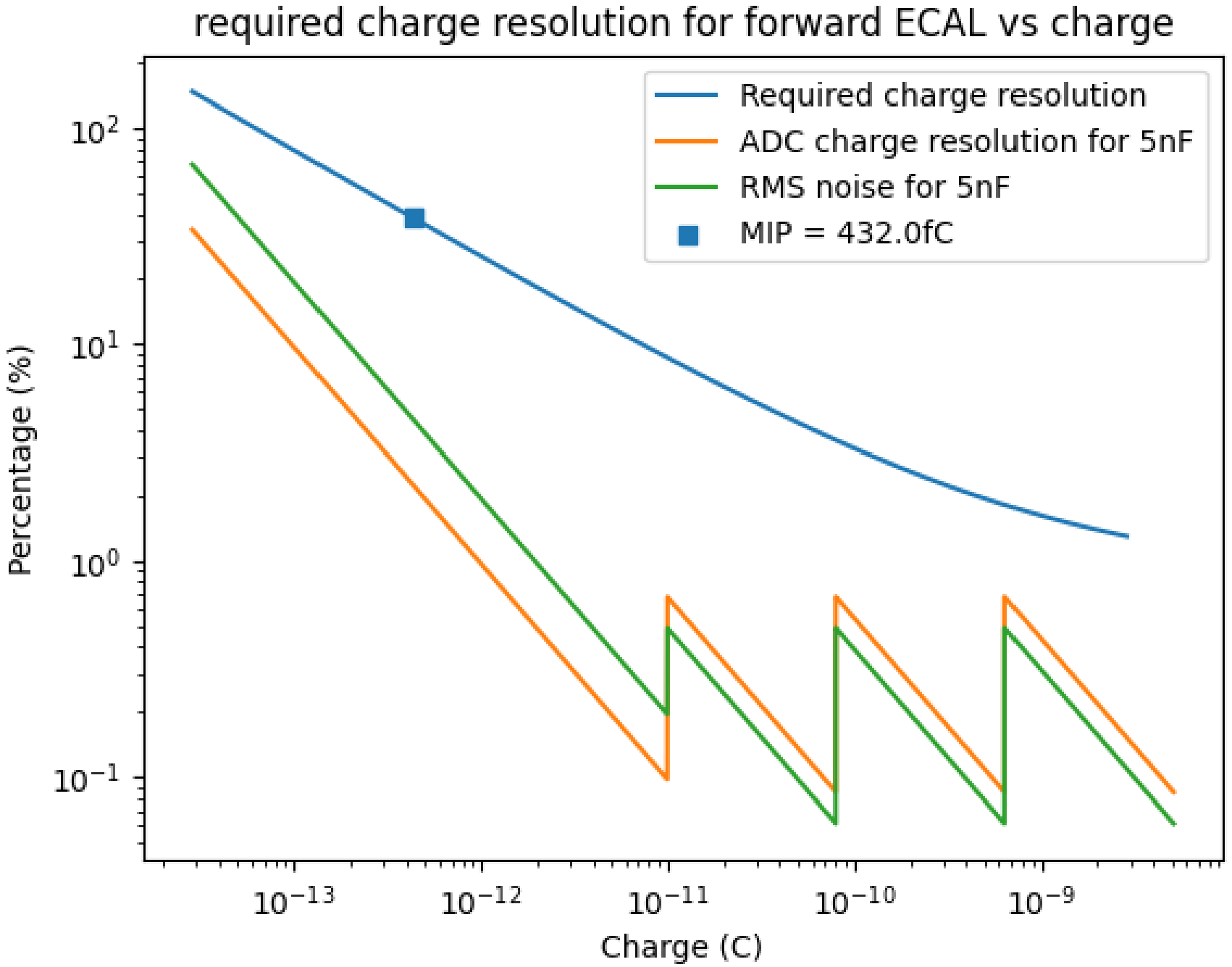
Optimization of sensor configuration (series/parallel)

- Simulations and measurements planned at IJCLAB, LLR and OMEGA

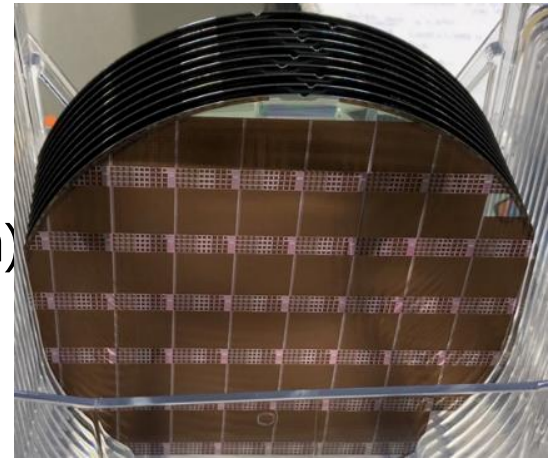
SiPM configuration	4s4p 530pF	16p 530pF	4s 2.5nF	2s2p 2.5nF	4p 2.5nF
Input capacitance	530pF	8.48nF	500pF	2.5nF	10nF
SiPM config gain (μV/p.e)	13.58μV	3.396uV	11.52μV	5.76μV	2.88μV
Dark count rate (typical) [MHz]	11.2	11.2	12	12	12
Dark count rate (max) [MHz]	33.6	33.6	40	40	40

Simulation results using the 2s2p 2.5nF configuration

Operation modes	1	2	3	4
Cf	70fF	70fF	140fF	280fF
Rf	250kΩ	150kΩ	60kΩ	15kΩ
Maximum input voltage	1V	1V	2V	4V
MIP (15p.e)	432fC	432fC	432fC	432fC
Peak voltage @MIP	42.29mV	43.83mV	21.59mV	11.47mV
Jitter @ MIP	180ps	183ps	192.4	180ps
Electronic RMS noise @shaper	1.913mV	2.14mV	1.45mV	1.63mV
SNR @MIP	22.1	20.48	14.89	7.04

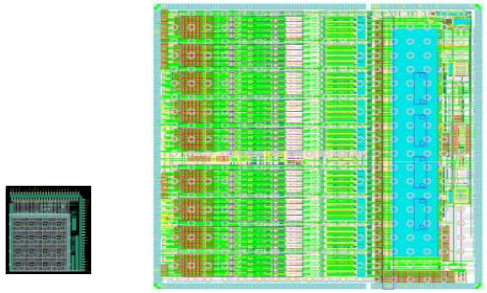

required charge resolution for forward ECAL vs charge
Required charge resolution
ADC charge resolution for 5nF
RMS noise for 5nF
MIP = 432.0fC
Percentage (%)
10^{2}
10^{1}
10^{0}
10^{-1}
10^{-13}
10^{-12}
10^{-11}
10^{-10}
10^{-9}
Charge (C)

Plans for 2024 [ePIC ANL meeting]

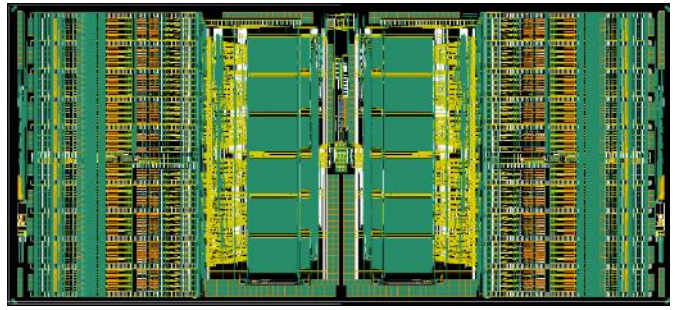


- CALOROC = H2GCROC (SiPM) for EIC
  - Analog part = H2GCROC, backend EIC specific
  - Need to choose HGCROC pin-pin compatibility (64 ch) or HKROC size (32ch)
  - 2 versions : conservative (ADC/ToT), improved (multi-gain)
  - Cost in MPW : 2 * (50 or 100 mm²) * 2 k€ > Engineering run = 250 k€
  - Mid/fall 2024 tbd

HKROC

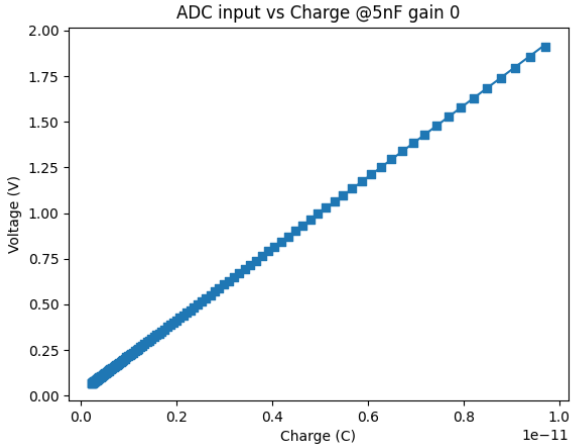


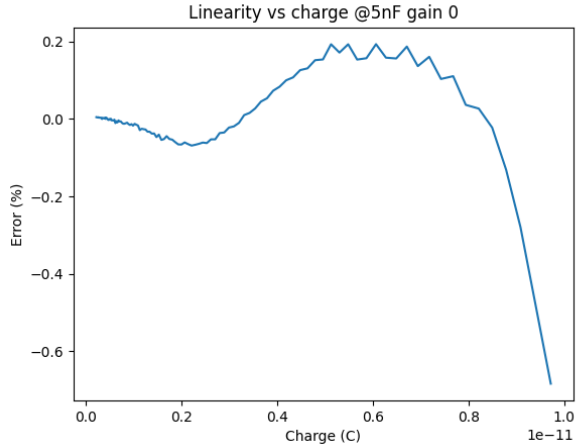
- EICROC
  - Possibly EICROC0A with improved digital noise and low power ADC
  - EICROC1 (4 or 8)*(16-32) channels with possible column « flavours »
  - Probably not yet with EIC readout
  - Area : 20 - 35 mm²
  - Mid/fall 2024 especially if Engineering Run chosen

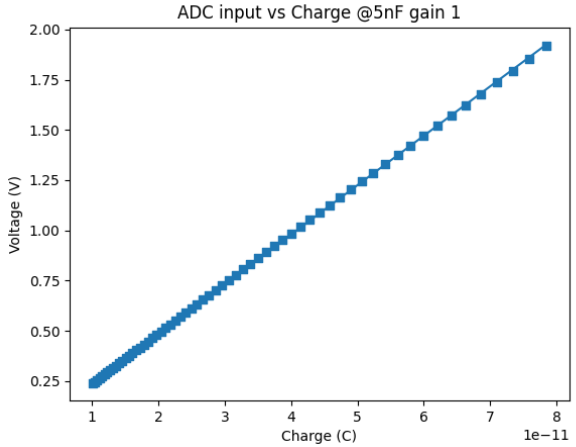


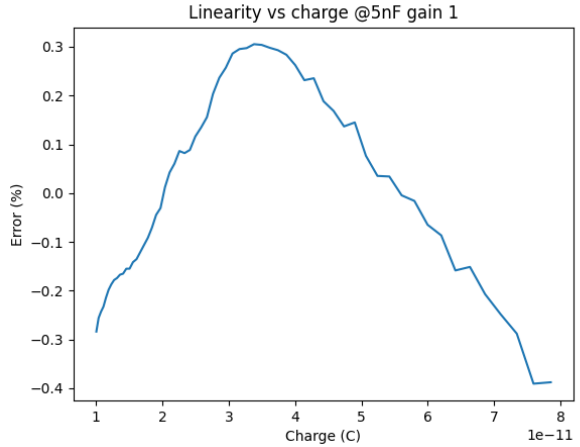
backup

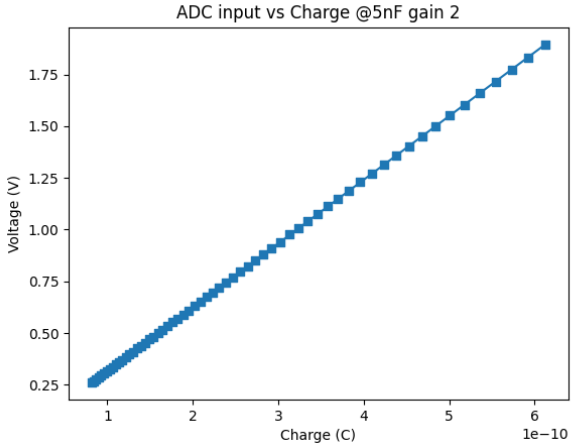
Linearity mode 1 and 2 (they are similar)

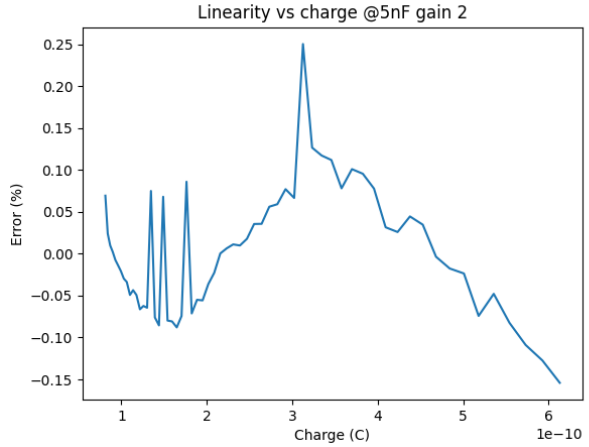


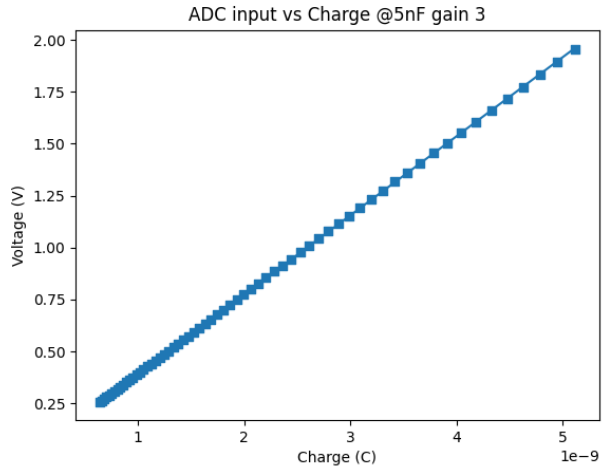


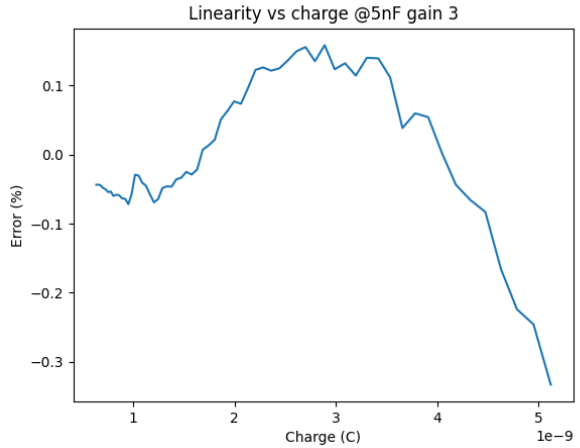




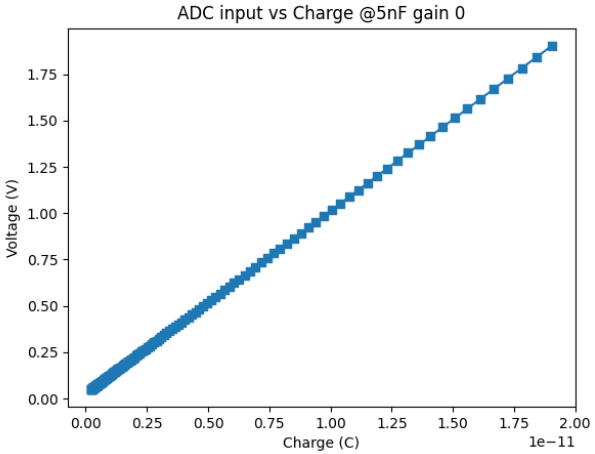


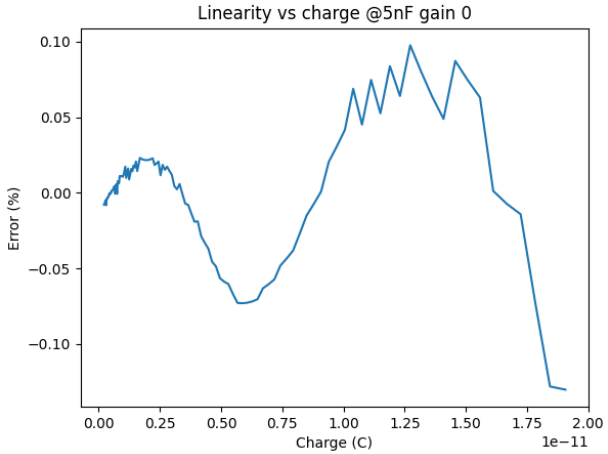


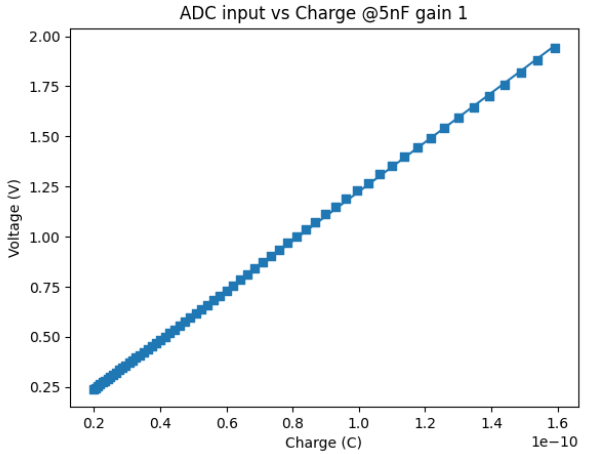


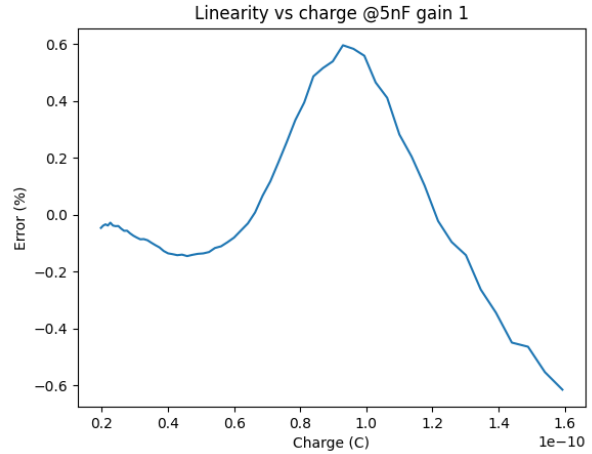


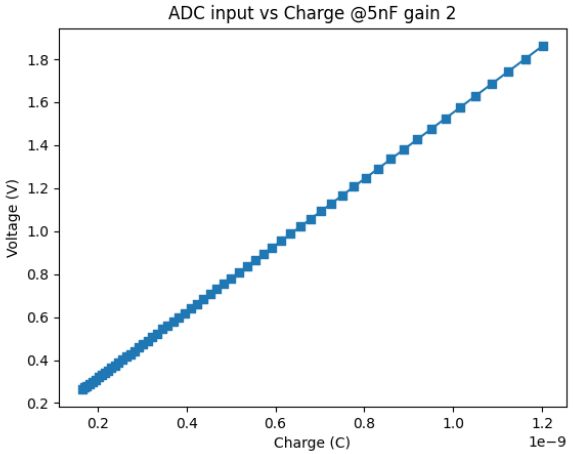
Linearity mode 3

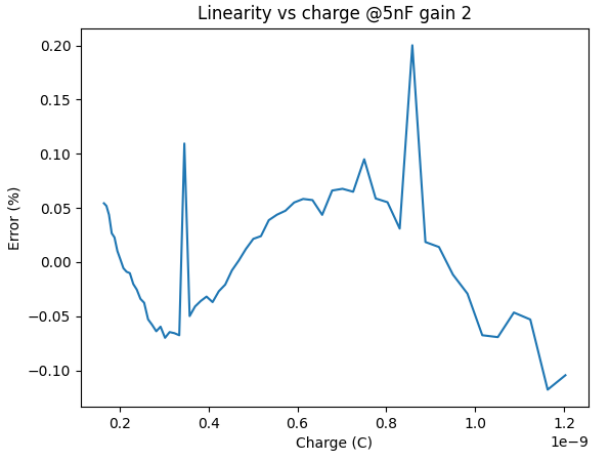


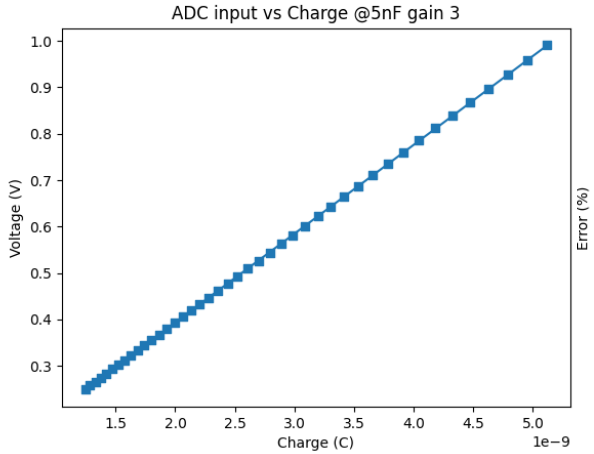


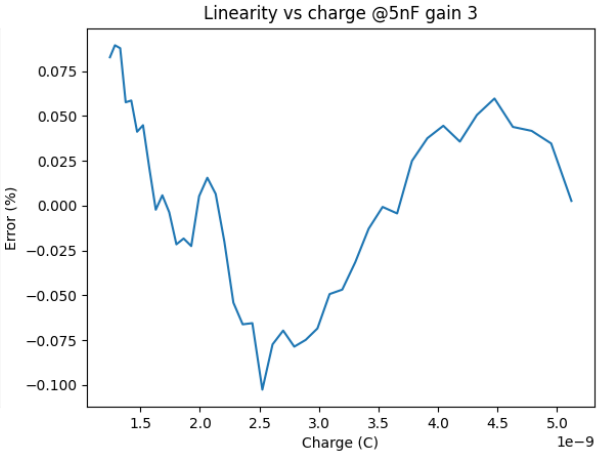




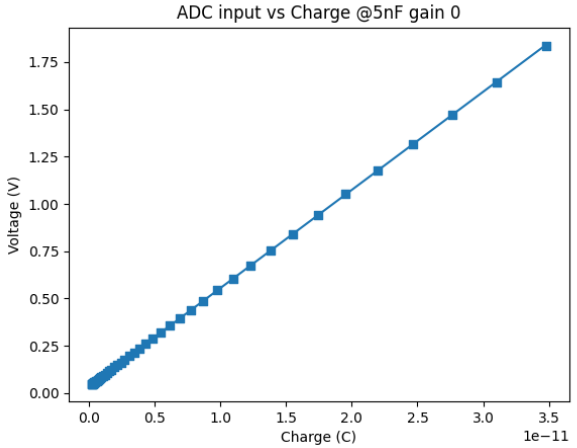


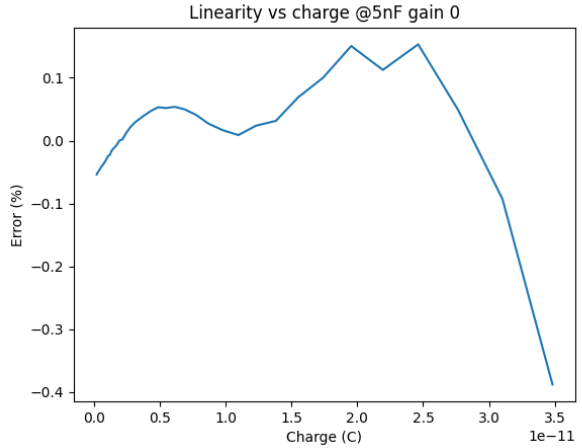


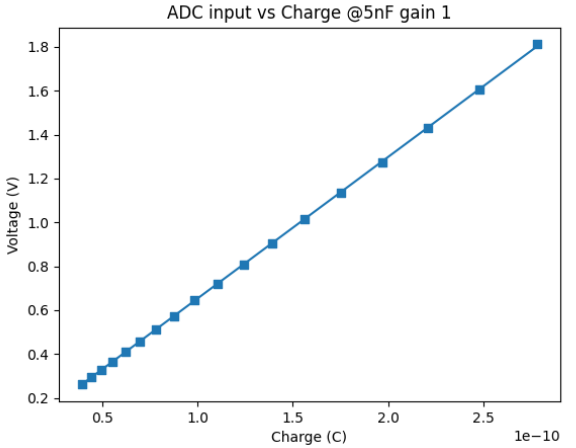


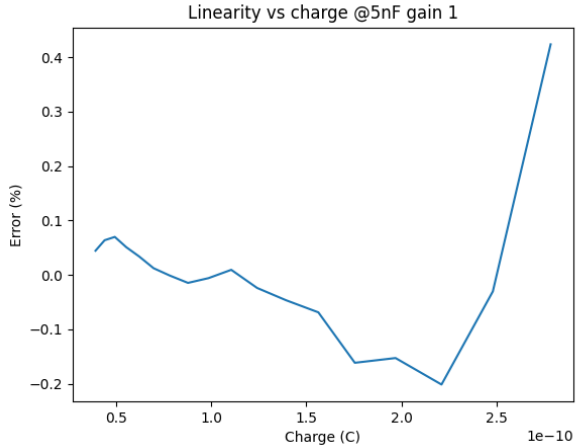


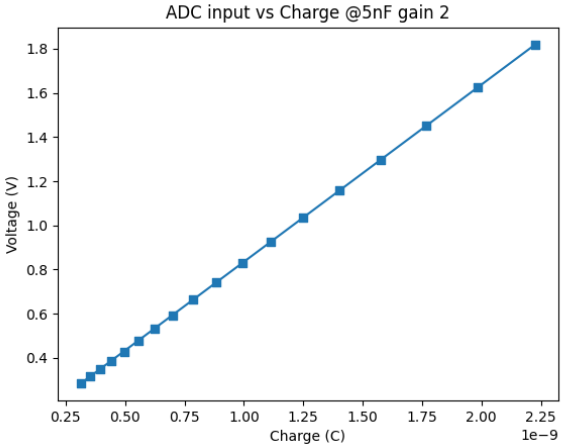
Linearity mode 4

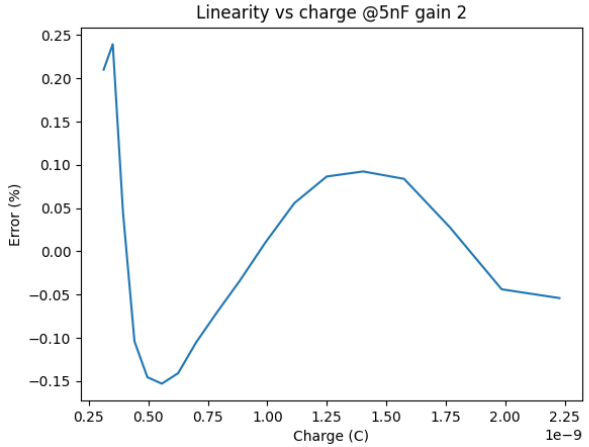


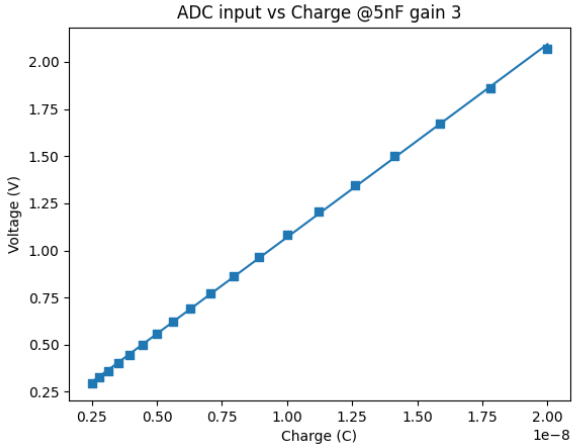


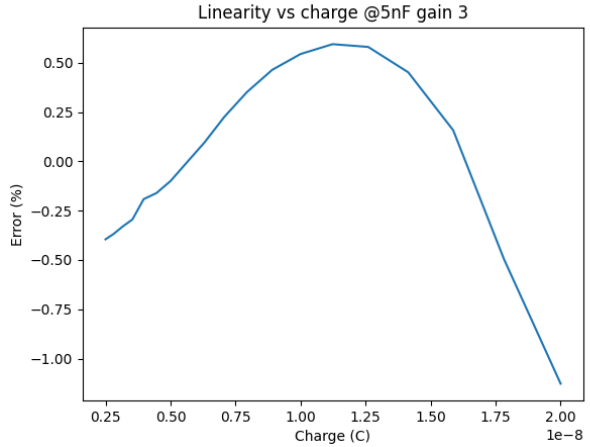


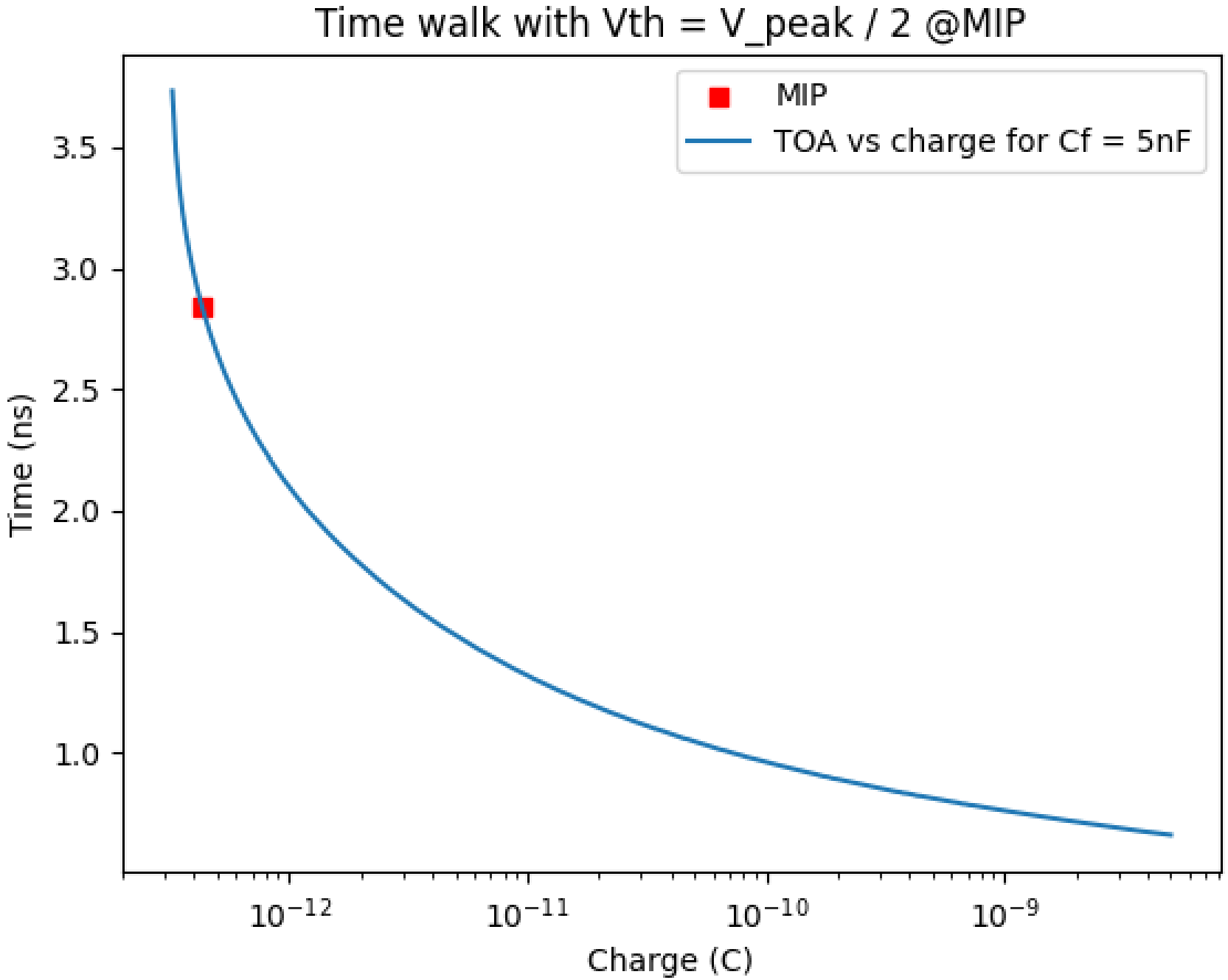


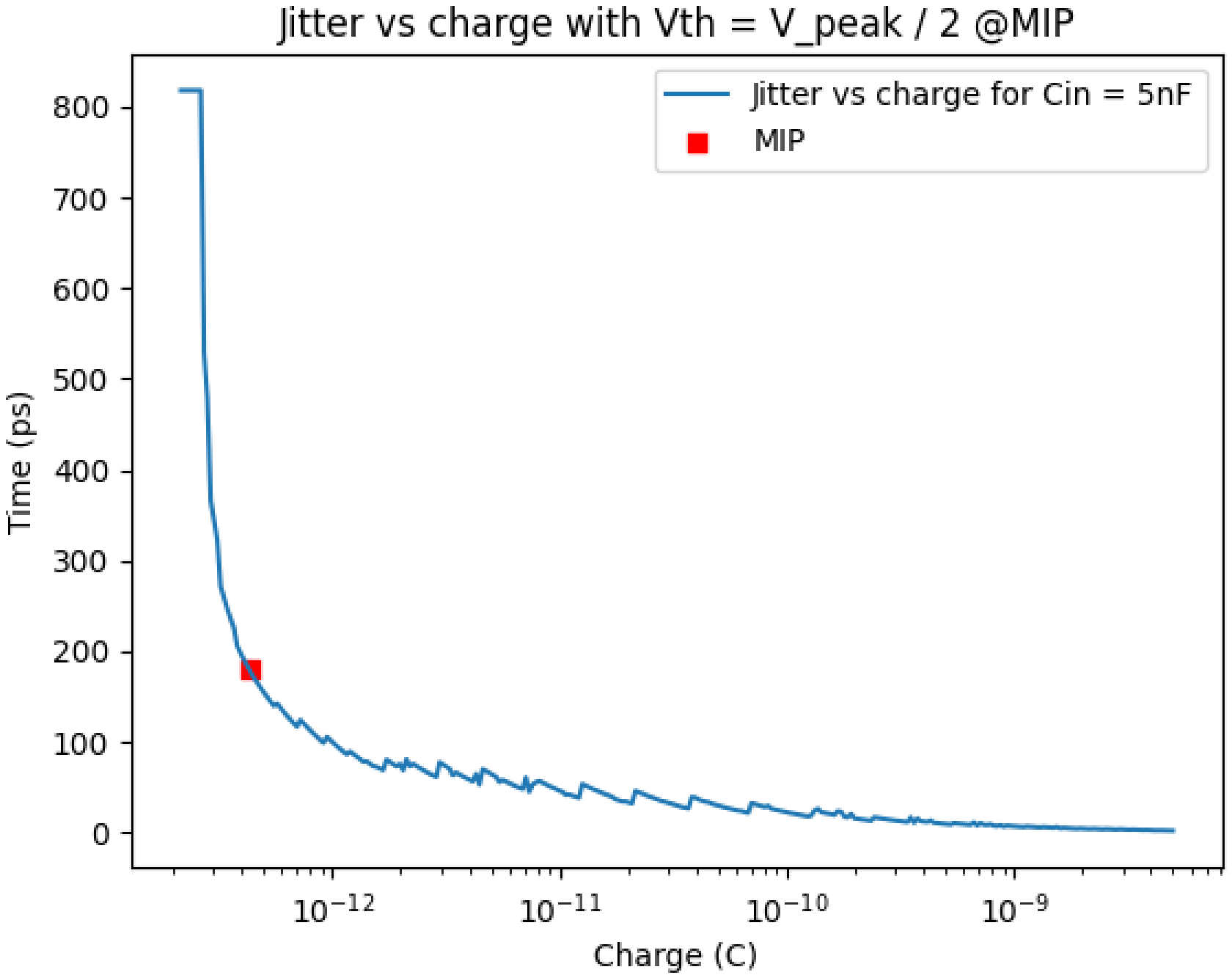






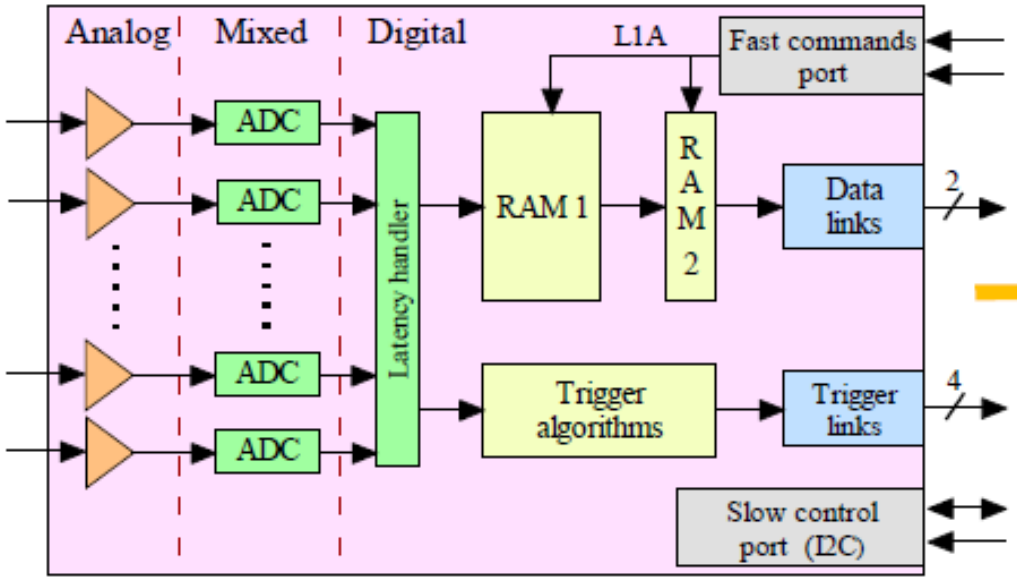


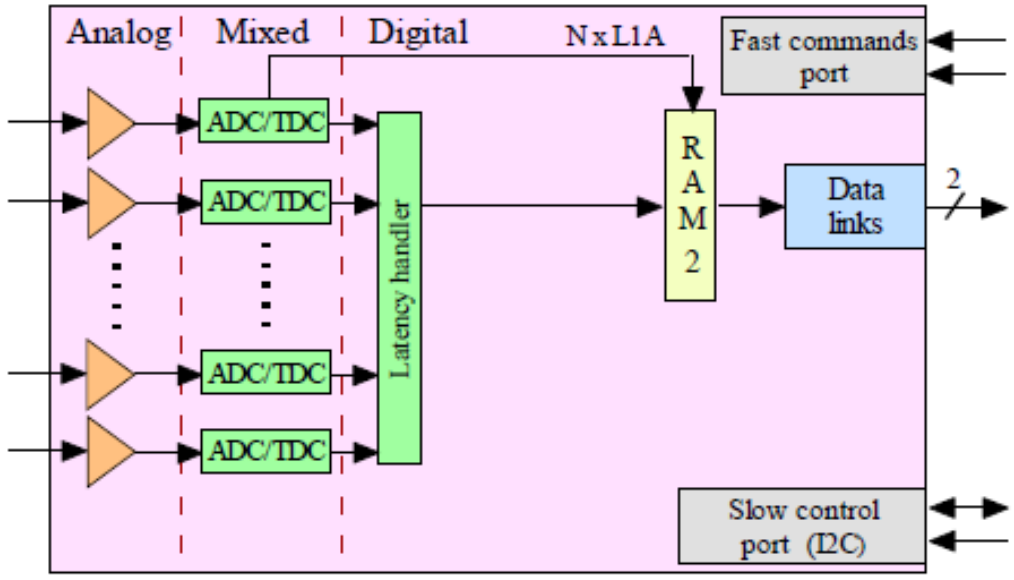

Time walk with Vth = V_peak / 2 @MIP
MIP
TOA vs charge for Cf = 5nF
Time (ns)
3.5
3.0
2.5
2.0
1.5
1.0
10^{-12}
10^{-11}
10^{-10}
10^{-9}
Charge (C)


Jitter vs charge with Vth = V_peak / 2 @MIP
Jitter vs charge for Cin = 5nF
MIP
Time (ps)
800
700
600
500
400
300
200
100
0
10^{-12}
10^{-11}
10^{-10}
10^{-9}
Charge (C)

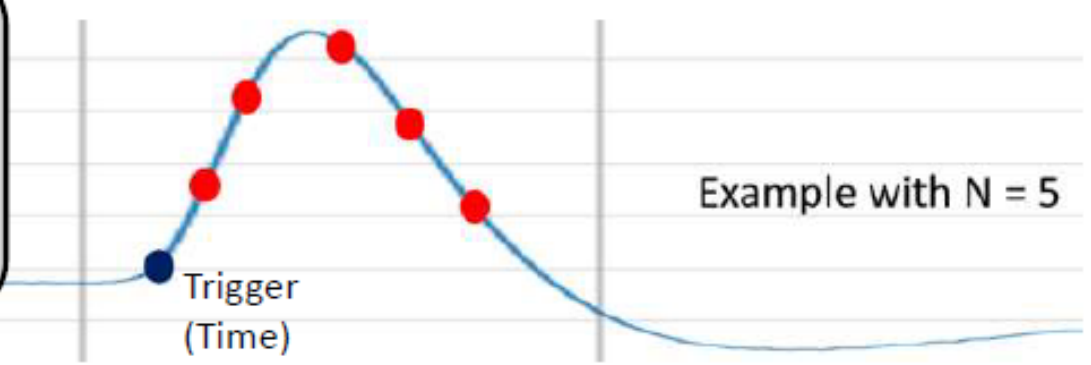
Evolution for EIC readout [F. Dulucq]

- Data streaming : auto-trigger and zero-suppress



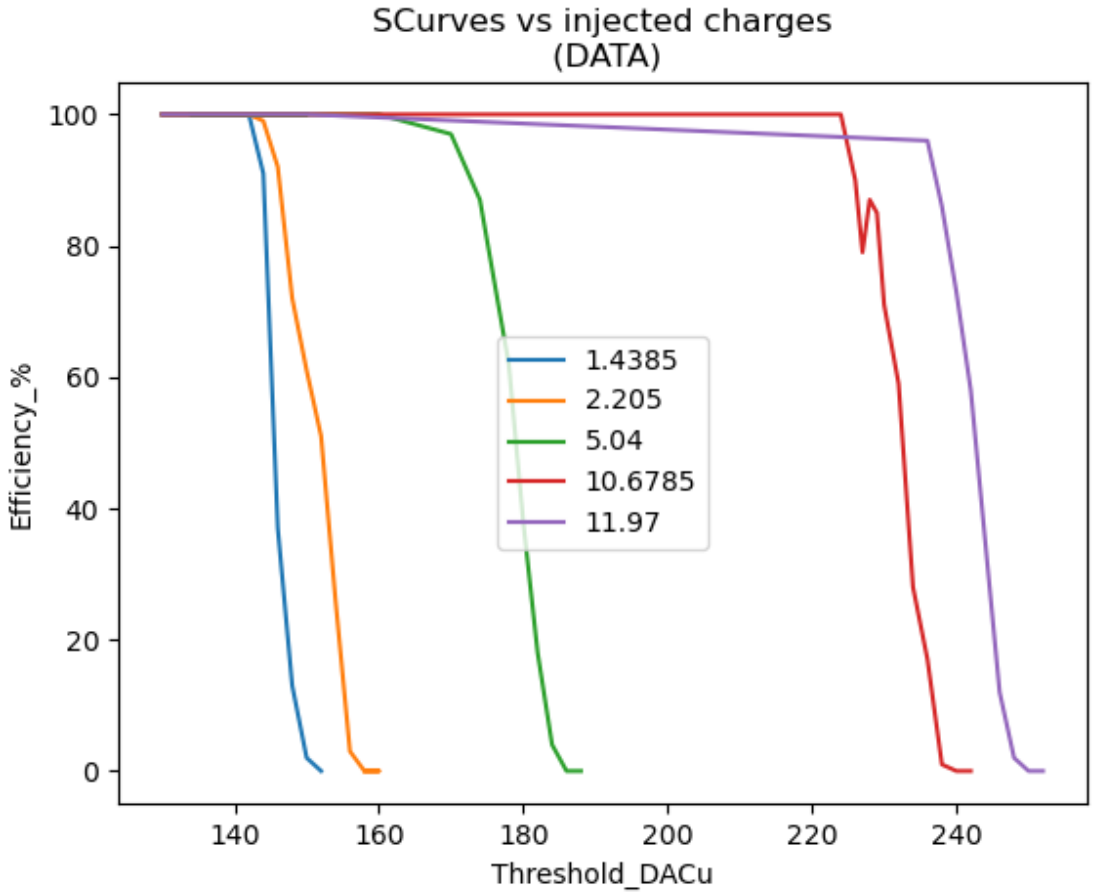


- Each event passing the threshold is readout
- Auto-trigger with N "samples" (1 to 7)
- Can be exercised with present HGCROC (multiple L1A-triggers)



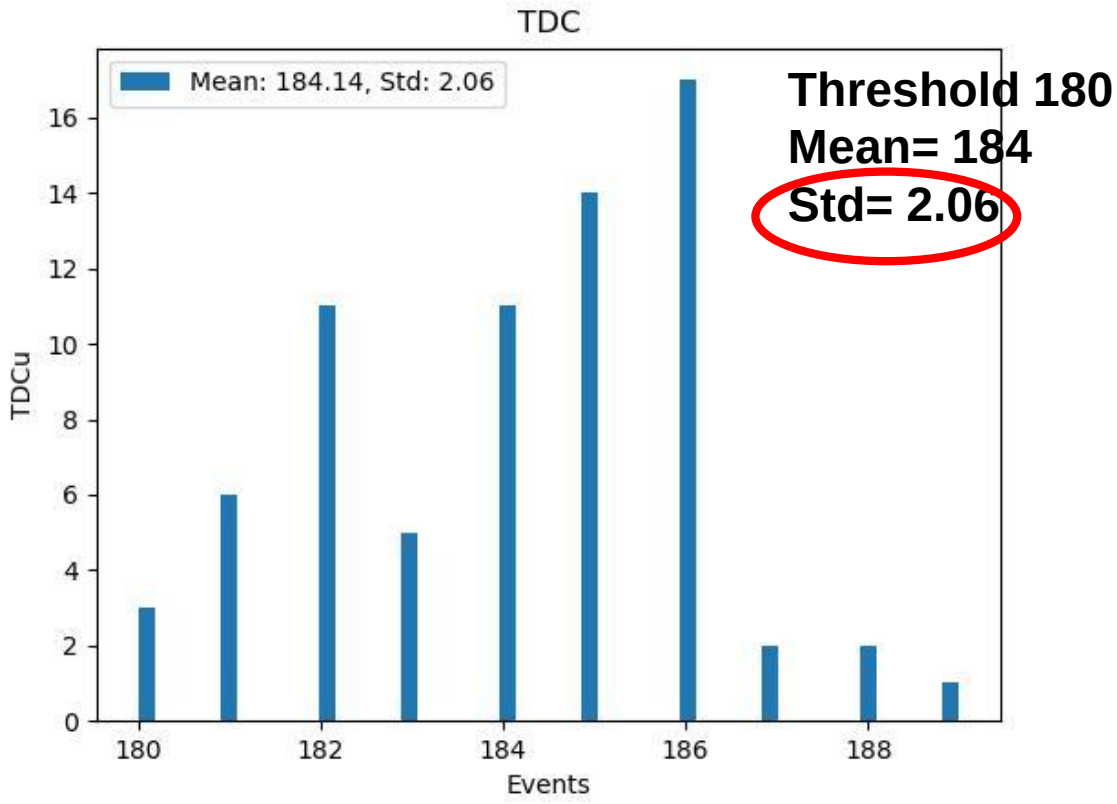
Trigger efficiency [Selma, Adrien]

- Measurements with DAQ (clocks on)
- Minimum threshold ~ 2 fC
- Noise from s-curve ~0.2 fC
- Better from what is observed with analog probe (~10fC clock noise)
  - Probe picks up clock noise

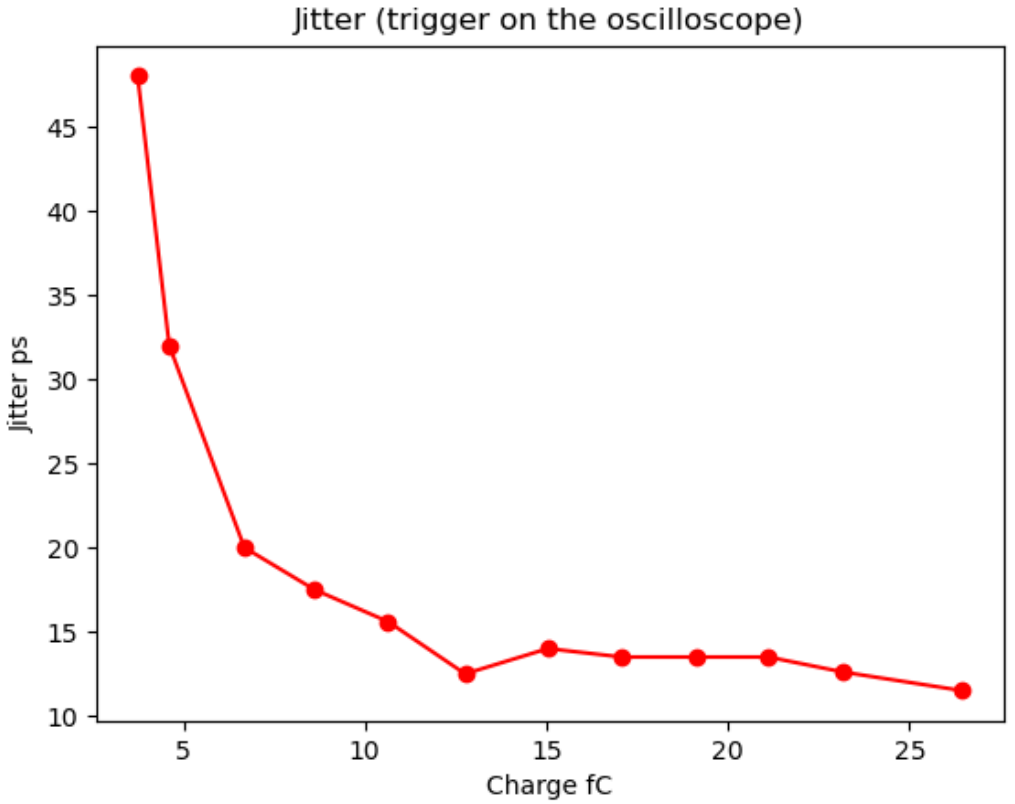


Jitter measurement [Selma, Adrien]

- Scope measurement from discriminator output : 15 ps @ 10 fC
- TDC measurements ~50 ps
  - Still large correlated noise under investigation



Threshold 180
Mean= 184
Std= 2.06



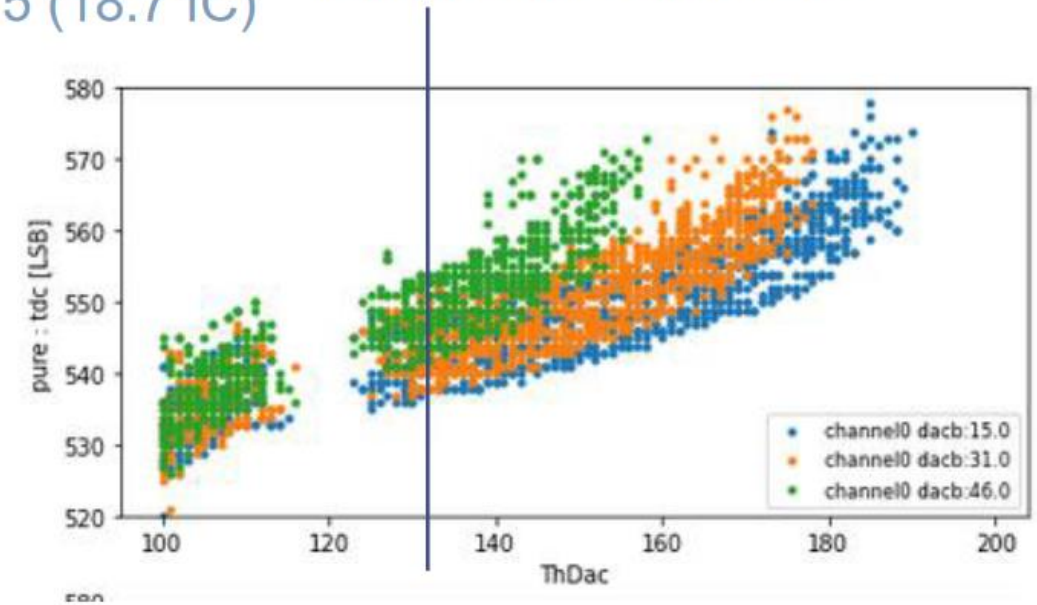
More TDC measurements [Florent]

- Threshold ~2 fC
- Noise ~3 TDCU = 75 ps

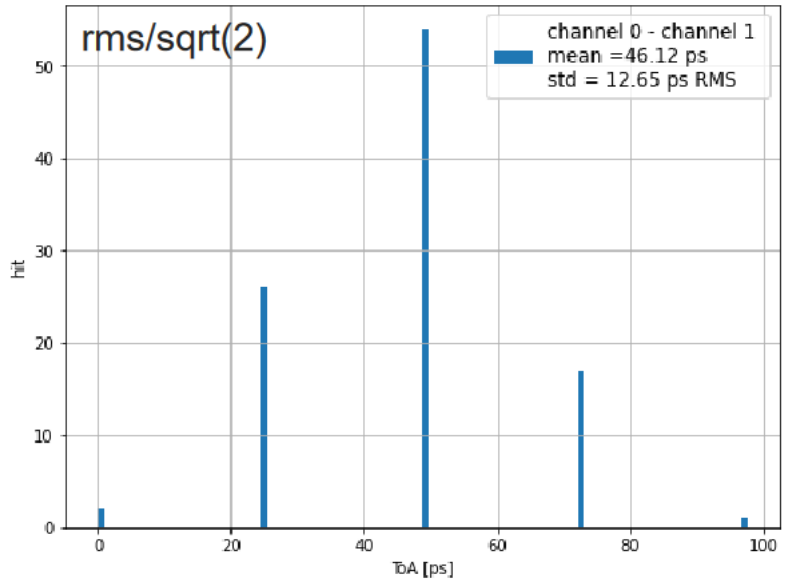
dacb_pulser :

- 46 (6.2 fC)
- 31 (12.5 fC)
- 15 (18.7 fC)

Estimated noise floor : 2 fC ?



ThDac : 130 :

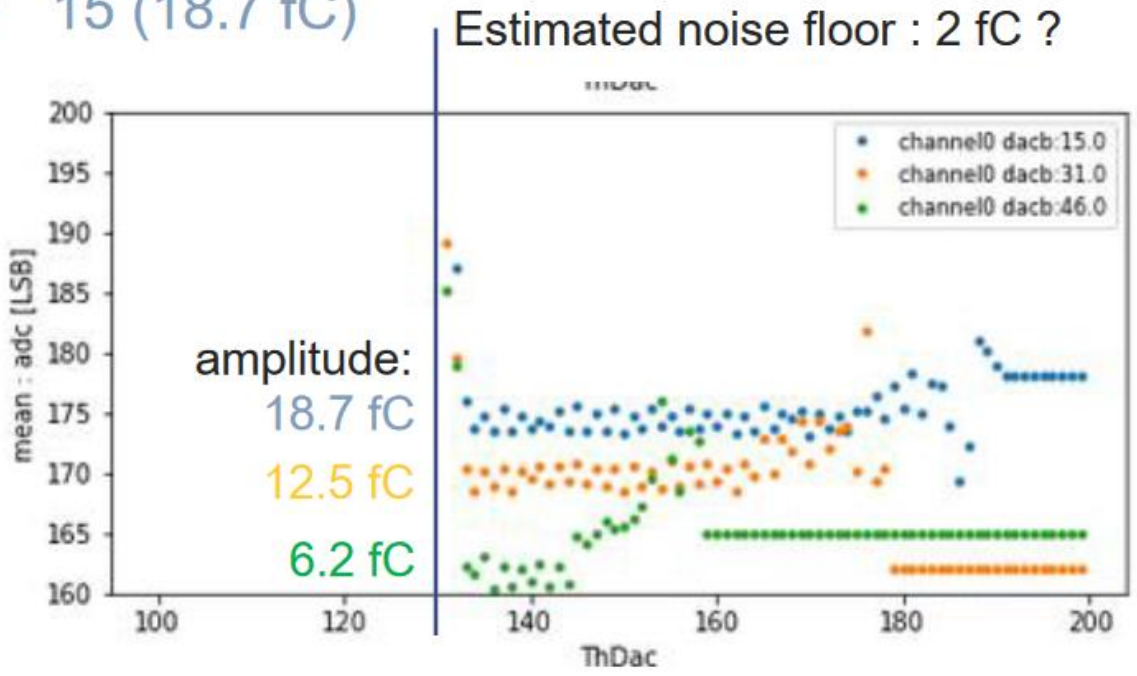


Distribution of the time difference

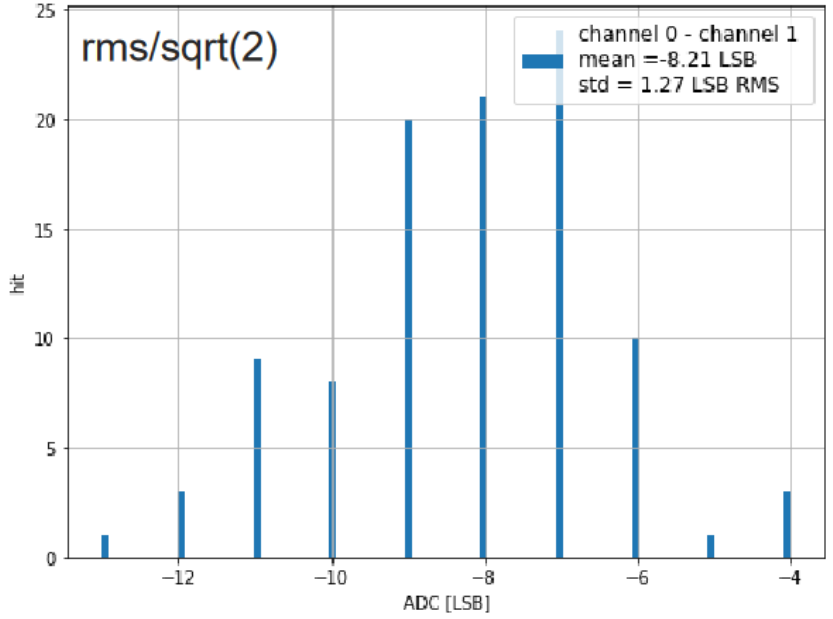
Preliminary ADC measurements [Florent, Laurent]

- ~large ADC noise (~10 UADC) under investigation
- Mostly coherent

dacb_pulser :
- 46 (6.2 fC)
- 31 (12.5 fC)
- 15 (18.7 fC)



ThDac : 150 :

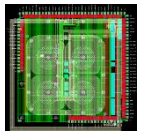


Distribution

Noise near 1.2 LSB RMS

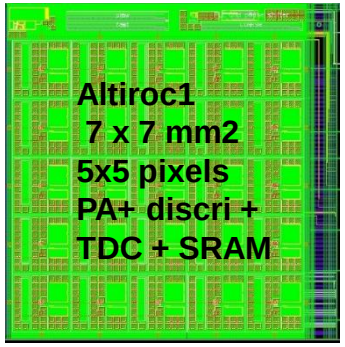
ATLAS LGAD readout : evolution of ALTIROC

2016

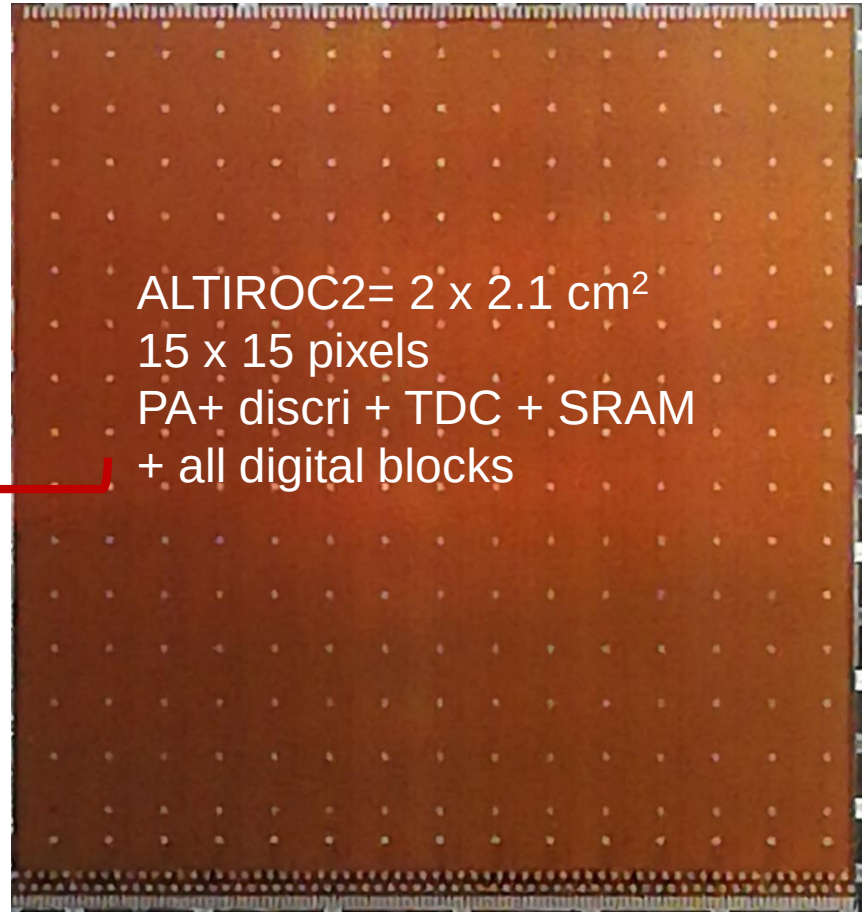


Altiroc0
2 x 2 mm2
2 x 2 pixels
PA + discri

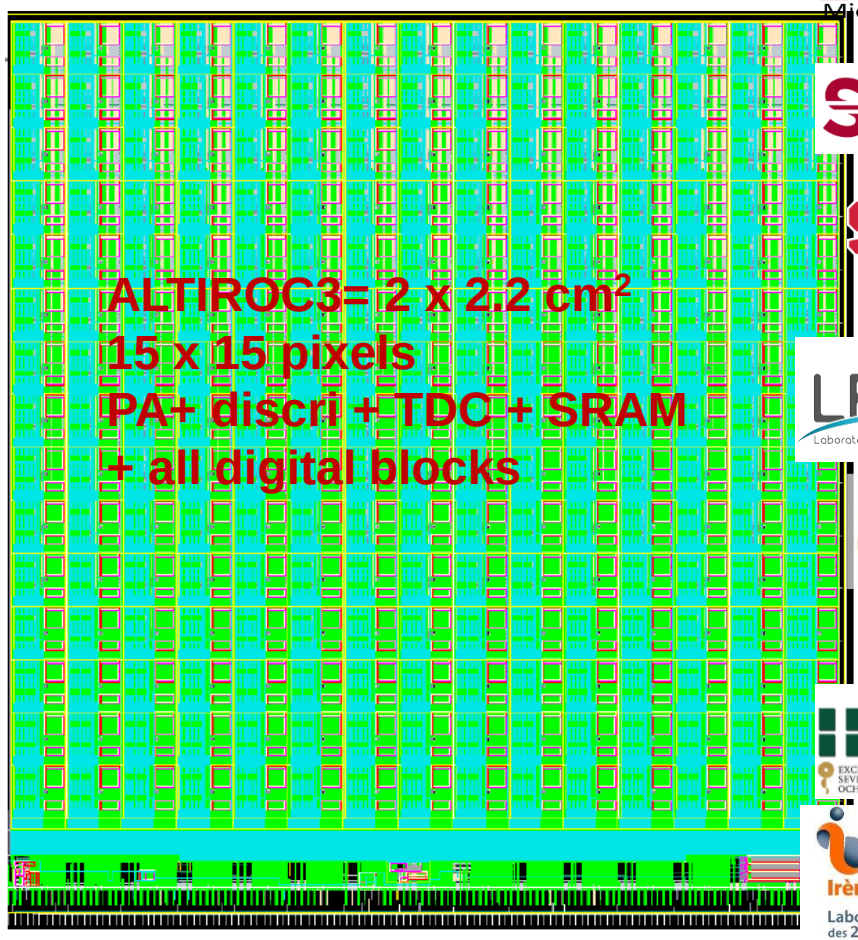
2018



2019



2021



Altiroc0 and 1:
No digital,
To validate the FE part at system level (= ASIC bump-bonded onto a sensor)

ALTIROC2:
First full size chip with 15 x 15 channels – 2 x 2 cm2
To demonstrate the functionality/performance of the ASIC (time resolution + luminosity counting) alone and bump-bonded onto a sensor
But NOT to be fully radiation hard (against SEE)

ALTIROC3:
Last full chip prototype before pre-production
Same as Altiroc2 but fully triplicated

Comparison EICROC / HGCROC

EICROC

- « 2D chip » 16 -> 1024 channels
- Input capacitance : Cd = 1-5 pF
- Dynamic range : 1 fC – 50 fC
- ToA and ADC
- Target power : 1 mW/ch
- Area 10 mm² (300 mm² final)

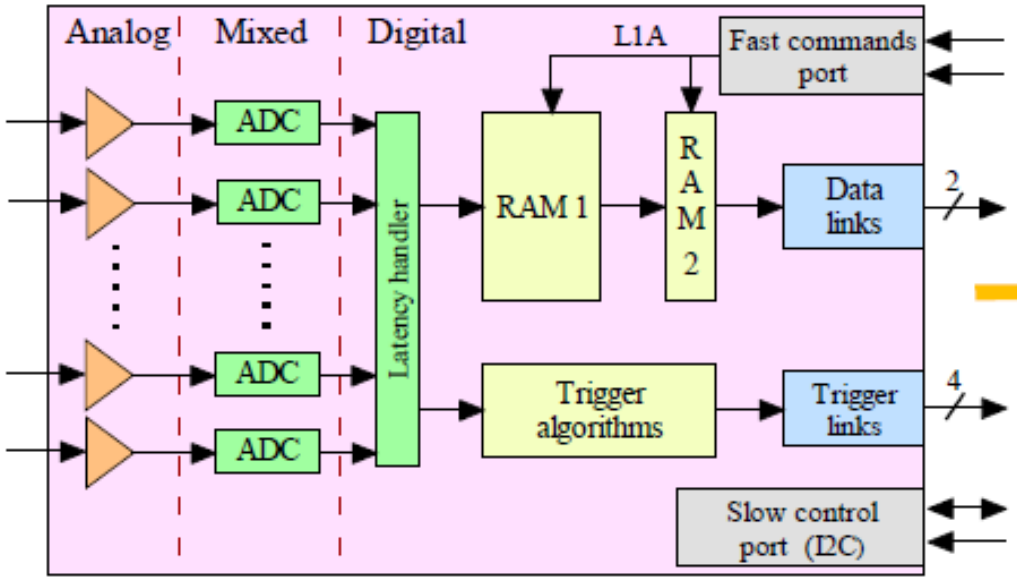
HGCROC

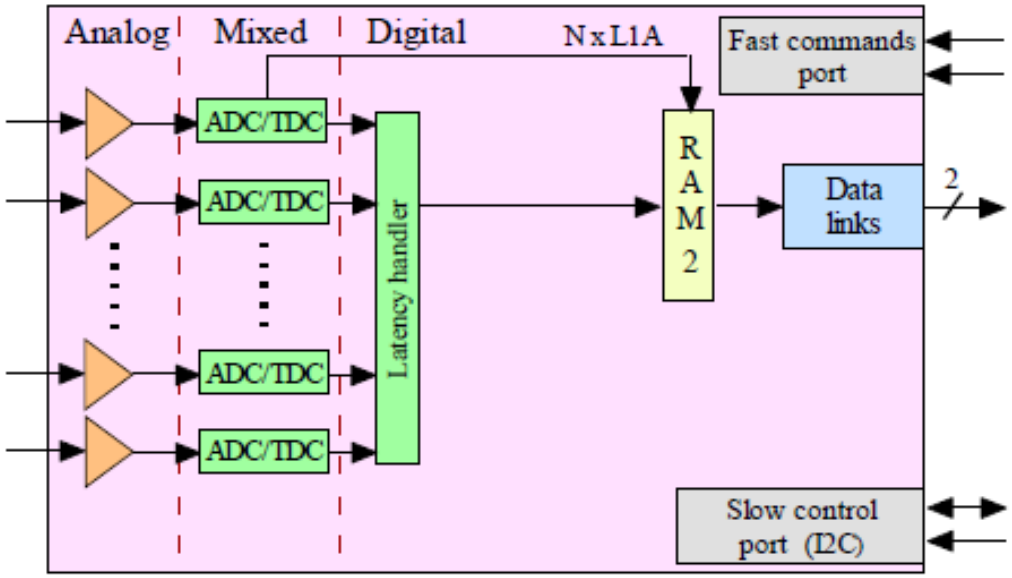
- « 1D chip » 72 (64) channels
- Input capacitance : Cd = 5-50 pF
- Dynamic range : 1 fC – 10 pC
- ToA and ToT
- Target power : 5-10 mW/ch (now 15)
- Area 100 mm²

- SiPM version H2GCROC
- Cd = 100 – 2.5 nF
- Studies for 10 nF groupings
- Can be used by EIC calo

Evolution for EIC readout [Frédéric]

- Data streaming : auto-trigger and zero-suppress, 200 MHz clock
- Already done in HKROC (see backup)





- Each event passing the threshold is readout
- Auto-trigger with N "samples" (1 to 7)
- Can be exercised with present HGCROC (multiple L1A-triggers)