eRD109: Progress Report

Matthew Gignac on behalf of the
UC Santa Cruz UFSD group

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Status & Plans

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Investigating third party ASIC solutions for AC-LGAD ToF detectors

- ***HPSoCv2 ASIC (Nalu Scientific)*:**
  - Chip with fixed digital back-end under fabrication at TSMC – **expected by March**
  - Once revised chip is in-hand, full re-characterization with and without sensors planned. Until we receive the revised chip, not much work expected on this chip
- ***AS-ROC (Anadyne Inc.)***
  - Chip designers came to UC Santa Cruz on February 20th; Had a productive debugging session
    - Concluded that the discriminator cross-talk is caused by the output driver of the discriminator. Small amount of cross-talk (~2%) in the pre-amplifiers
    - Solving these issues would require a re-design. Not planned in the context of eRD109/ePIC since funding for this chip has not been continued. We will summarize its performance and effectively conclude our work on this chip in the coming month.

Milestones

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Milestones and timelines

1. ~~ASROC and HP-SoC board design, layout, and production (Summer-Fall 2023~~)
2. ~~ASROC~~ and HP-SoC ASIC characterization (Fall 2023)
3. ~~ASROC~~ and HP-SoC integrated system tests & characterization. ASICs will be paired with eRD112 sensors (Winter 2024)

Only remaining work for this funding period is on the revised HPSoC-v2 chip