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Status report of the eRD109 project on SALSA chip development

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EPIC DAQ/electronics WG meeting

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SALSA CHIP TARGET SPECIFICATIONS

Versatile front-end characteristics

- Dedicated to MPGD detectors and beyond
- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1nF
- Large range of peaking times: 50-500 ns
- Large gain ranges: 0-50 to 0-5000 fC
- Large range of input rates, up to 100 kHz/ch with fast CSA reset (limit assumed for EPIC: 25 kHz/ch)
- Reversible polarity
- Front-end elements can be by-passed

Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s
- Possibility to double rates by coupling pairs of channels
- Integrated DSP for internal data processing and size reduction, treatment processes to be selected according to user needs
- Continuous readout compatible with streaming DAQ foreseen at EIC, triggered mode also available
- Several 1 Gb/s output data links

General characteristics

- ~1 cm² die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, TID), working at 2T magnetic field

STATUS OF SALSA0_DIGITAL PROTOTYPE

SALSA0_digital

- Tested from end of November 2023 to evaluate ADC block performance
- Resolution OK but max sampling rate too low, fixed in present design
- Problem of offset of the digital 0, with reduced dynamic range leading to lower ENOB
- Also lower power consumption compared to simulation
- 10 more chips were packaged, but they are also affected with the same problems
- Studies ongoing in simulations, but can’t reproduce these behaviors yet, to be continued

STATUS OF PRISME PROTOTYPE

PRISME prototype

- Test of new hybrid 65nm PLL block for SALSA with 4 clock outputs

Test bench

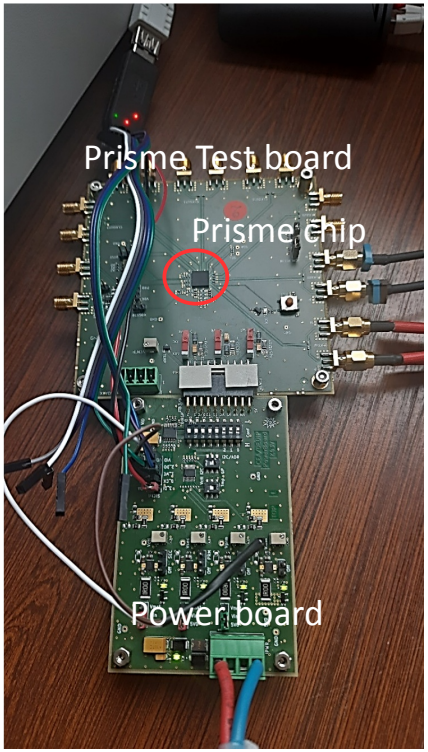
- Power boards + PRISME test boards arrived February 19th and are working
- Test bench completed with low jitter clock generator from CERN + high precision signal generator, 80GS/s scope and phase noise analyzer

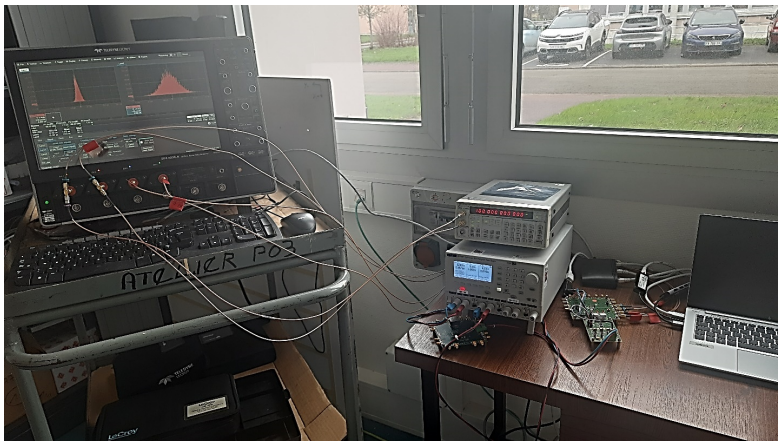
Preliminary results

- Power consumption nominal
- I2C working to read and write registers
- Low voltage differential clock signals going in and out the chip

Tests on PLL block

- Digital branch of PLL operational (allows to find the right frequency range for the analog branch)
- Oscillator driven by analog branch reaches the 3.2 GHz nominal frequency from 40 and 100 MHz input clocks, divider working properly
- 4 configurable outputs tested → deliver right requested frequencies
- Ongoing tests on jitter characterization and optimization





STATUS OF SALSA1 DEVELOPMENT

Purpose and architecture

- Performance evaluation of front-end + ADC chain, + tests of different blocks
- 4 front-end channels + 2 direct inputs to ADC, 12-bits parallel output with dynamic multiplexer

General Status

- Schematics in progress, 1st version produced with some missing blocks
- Submission to TSMC foreseen April 17th → tight time line

Front-end stage

- Layout design of updated SALSA0_analog version almost finished
- New version of front-end with improved pole-zero cancellation: schematics and layout ongoing

ADCs

- ADC 1 (Sao Paulo): updated to 50 MS/s sampling rate, reduced surface (200 x 250 µm²)
- Schematics completed, analog part of layout done, finalization of digital part
- Design of interface buffer between front-end and ADC in progress
- ADC 2 (Saclay): schematics completed, layout design almost complete, simulations at layout level in progress
- Integration in SALSA1 of both ADCs, each for one half of the channels

Services

- PLL, bandgap, probes, taken from PRISME
- I2C and service layouts completed, basic I2C architecture validated with PRISME
- Multiplexer layout in progress, simulations in progress

STATUS OF SALSA2 DEVELOPMENT

Purpose and architecture

- Like final SALSA but with reduced number of channels - 32 ?
- Implement full chip architecture including DSP and input/output interfaces in a version close to the final one

DSP

- First draft of data processing established and presented at EPIC DAQ WG in January
- Design of architecture in progress, draft of data format in discussion
- Draft list of processes: baseline correction, common mode correction, digital filtering, zero suppression, feature extraction, trigger management, generation of calibration data, data formatting
- We still need inputs about DSP feature requests from MPGD and DAQ WGs ! (cf January presentation)

Input interface

- Unified interface proposed, combining clock + synchronous commands + slow-control in one diff line, under study
- Synchronization of chip with EIC/EPIC time structure, connection with DAQ commands, etc... under discussion with EPIC DAQ community, we also need inputs on this !

Expected to be submitted first trimester 2025

PROJECT MILESTONES AND NEXT STEPS

eRD109 FY23 project milestones

- Specifications of SALSA1 design → done
- Production of SALSA1 prototypes → submission expected April 17th
- Packaging and test card production → expected Autumn 2024
- Performance evaluation → expected end of 2024 / beginning of 2025

Milestones of generic R&D program for EIC project (new 65nm PLL block)

- PRISME prototype submission → done July 19th 2023
- Packaging and test card production → done February 2024
- Radiation tests → Summer 2024 ?

eRD109 FY24 project milestones (proposal)

- SALSA2 specifications → July 2024
- SALSA2 submission → March 2025
- Beginning of SALSA2 tests → September 2025

Very next steps

- Tests on PRISME prototypes → in progress
- SALSA1 submission → April 17th
- SALSA2 specifications and architecture → Spring-summer 2024