Status of the eRD109 “RDO/Timing/Service Hybrid”

EPIC DAQ Meeting, 07-Mar-2024

Wei Li, Mike Matveev, Tonko Ljubicic (Rice University)

William Gu (Jlab), as an external contributor and interested party

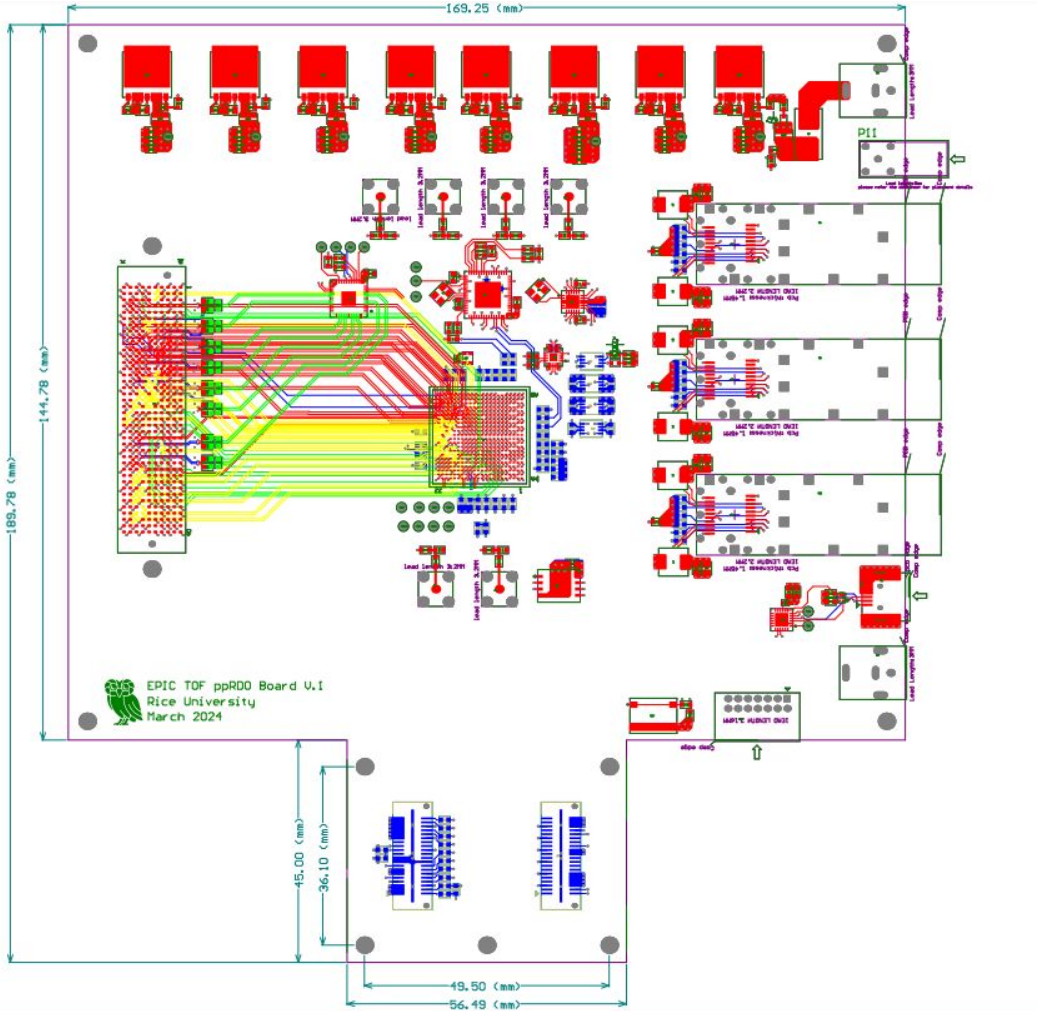
Zhenyu Ye (LBL)

Prithwish Tribedy, Prashanth Shanmuganathan (BNL)

Status as of today

	Feb 1, 2024	Mar 7, 2024	In Proposal
Schematics	90%	100%	Jun 1
0th firmware	90%	100%	–
Purchase long-lead items	0%	100% FPGA 90% others	Jun 1
Board layout	50%	90%	–
PCB design	0%	50% (external vendor)	Aug 1
Boards complete	–	~end April	Sep 31

Comfortably ahead of schedule!



⇐ ppRDO PCB top layer

Conclusion

- Ahead of schedule
- Setting up firmware & lab development tasks
  - William: timing distribution, fiber protocols
  - TL: general framework, ASIC to/from general data flow (ETROC, EICROC1+, other ASICs?)
  - LBL: ETROC integration
  - BNL: lab timing measurements, EICROC1+ interfacing