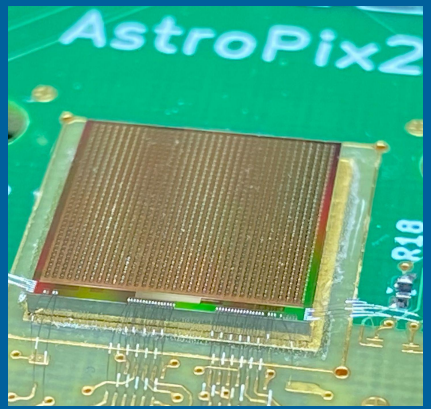
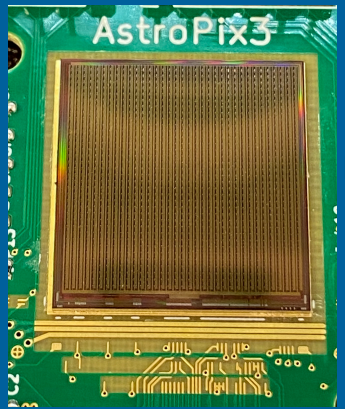
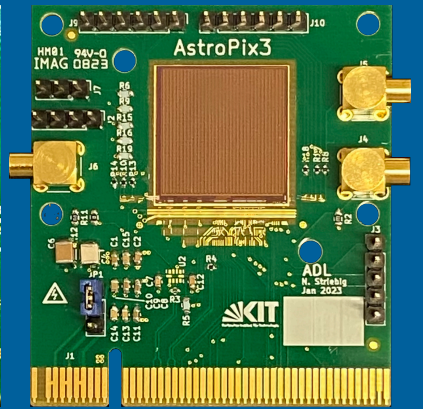
ePIC BIC R&D Meeting

AstroPix bench test







Manoj Jadhav
Argonne National Laboratory

March 06, 2024

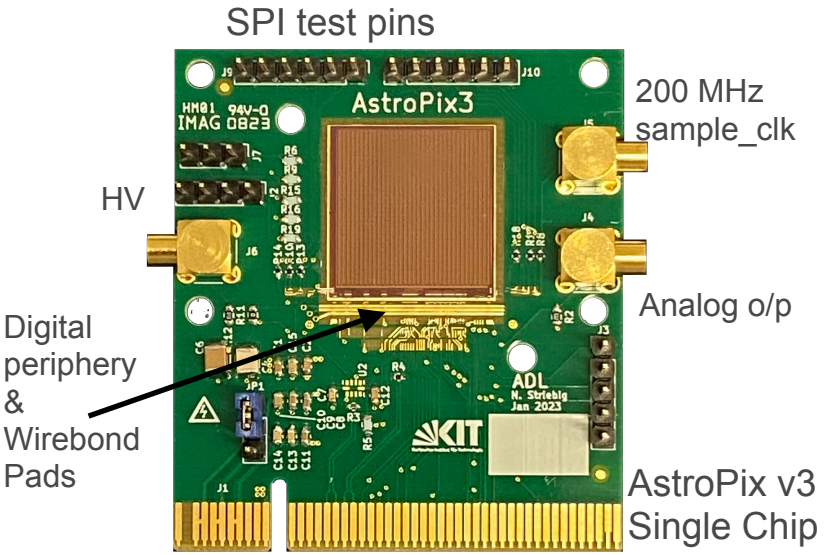
AstroPix v3 Specifications

AstroPix v3

- 2 × 2 cm² full-size chip with 35 × 35 pixel matrix
- 10-byte data frame per hit
- Noise scans
- Chip-generated injection signal
- Energy Resolution with sources

AstroPix v4

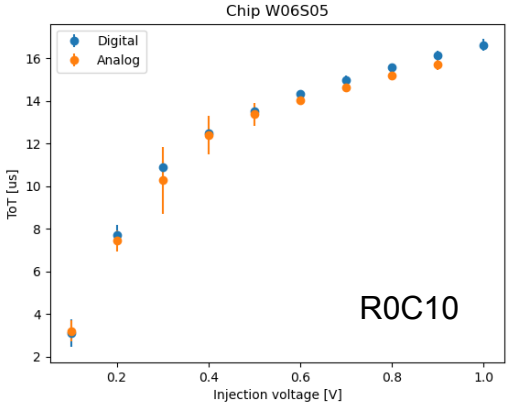
- 1 × 1 cm² chip with 13 × 16 pixel matrix
- 7-byte data frame per hit
- TuneDAC per pixel
- Energy Resolution
- Tuning and Calibration



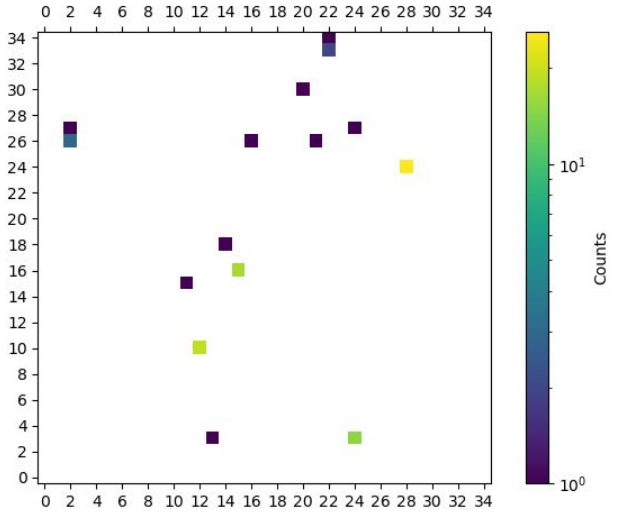
AstroPix v3 Results

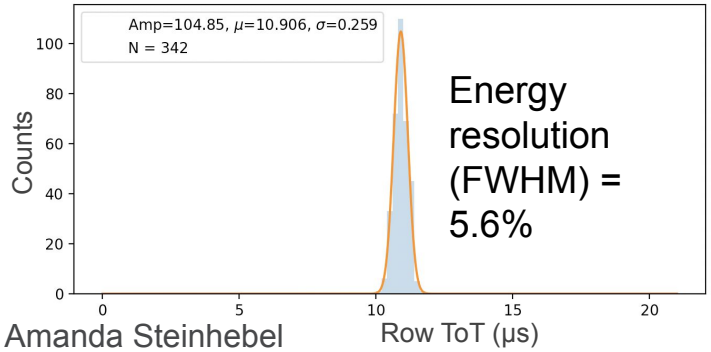
Test Bench Measurements

- Injection voltage scan shows that the analog and digital ToT agree well
- The energy resolution of 5.6% is measured using an injected pulse
- Noise scan shows <1% of noisy pixels
  - resolves issue with noisy pixels observed with v2
- Noisy pixels can be masked by disabling the comparator



Amanda Steinhebel





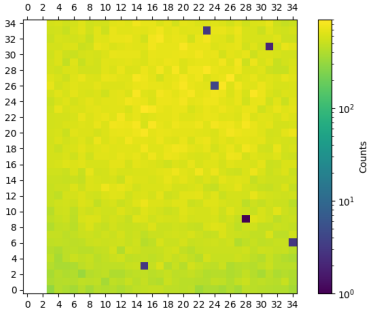
Amanda Steinhebel

AstroPix v3 Results

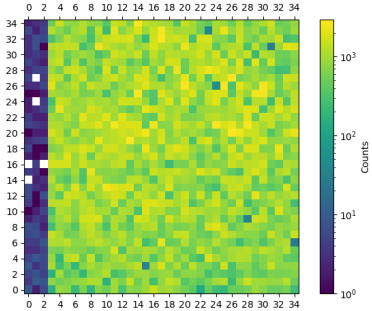
Source Scan Measurements

- Ba133, 30min, ~8 nCi
- Am241, 10min, ~106 nCi
- 200 mV threshold, delta(TS)<=1
- First 3 cols (PMOS) disabled
- Ba133, 5min, ~8 nCi, enabling PMOS amplifier col
  - higher hit rate in PMOS cols

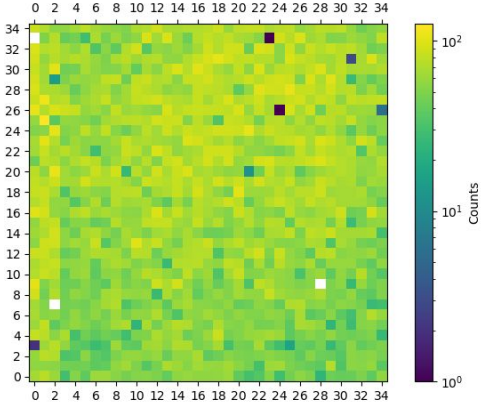
Ba133 - 93.6% of hits paired

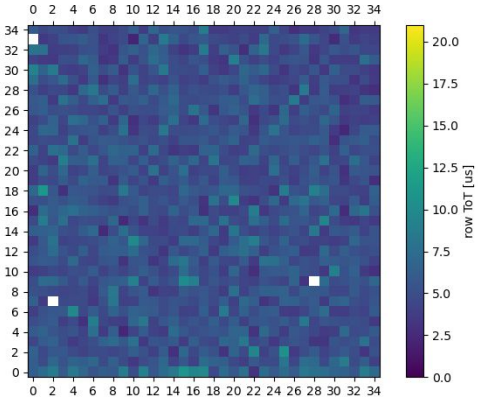


Am241 - 82.1%% of hits paired

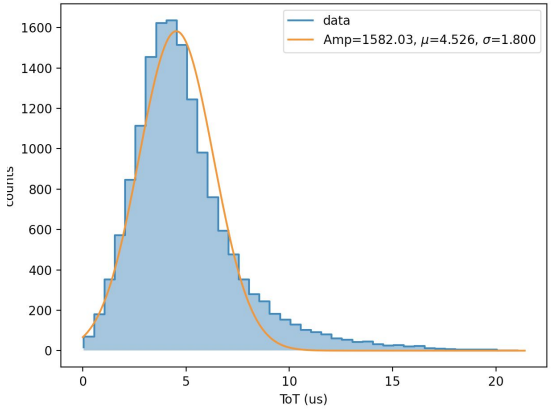


Ba133

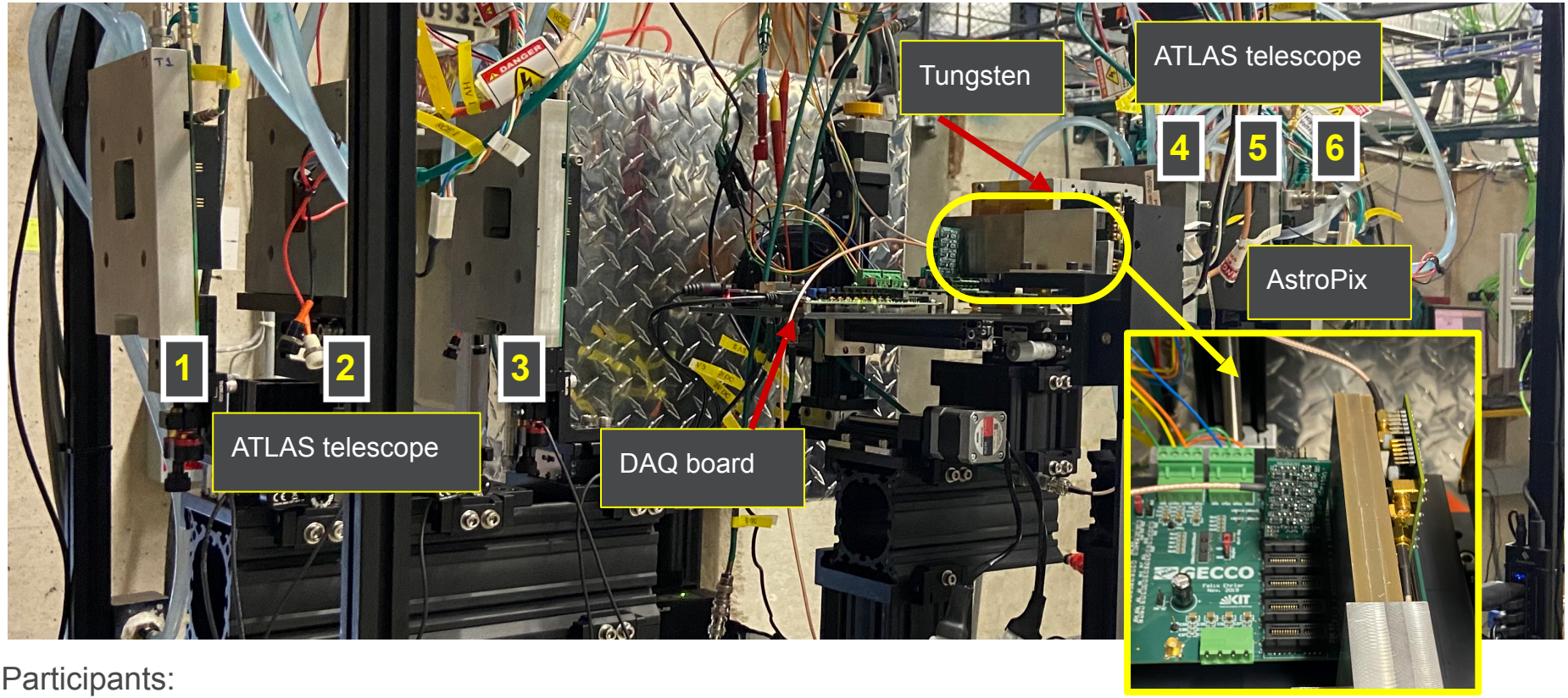




Mean ToT distribution



AstroPix v3 TestBeam



Participants:
Jihee Kim, Maria Zurek, Manoj Jadhav, Jessica Metcalfe

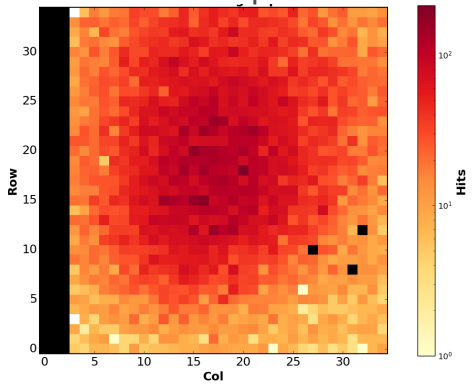
AstroPix v3 TestBeam Results

120 GeV Proton Low intensity beam

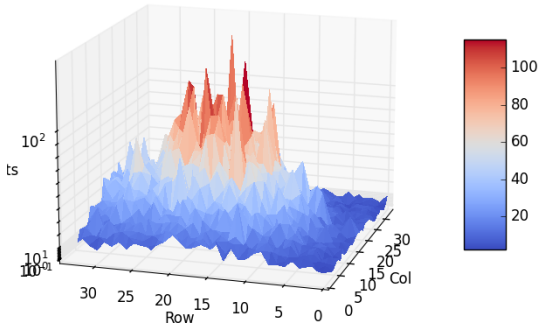
- 120 GeV Proton
  - 5000 protons/spill
  - 4.7 mm × 4.8 mm beam spot
- Data acquisition
  - Total 8 hours
  - 300 mV threshold
  - HV bias voltage 150 V
- Total 37,472 raw events
  - 96.67 % of events were decodable
  - 44,742 pixels* were fired
  - Among 91.1 % of active pixels, 91.02 % of pixels were fired
- Uniform pixel response for Minimum Ionizing Particle

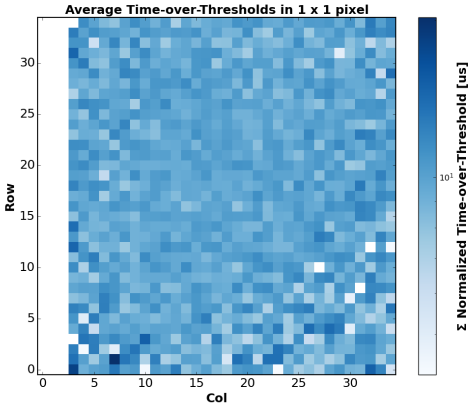
*Matching hits with exact time timestamp + ToT matching

Hit map

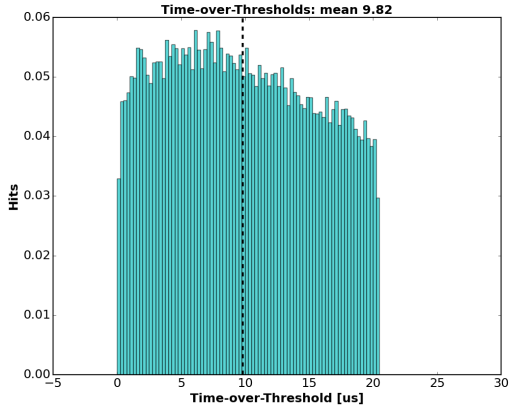


Hit map 3D





Average ToT in Pixel array

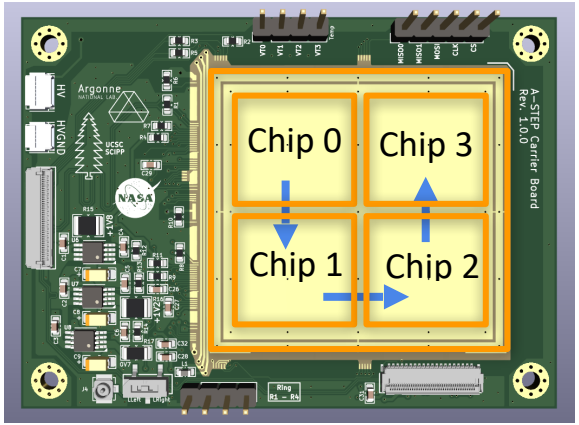


ToT distribution

Ongoing Tasks

- Depletion depth measurements are ongoing.
  - TCT data collected by Amanda with the help of UCSC colleagues
- Irradiated AstroPix v3 with different 400 MeV Proton dose
  - Data analysis and sensor characterization of irradiated samples
- AstroPix v3 quad-chip development
  - Testing the first iteration of a carrier board

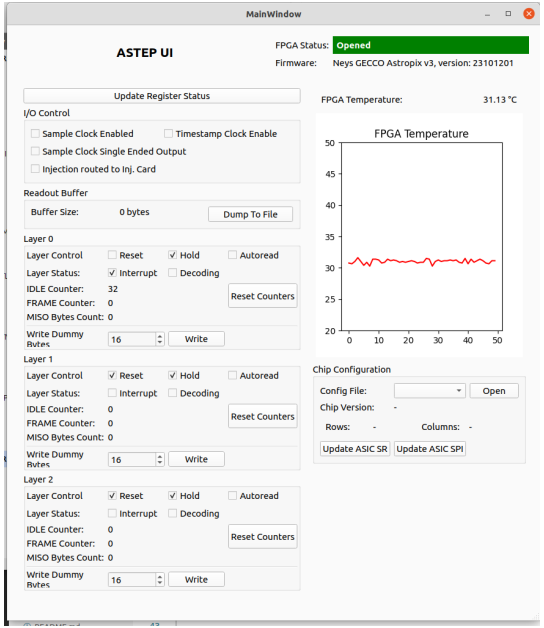
AstroPix v3 quad-chip carrier board
- Demonstrate required services
- Daisy chaining



FW-SW Development for Quad Chip layers

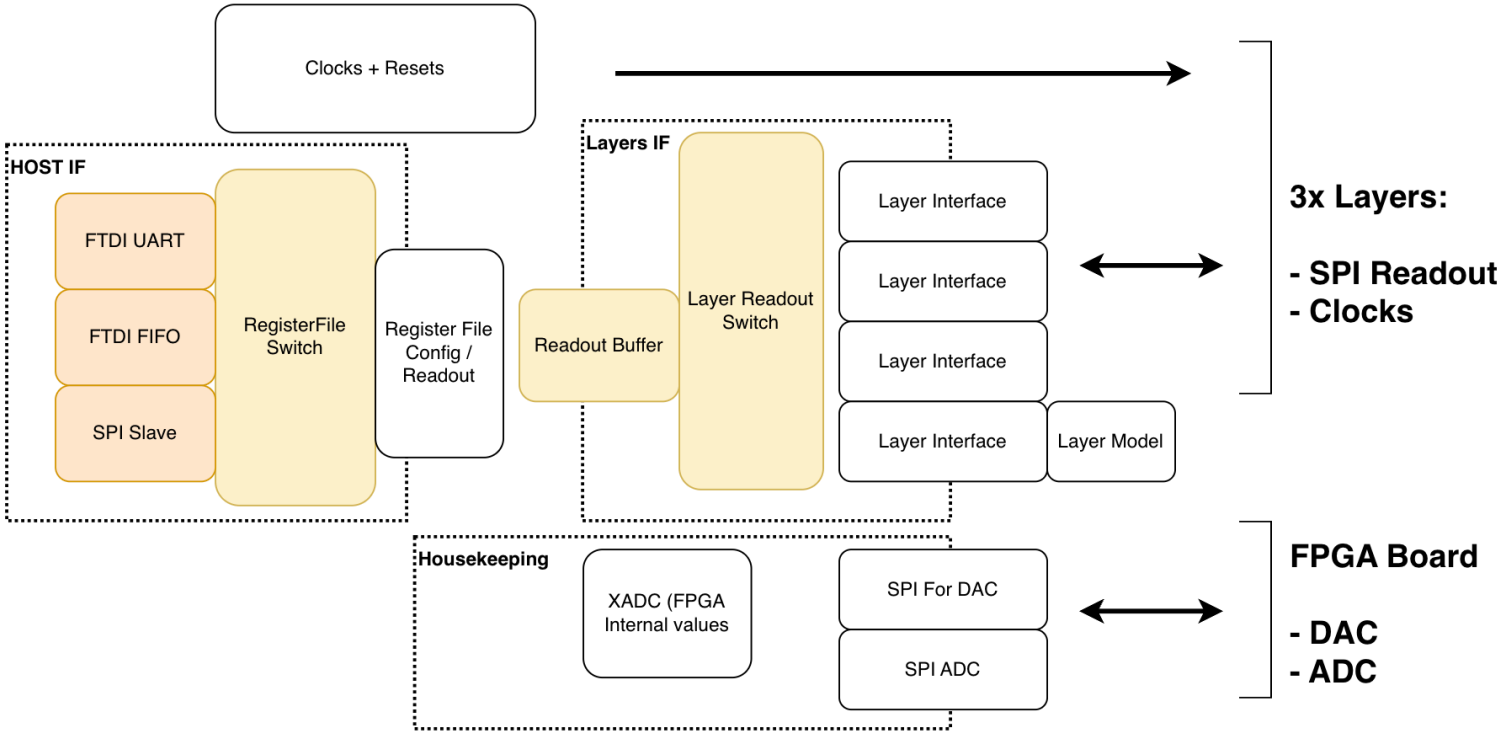
New FW for quad-chip layers

- FW-driven SPI readout to reduce deadtime
  - The self-trigger readout when there is data in buffers without SW check
  - Sensor data frame detection, IDLE discard, Tagging/ reframing, routing to single Readout Buffer
- FW Scale-ability
  - Read through the daisy chain in FW rather than SW
  - Up to 20 daisy-chained SPI inputs have their own interfaces, which feed into the global buffer
- SW speedup to match FW
  - Reduce the chance of incomplete data return
  - Speed-up in analysis scripts, esp. when probing every pixel individually



https://github.com/AstroPix/astep-fw

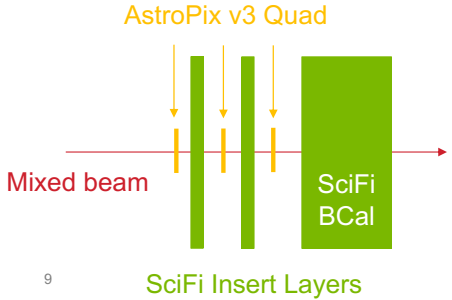
FW-SW Development for Quad Chip layers

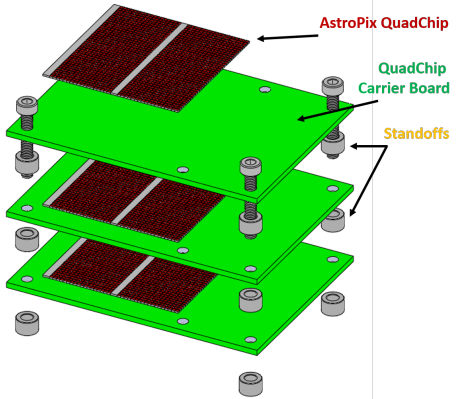


https://astropix.github.io/astep-fw/fw/architecture/

Future Tasks

- AstroPix v3 quad-chip carrier board upgrade
- Multilayer AstroPix integration with quad chipboard
- V4 chip testing
  - Energy resolution
  - Tuning and Calibration
  - Dynamic range studies
  - Depletion depth measurement
  - Irradiation and SEE testing
- Module-like PCB board design with 9 single chips
- Integration with SciFi BCal



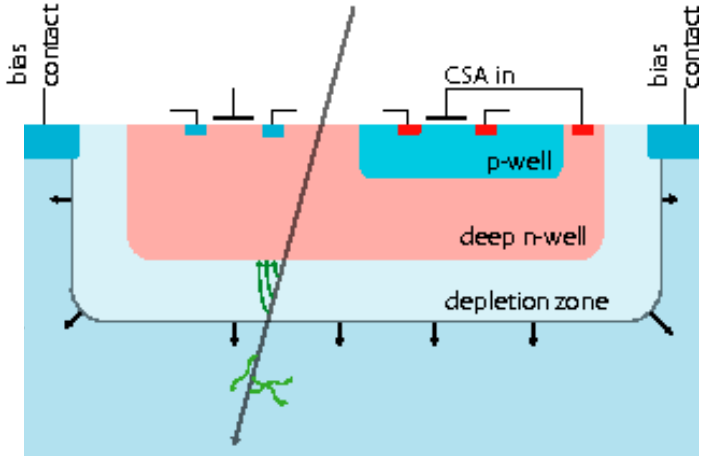


Thank you

AstroPix

HV-CMOS Monolithic Active Pixel Sensor (MAPS):

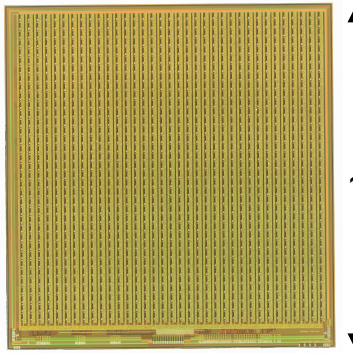
- Combination of silicon pixel and front-end ASIC
- On-pixel charge amplification and digitization
- The technology uses more typical CMOS wafer processing for cost-effective mass production
- Fabrication on a single wafer enables a shorter design cycle
- No need to bump-bond to each pixel - improves yield



AstroPix (based on **ATLASPix3** **arXiv:2109.13409**)

- 180 nm HV-CMOS MAPS sensor
  designed at KIT (also designed ATLASPix, MuPix, etc.)
- Developed for AMEGO-X GSFC/NASA mission
  (Upgrade to the Fermi's LAT)

AstroPix v3 (Under test)



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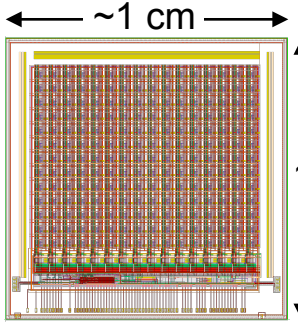
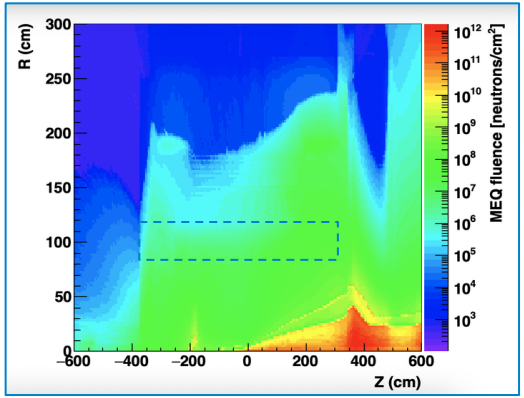


AstroPix v4
(Ready to test,
Nicolas' Talk)

AstroPix v3 Iradiation

- IV and CV measurements performed for the v2/v3 chips before irradiations
  - Same measurements will be repeated post irradiation
- 9 v2 & 6 v3 chips irradiated for Passive Irradiation (Al-foil dosimetry)
- Active Irradiation for Latch-up (and SEE) is planned - week of 26th May

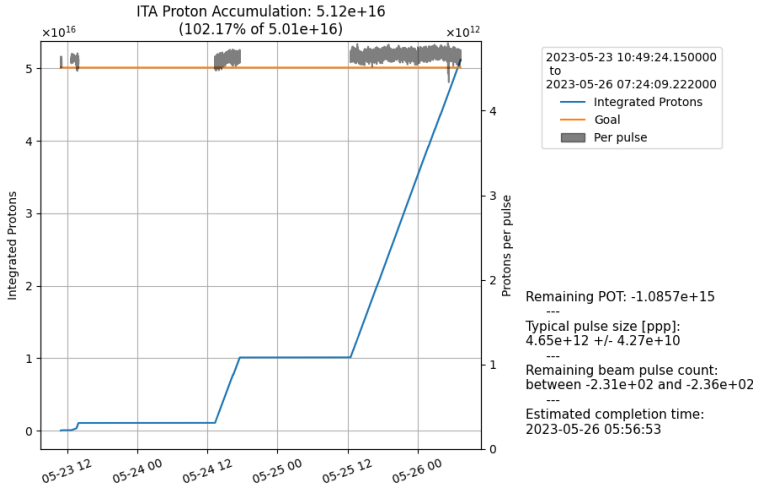


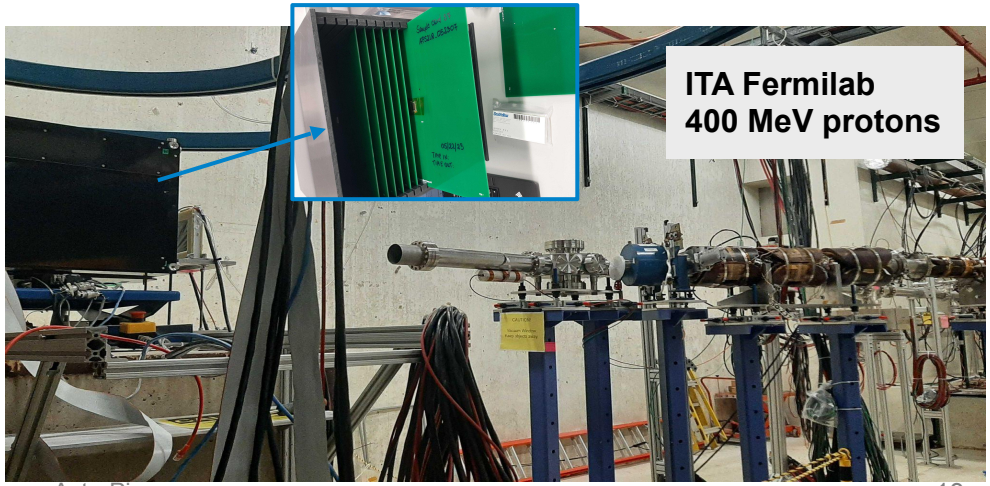
V2 Irradiation

Nb of samples	Doses (400 MeV protons)
3	4.50E+13
3	1.08E+15
2	1.01E+16
1	5.02E+16

V3 Irradiation (low and high ResChips)

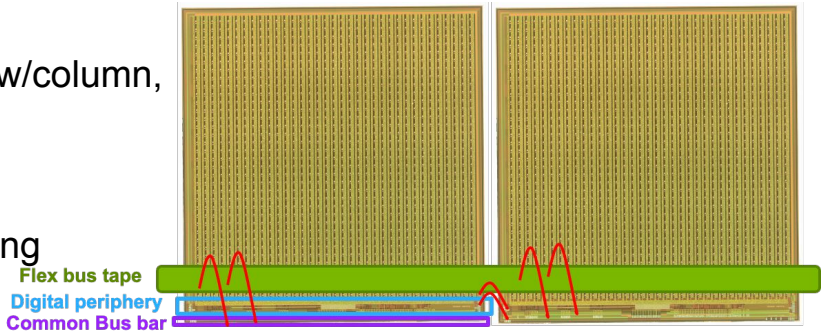
Nb of samples	Doses (400 MeV protons)
2	4.50E+13
1	5.04E+15

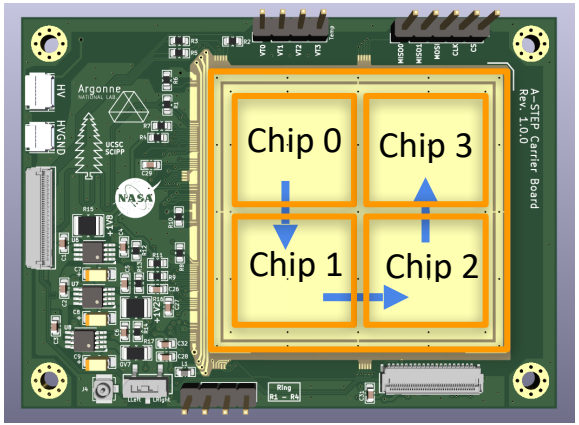




AstroPix Readout

- 10 bytes of data per hit - header (chipID, payload), row/column, timestamp, ToT
- SPI I/O daisy chained - chip-to-chip signal transfer
  - signals are digitized and routed out to the neighboring chip using 5 SPI lines via wire bond
- Power/Logic I/O distribution on the module (through a bus tape)
  - 4 power lines (LV, HV), ~20 Logic I/O (SPI, clk, timestamp, interrupt, digital Injection, etc.)
  - HV, VDDA/VDDD(1.8V), VSSA(1.2V), Vminuspix(0.7V)
  - power distribution can be controlled using voltage regulators
  - mostly part of the end of the stave services
- Data will be received by FPGA at the end of the stave
  - FPGA aggregates data before sending off-detector
- Low heat load at chip, only cooling of end of the stave card
- The operational temperature for AstroPix is at room temperature and considered to be operated at 22 °C



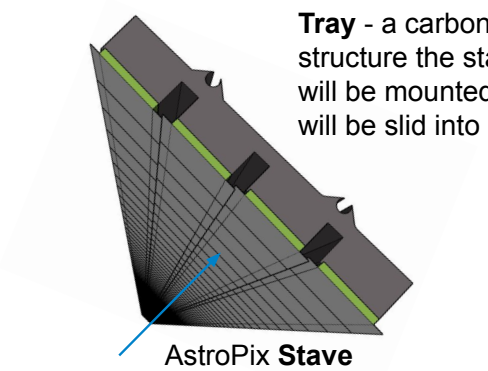


AstroPix v3 quad-chip carrier board
- Demonstrate required services
- Daisy chaining

AstroPix Assembly

AstroPix v5 (Production version)

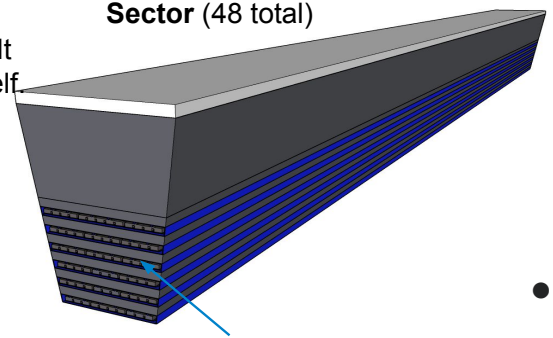
- Full size chip - 2 × 2 cm², pixel pitch 500 µm,
- 35 × 35 pixel matrix → 1225 hit buffers
- Fix any bug from v4



Tray - a carbon fiber structure the staves will be mounted on. It will be slid into a shelf.

AstroPix **Stave**
Consists of 1 x 108 chips with the support structure, "turbofanned"
AstroPix **Module**
Subset of chips

Sector (48 total)



Shelf - a carbon fiber structure that is glued to the Pb/ScFi layers, that we will slide trays with AstroPix staves on.

*The designs presented on these slides are not final but for illustration only

Module Strategy

- QC testing with wafer probing + Module and stave level QC testing and tuning
- "Baseline" model of Modules on Stave
  - Module - 8 single chips
  - Stave - 13 Modules - 104 chips
  - 12 or 14 Staves per AstroPix layer per Calorimeter Sector
  - Total 249600 chips
- All staves are identical and get combined in a separate production step
- Data is transmitted to the end of the Stave card using flex base tape
- Institutions - ANL, GSFC/NASA, KIT, UCSC, Korea, Oklahoma State

AstroPix Timeline and Production

v3 full size chip (ongoing testing)

- Test bench characterization (ongoing)
- Testbeam performance studies
- Active and passive irradiation **~10^{15} $n_{equivalent}/cm^2$**
- **Quad-chip readout (ready to test)** for NASA's hosted payload mission (A-Step) - **January 2025**
- Integration with Pb/SciFi - FY2024 **(Henry's talk)**

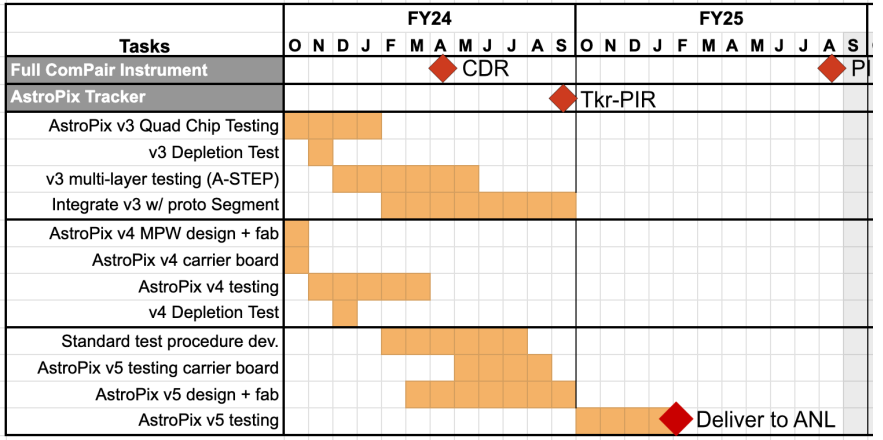
v4 new features for better performance (MWP)

- **Final design version**, smaller chip (1cm × 1cm)
- Fabricated wafers **delivered last week**
- Chip carrier board design for bench test is ready for the PCB fabrication

v5 full size final chip

- Fix any bugs from v4
- v5 chips available **November 2024**

GSFC/NASA ComPair-2 AstroPix timeline



BIC@ePIC Timeline

- **Prototype R&D** (v3) Ongoing - till Nov 24
- Pre-Production (v5) chips starts **Nov 2024**

(More info in Maria's talk)

Production

- Fabrication by TSI - with a large production order, AMS is a backup