Updates on BTOF ASIC – Discussion with Designer

- What can be the dead time?
  - O(100 us) frontend, Streaming Readout
    - how and how many chips will share data lines (motivation is to reduce number of traces on flexible module hybrid PCB)
    - Daisy chain vs mater/slave vs token => discussion with ASIC designers needed
    - How deep is needed for the on-chip memory => simulation study needed
- What is the data rate needed : GB/s
- BTOF: 1 Mb/s
  - 1Mb/s is an overestimate: 30 Hz/channel*128 channels*50b/hit= O(200kb/s) per chip
- In the google doc we have "Output format: include 14b Chip ID, 12b BCID, and 7b channel ID+12b TDC+10b ADC per hit ", could you break down each of them why those numbers are needed?
- 11b BCID: 1160 bunches in EIC, $2^{11}=2048$
- 6b Chip ID: 128 chips on a stave, read out from both ends (128/2=64), $2^6=64$
  - Subject to change depending on BTOF detector design, i.e. how many chips will share the data lines on a stave
- 7b channel ID: $2^7=128$
- 8b TDC: (1/98.5MHz) / (20 ps) = 508, so $2^8=512$
- 10b ADC: AC-LGAD S/N~40, $1/2^8$ equivalent bit ADC resolution is 0.4% = 1/6 * (N/S), 10 bits
  - ~10% might be sufficient already => can check the test beam data and simulation (smearing)
  - Would TOT instead of ADC work => can check ETROC2 TOT versus Q_{inj}

Schedule of Sensors and ASICs
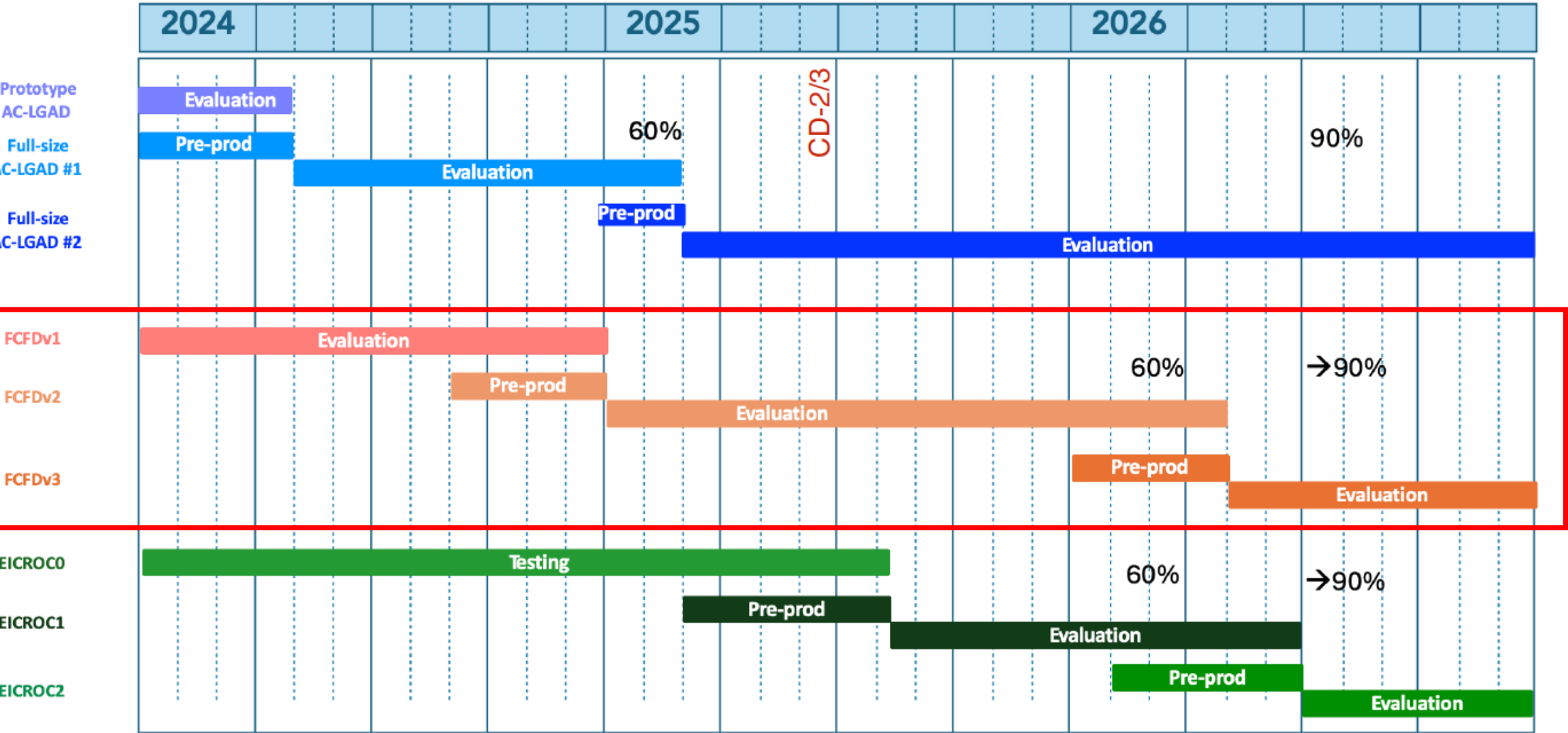
Schedule of Sensors and ASICs
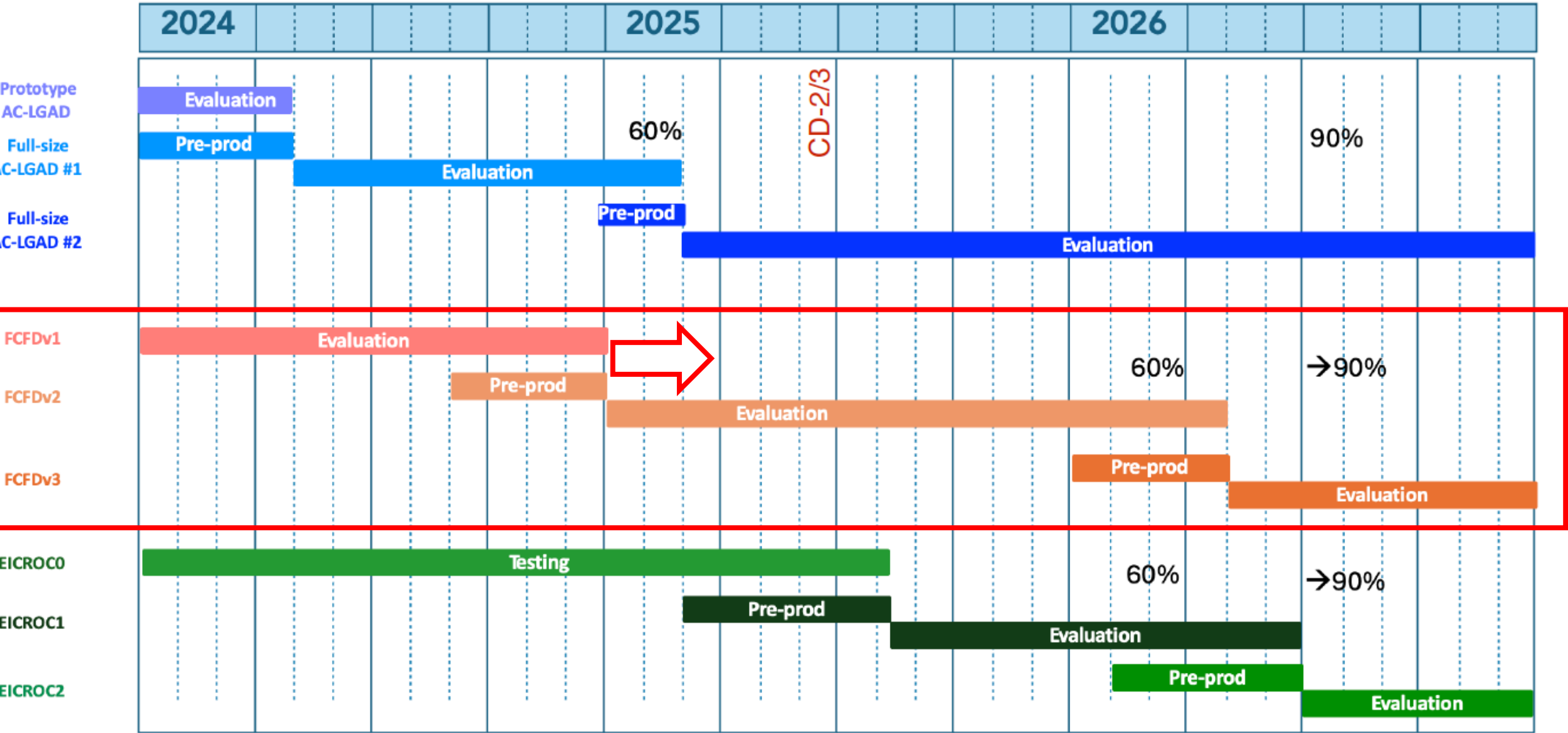
PED Request – LBL&FNAL

- FCFDv1 submitted last September, received at FNAL this February

  - Passed initial smoke (power-on) test

- PED request to support EE efforts at LBL to work with Fermilab FCFD design team on

  - Design test systems for FCFDv1

  - Conduct tests on FCFDv1 in lab and test beam

  - Provide feedbacks to the FCFD design team for FCFDv2 design

  - Evaluate FCFD with the EPIC ppRDO prototype board