News – 2/27/2024

- **EIC Project Detector R&D**
  - **FY24 plan (p2);** contracting in progress, mid-year report due Feb 29, 2024
  - Detector R&D Day on March 25, 2024, Detector R&D annual review in August 2024 with deadline for submission July 1, 2024

- **ePIC TOF Project Engineering Design**
  - Mechanical engineering on support structure and cooling: Mechanical PED
  - BTOF (and FTOF?) module prototyping in preparation

- **ePIC TOF Simulation**
  - TOF geometry: Zhenyu updated TOF according to latest geometry database in DD4HEP #564 Wei: will update the FTOF design
  - TOF in tracking – Nicolas et al.: re-check FTOF material budget impact
  - TOF PID reconstruction – Oskar et al.: TOF reconstruction, validation plots, and PID LUT
  - TOF digitization – Souvik/Adam: charge sharing and detector noise
  - TOF service in simulation – TBD: implement the missing material for mechanical support structure, cooling and cabling

- **ePIC TOF DSC**
  - Working with CAMs to understand/update the TOF cost and schedule – in-kind contributions and FTOF labor spreadsheet
  - **Reform TOF DSC ORG with new leadership team and working group structures (p5)**

- **Upcoming Reviews**
  - Incremental Design and Safety Review on July 5-6, 2023: Presentations; Review report; answers in preparation (p3/4)
  - PDR2 in Summer 2024?; CD2/3 in Winter 2024?
  - **pre-TDR/TDR planning (p6/7):** see Silvia's slides at TIC on Feb 19, PID discussion on Feb 23, **and presentation at TIC on March 4**

AC-LGAD FY24 R&D Proposal

- Optimized sensor design and final prototypes that meet ePIC requirements, including timing and spatial resolution, irradiation tolerance, and reasonably large size for module assembly
- Prototypes of interposer for mechanical/electrical connections between strip sensor and ASIC
- ~~Prototypes of light-weight module mechanical structures for forward TOF~~
- Prototypes of frontend ASICs
- Functional and full size low-mass Kapton PCB
- Low-cost interconnect for sensor-ASIC hybridization
- Service hybrid prototype

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eRD112 (414k->286k$)
- Sensor R&D (346k->261k$)
  - BNL, HPK ~~FBK~~ productions
  - TCAD, lab/beam/irradiation tests
- Sensor/ASIC integration (15k$)
  - Interposer
- ~~Mechanical structure ($53k)~~
  - ~~Light-weight structure w. cooling~~

eRD109 (435k->390k$)
- Frontend ASICs
  - EICROC (85k$)
  - FCFD (40k$)
  - ~~3rd Party ASICs (45k$)~~
- Frontend electronics
  - Low-mass Kapton PCB (30k$)
  - Low-cost hybridization (15k)
  - Service hybrid (220k)

EPIC Simulation
- Geometry model, digitization and reconstruction
- Requirements on spatial, timing resolutions, and material budget

Project Engineering Design
- Engineering design for pre-TDR
- Integration & services

Sensor   **Electronics**   **Sensor-ASIC integration**   **Mechanics**

News

- **Incremental Design and Safety Review on ePIC PID detectors conducted on July 5-6:** Review [presentations](); Final review [report]()

Detector

- (AC-LGAD) 35ps Barrel/ 25ps FW timing resolution seems to be almost the best performance without safety margin. Under these circumstances, a bias voltage scheme should be more flexible than only one pair of cables for each board, because the temperature gradient and the position-dependent radiation fluence require different operation voltages.

- (AC-LGAD) The type of interconnection to the sensors (like wire bonding or bump bonding) must be clearly specified. If a detector uses a bump bonding connection, we would advise to start testing the flip-chipping process since it takes longer to develop a stable procedure.

  ✓ Fluence: Wei/Xiao
  - Power for Service Hybrid: Tonko/Wei
  - Thermal: Yi/Andy

  - eRD109: ORNL
  - eRD112: UCSC/UIC

Electronics

- The initial requirements for the EICROC were specified mostly for the Roman Pot detector and not for all detectors which use EICROC. We advise summarizing the requirements for all detectors and making a single EICROC specification before submitting further prototype chips.

- A specification on the tolerable clock drift and the robustness to phase irregularities should be defined and will help to ensure that these parameters are measured and controlled in the architecture from the beginning of the design phase. The DAQ design should include a backup solution for a directly distributed clock to the RDO boards to provide the clock precision required by each subsystem.

  - BTOF: Draft
  - FTOF: ?

  ✓ Tonko: 5ps jitter

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News

- **Incremental Design and Safety Review on ePIC PID detectors conducted on July 5-6:** Review [presentations](); Final review [report]()

Tracking

- Recent progress has been made in ePIC's cross-cutting PID WG to understand tracking requirements for PID detectors. Requirements documents should capture the bi-directional interface between tracking and PID detectors: e.g., translation between extrapolated track impact point and angle resolution requirements for PID detectors. It could be evaluated where the PID subdetectors can contribute to improving the tracking performance and how in the reconstruction algorithms this could be integrated.

- Encouraging track momentum resolution improvement was achieved by including the AC-LGAD in reconstruction. The reviewers suggest extending this study to understand the impact on the extrapolated track impact point and angle at the radius of the DIRC.

Recommendations

1. Capture the bi-directional interface between tracking and PID detectors: e.g., translation between position and angular resolution requirements for PID detectors.

- ZY: (recommendation)

- Nicholas (NCU?)

- ZY: [draft]()

The Request

Dear DSLs,

Following what has already been communicated at the ePIC collaboration meeting (Jan 9-13, 2024), the DSLs are requested to prepare a TDR plan for their subsystem for calendar year 2024, including:

• The lab/testbeam/prototyping needed;

• The further progress needed for the reconstruction software;

• The verification of the implementation of the detector and detector response in simulation and validation using information from lab/testbeam exercises or from literature;

• The studies required to demonstrate the detector performance;

• The required engineering design;

• The needed resources to achieve 60% (CD-2) and 90% (CD-3) design completion;

• The plan should include the time required to draft the text for the pre-TDR (CD-2) and TDR (CD-3).

The plan should present the activities required month by month in order to allow progress to be monitored. The ultimate goal of this exercise should be 90% design completion consistent with the requirements of the TDR and CD-3, indicatively by the end of 2024. We recognize that the available time is limited. Therefore, please make an educated selection of the most essential studies doable within the available time.

We understand that a planning exercise like this will identify shortcoming in workforce and resources. Those shortcomings should be clearly identified so everyone is aware and we can work together to address them.

The plans will be presented at dedicated CC WG meetings, to be organized by the CC WG conveners over the next few weeks. The CC WG conveners will be asked to report on the status of the planning at the TIC meeting on Monday Feb. 19.

Thank you,

Silvia, John, Oskar, Matt, Prakha

component	Current status	R&D	PED	Beam Test	60%	90%
Sensors	prototyping: 1st HPK prototype tested; 2nd HPK production in prep.; 1st FBK prototype in prep.	eRD112 FY22 eRD112 FY23 eRD112 FY24-26		2022, 2023, 2024	FY25 Q2 (2nd HPK)	FY26 (3rd HPK)
ASIC	Prototyping: FCFDv0 and FCFDv1 for BTOF, EICROC0 for FTOF	eRD109 FY23 eRD109 FY24-26		2024	FY25 Q2 (FCFDv1,EICROC1)	FY26 (FCFDv3, EICROC2)
Module Flex PCB	Prototyping: long PCB	eRD109 FY23 eRD109 FY24	2026	2025-	FY24 Q4 (M2M, M2SH)	FY26 (full-length integration)
Module CF structure	Prototyping: BTOF stave produced, thermal simulation underway	eRD112 FY23			FY25 Q2 (full-length stave)	FY26
Module Assembly	Prototyping: Sensor/ASIC integration, Interposer	eRD109 FY24 eRD112 FY24	In prep.	2025-	Thermo-mechanic prototype FY24	Fully functional module FY26
Global support structure, Cooling	Conceptual design		Active		FY25 Q2 (1/12 with staves)	FY26 Q1 (1/12 FTOF wedge)
Service Hybrid	Prototyping: board layout	eRD109 FY24		2025-	FY25 Q1 (with ETROC2)	FY26 (final layout & ASIC)
Backendelectronics, Power supplies	Possible PS models identified	N/A	N/A		Design in FY24 (with project)	Purchase/test one in FY25
Software and simulations	Geometry and material in DD4HEP, have TOF PID, tracking δp	N/A	N/A	N/A	PID LUT in global framework in FY24	Refined material and responses in FY26

Critical Paths and additional Resource requirements

- FCFD ASIC development and testing for BTOF (FNAL+LBL PED?)
- BTOF+FTOF module assembly (UCSC+ORNL+Purdue PED?)
- Long Flexible Print Circuit Board for BTOF staves (ORNL+Nara+RIKEN)
- Software+simulation:
  detector response + realistic material (additional institutions?)

Strategy for the TDR (ASIC)

- BTOF digital block demonstration is in need (a concern)
  - It is important to show that "we can't show it now, but we will definitely be able to do it shortly"
  - It is necessary to fully understand and demonstrate the individual characteristics in pre-TDR
    - Characteristics of sensor, FCFD's analog block, and the combined performance
  - The FTOF study will help to corroborate the story
    - Successful signal readout of FTOF means "complete understanding of the AC-LAGD → analog → digital chain"
    - This knowledge shows that we have the technology to extend analog blocks to digital blocks while keeping a good timing resolution
  - Investigating the availability of other ASICs (e.g. HGCROC) is also important

- The beam test at DESY is scheduled for June
  - It is a good opportunity to show performance of the sensors and ASICs with realistic environment
  - Real MIP beam is mandatory to evaluate realistic performance
  - Before the beam test, the lab tests, e.g. radiation source and IR laser, is necessary
    - Gain uniformity, temperature dependence of gain, timing resolution, spatial resolution, and power consumption

New TOF DSC ORG

Position	Candidate(s)
1 Detector Subsystem Leader	Zhangbu Xu
1 Deputy DSL	Satoshi Yano
2 Detector Subsystem Tech. Coordinators	Mathieu Benoit, Matthew Gignac

- **Leadership Structure**

- **Work packages combining BTOF and FTOF**

1. Sensors (2 coordinators) Simone Mazza, TBC, Japanese colleague

2. Frontend Electronics (all electronics that are on the detector) (2 coordinators)
   Wei Li, TBD

3. Module local integration and assembly (2 coordinators)
   Mathieu/Matthew?, Takashi Hachiya

4. System tests and validation (2 coordinators)
   TBC+TBD

5. Mechanical structure, cooling and global integration (2 coordinator)
   Andy Jung, Yi Yang

6. DAQ & Clock distribution (1 coordinator)
   Tonko Ljubicic

7. Power system, Detector slow control, monitor and safety system (1 coordinator)
   TBC

8. Simulations, software & calibration, Database(1 coordinator)
   TBC