# Er1 High Speed test-chip testing

Initial tests on all 3 modules of the er1 High speed test chip.

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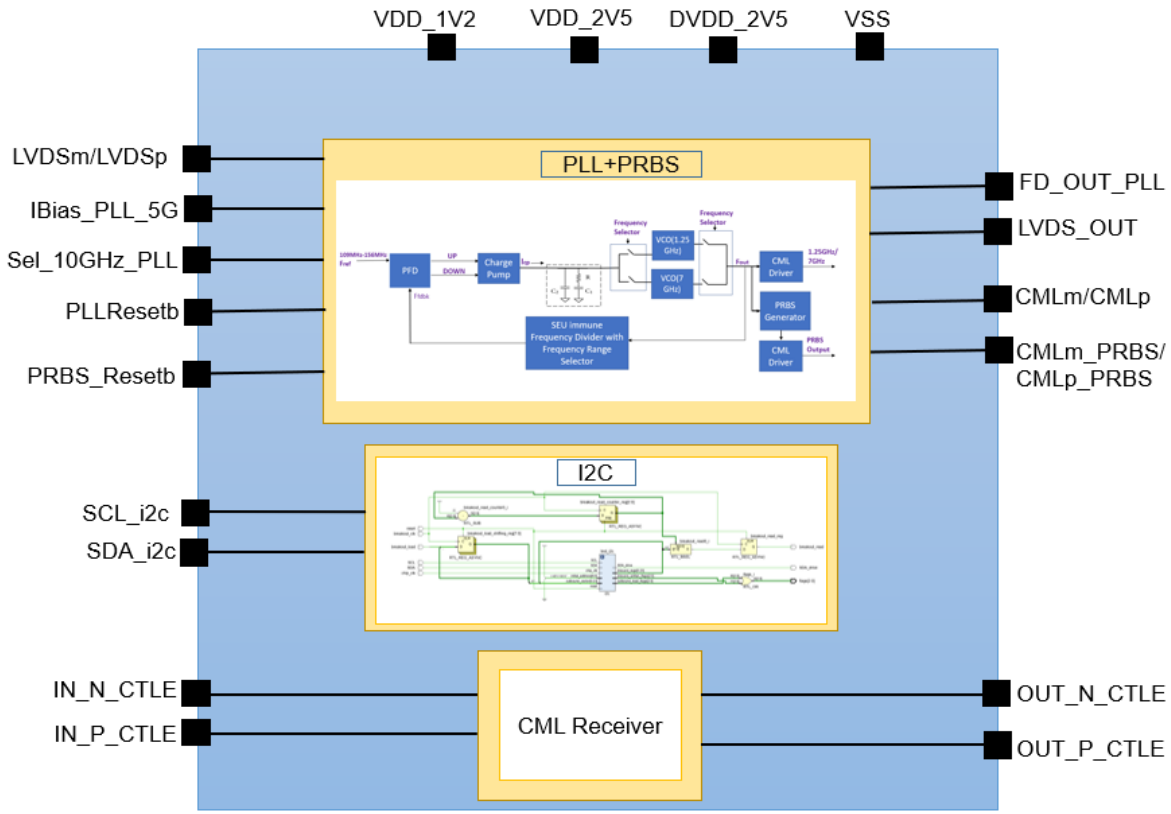
# Introduction

- 3 independent sub-blocks
- Phase locked loop with voltage controlled oscillator.
  - Direct clock output
  - PRBS output
- $I^2C$ module
  - Rad-hard $I^2C$ block test.
  - 3 off $I^2C$ registers.
- Continuous Time Linear Equaliser.
  - Input frequency response boosts signals around Nyquist frequency to compensate for transmission path loss.
  - Regenerates CML output.

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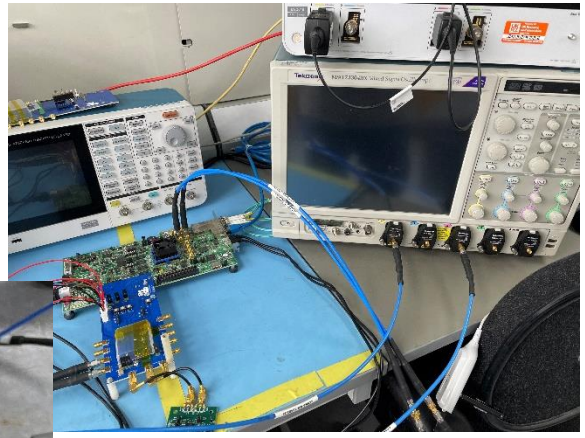
# Test setup

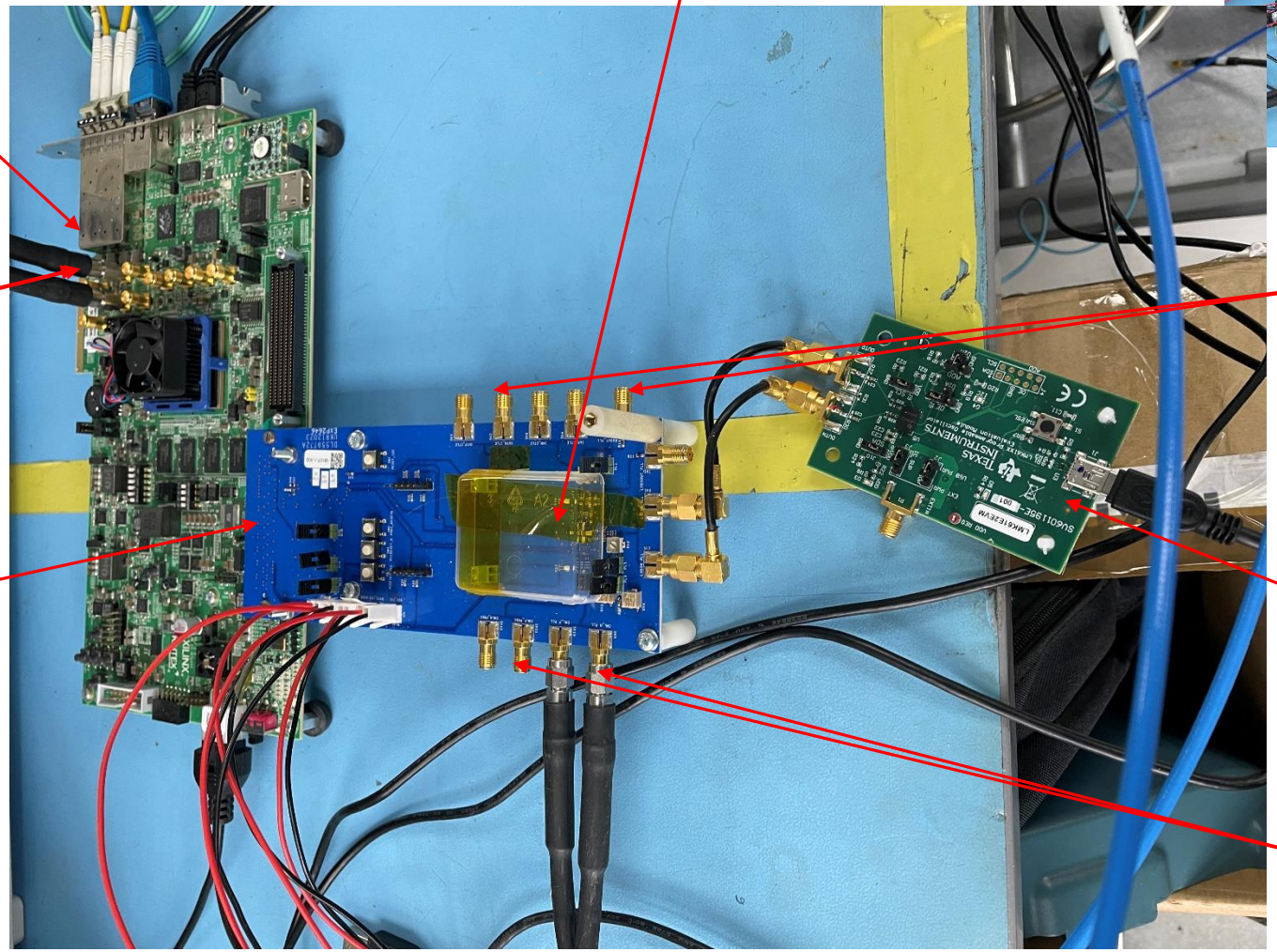
DUT on test board with level translators. Coupling capacitor and termination resistors for differential signals



Xilinx KCU105 dev board.

Can supply Multi Gigabit test patterns via SMA cables

Drives digital control signals and $I^2C$ buses via FMC connector



SMA connections for high speed Current Mode Logic (CML) inputs and outputs to CTLE

LMK61E2 programmable clock chip evaluation board supplies clock to PLL

SMA connections for CML outputs from PLL and PRBS

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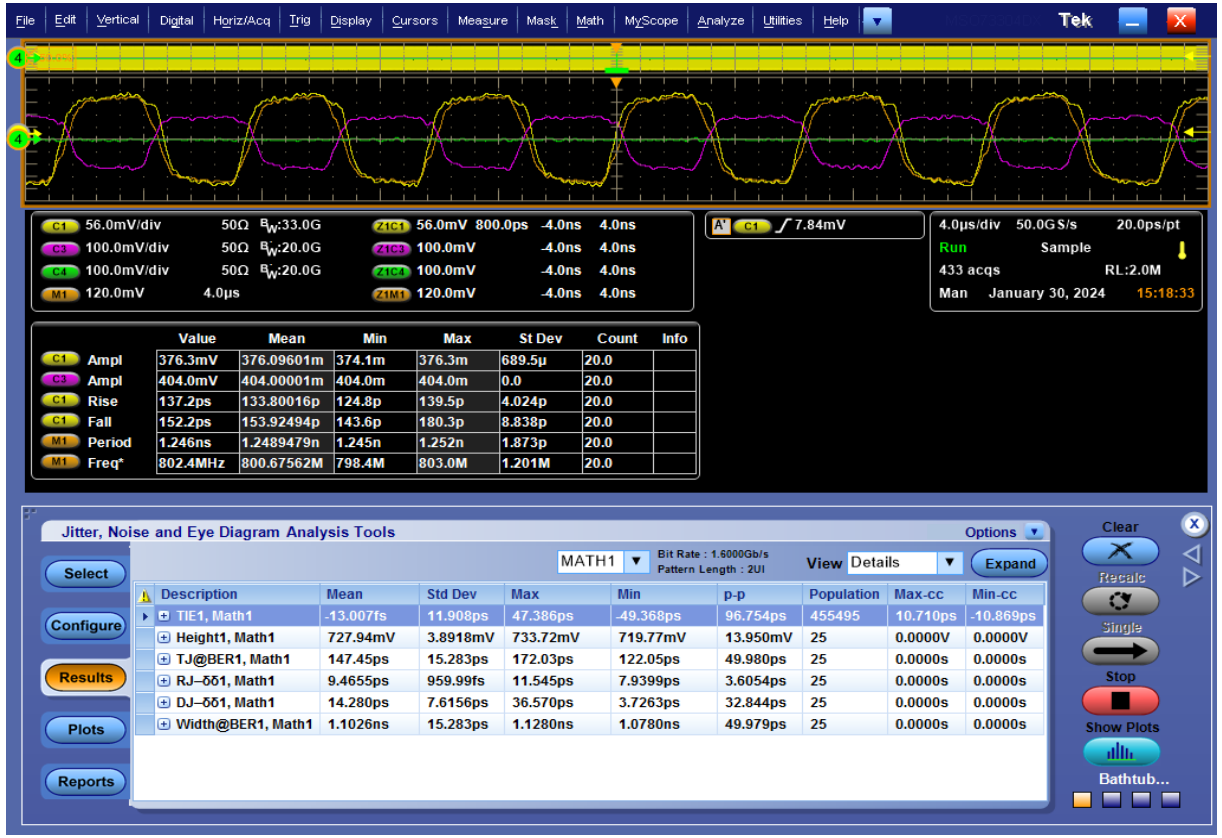
# $I^2C$

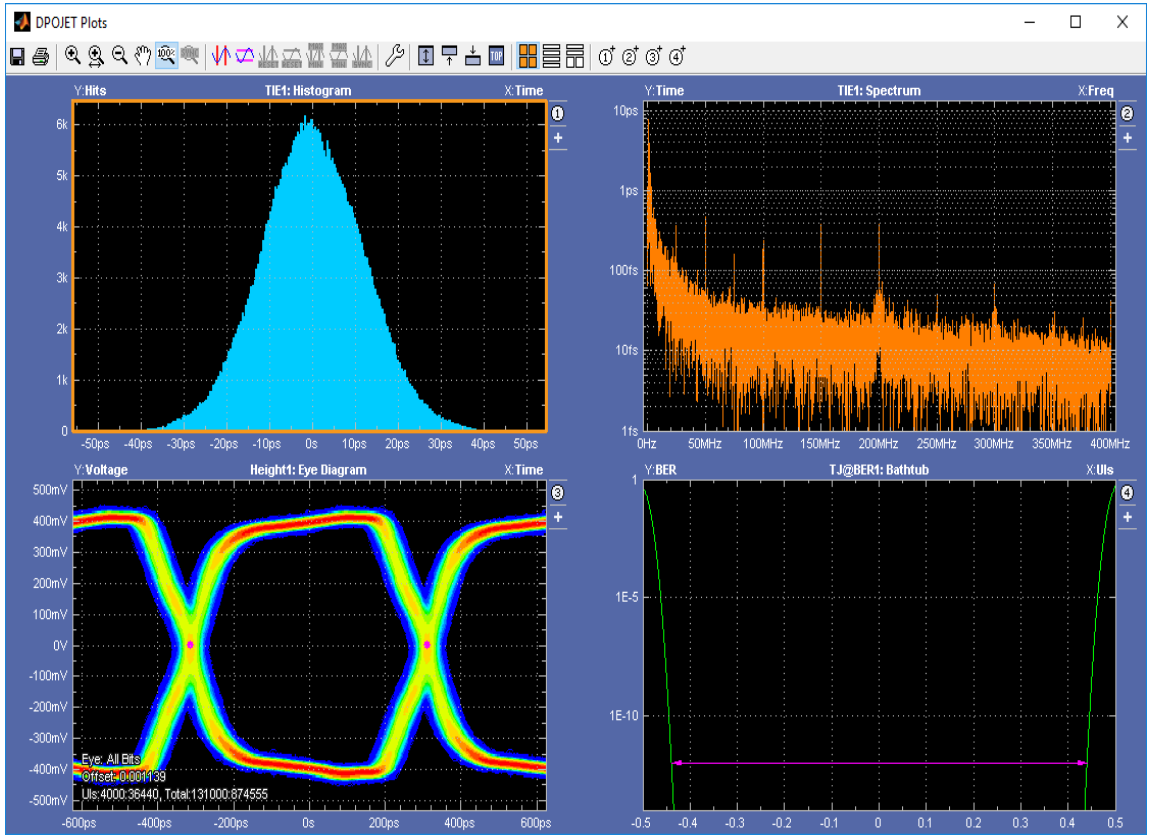
- DUT contains a test instance of a soft $I^2C$ macro.
  - This test instance is configured with 3 registers
  - Writeable (inbound) registers are triplicated with majority voting.
  - 2 of the 3 register addresses allow write and read-back of stored data
  - 3rd register accessible via breakout shift register – not tested yet.
- Xilinx Microblaze soft core processor system on the KCU105 including an $I^2C$ interface.
  - KCU105 design supplies reset and a clock for the DUT.
  - Test program running on Microblaze performs write/read tests
- **Tests Pass OK**.

# PLL and PRBS Tests

- PLL has 2 operating modes
  - Output frequency = 8 x input frequency  800 MHz- 2 GHz
  - Output frequency = 64 x input frequency  5.5 GHz – 7 GHz
- Test setup
  - Microblaze processor system on the KCU105 with GPIO interface.
    - Allows control of mode and reset pins of DUT.
  - PLL input clock is supplied from LMK61E2 evaluation board.
  - CML output signals AC coupled into Tektronix ‘scope
  - Python program on PC controls PLL resets, input frequency, PSU voltage and quantifies output using the ‘scope measurements.

# PLL Tests 100 MHz in 800 MHz Out




- 800 MHz output, full 400 mV amplitude
- Clean eye diagram and bathtub.

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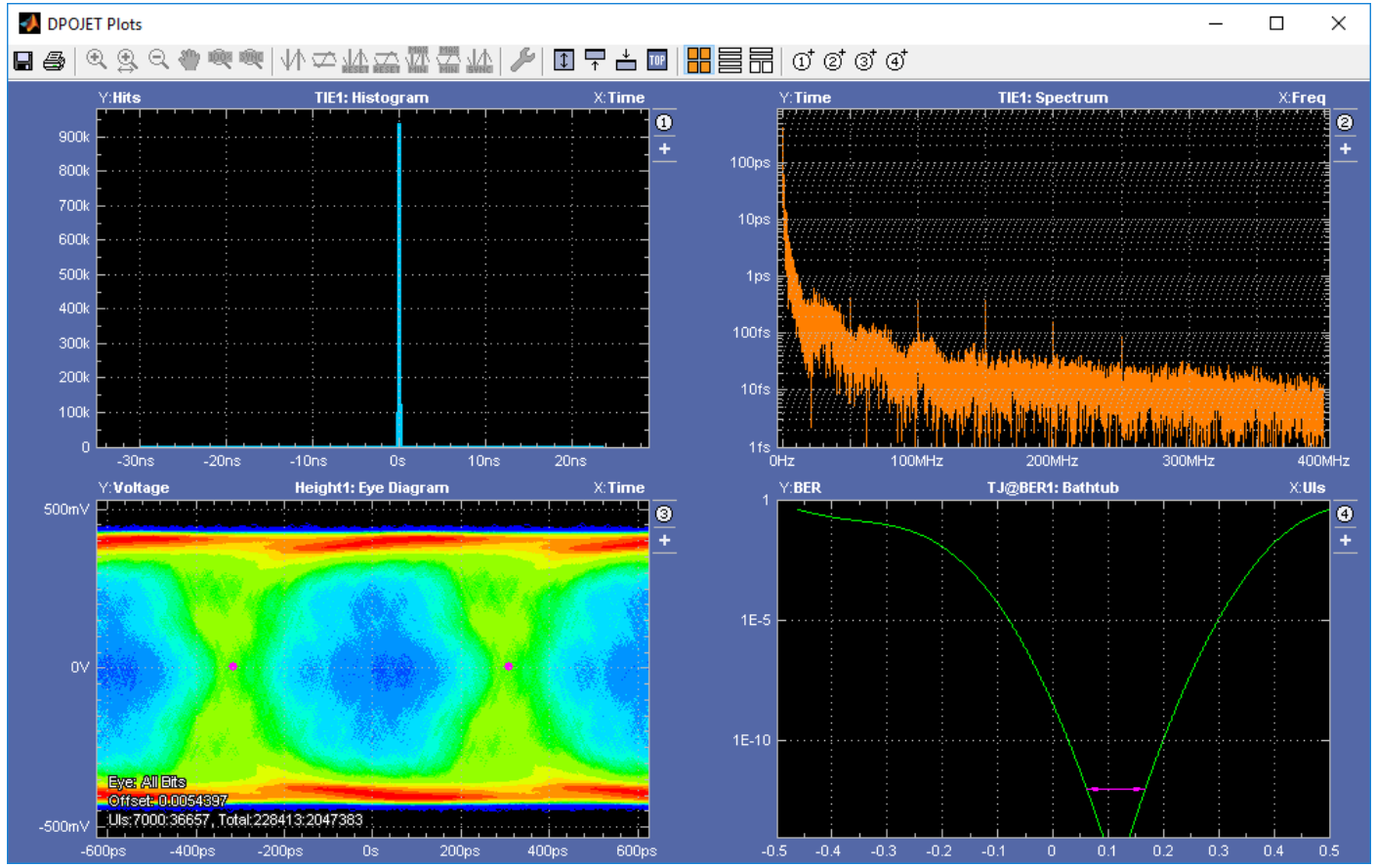
# Enabling the PRBS.




- Viewing Clock output with PRBS enabled.
- Eye diagram jitter is much worse.
- Bathtub narrows.
- Conclude that there is interference (possibly via VDD/GND) from the PRBS to PLL.
- No more test with PRBS enabled.

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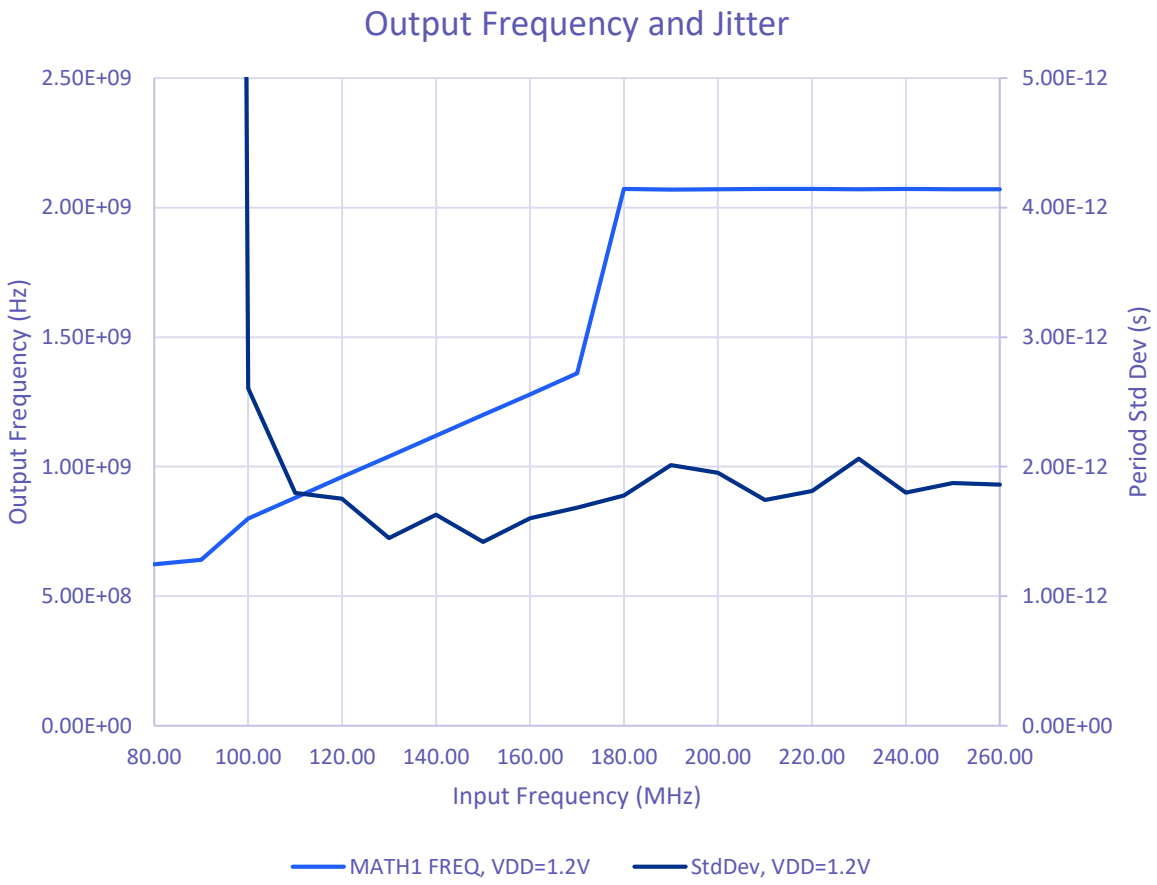
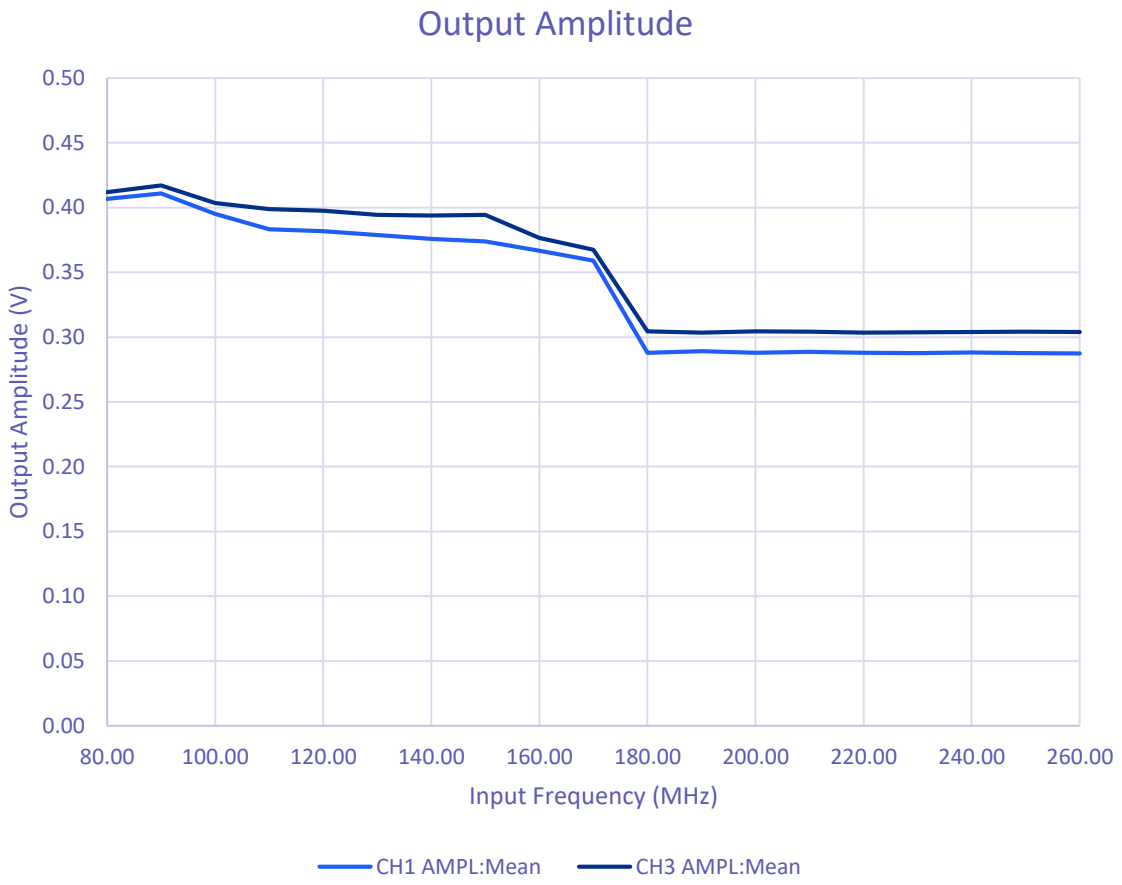
# Automated Frequency Scans, Low speed mode

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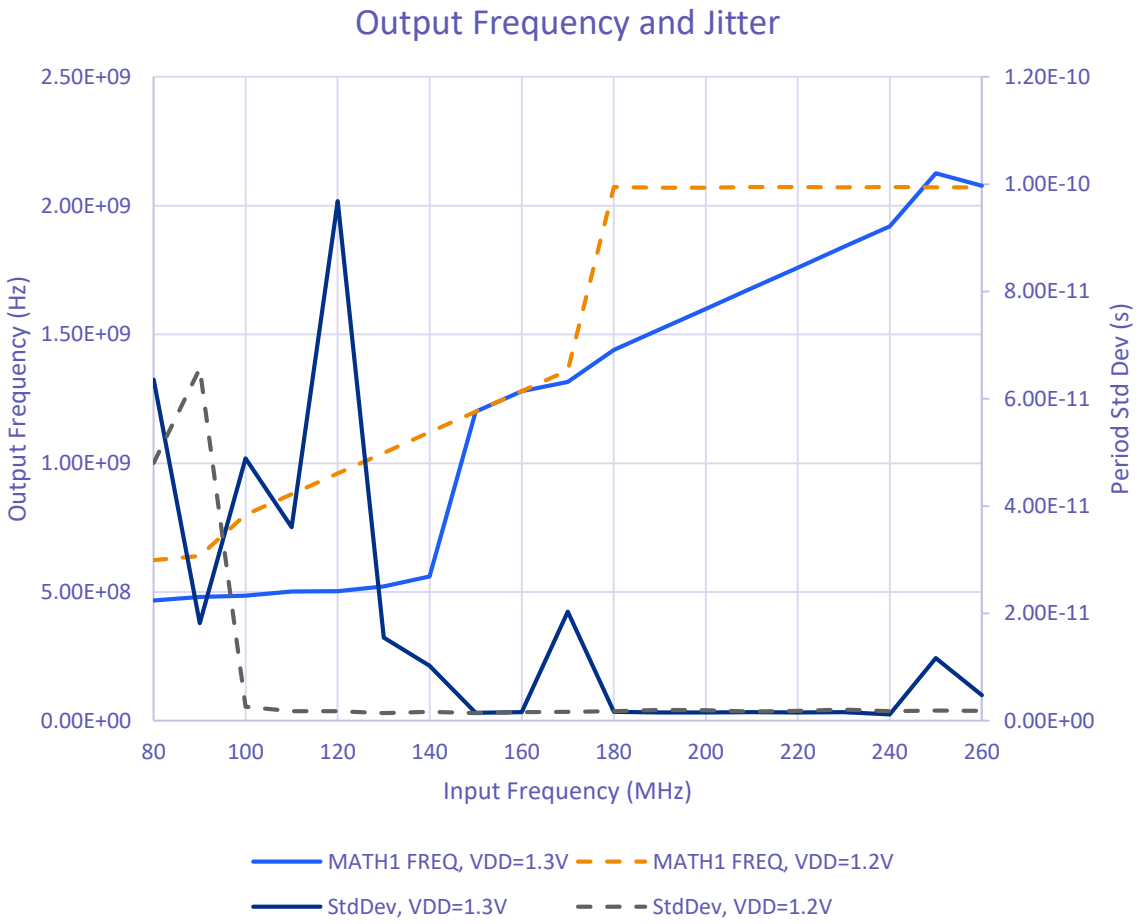
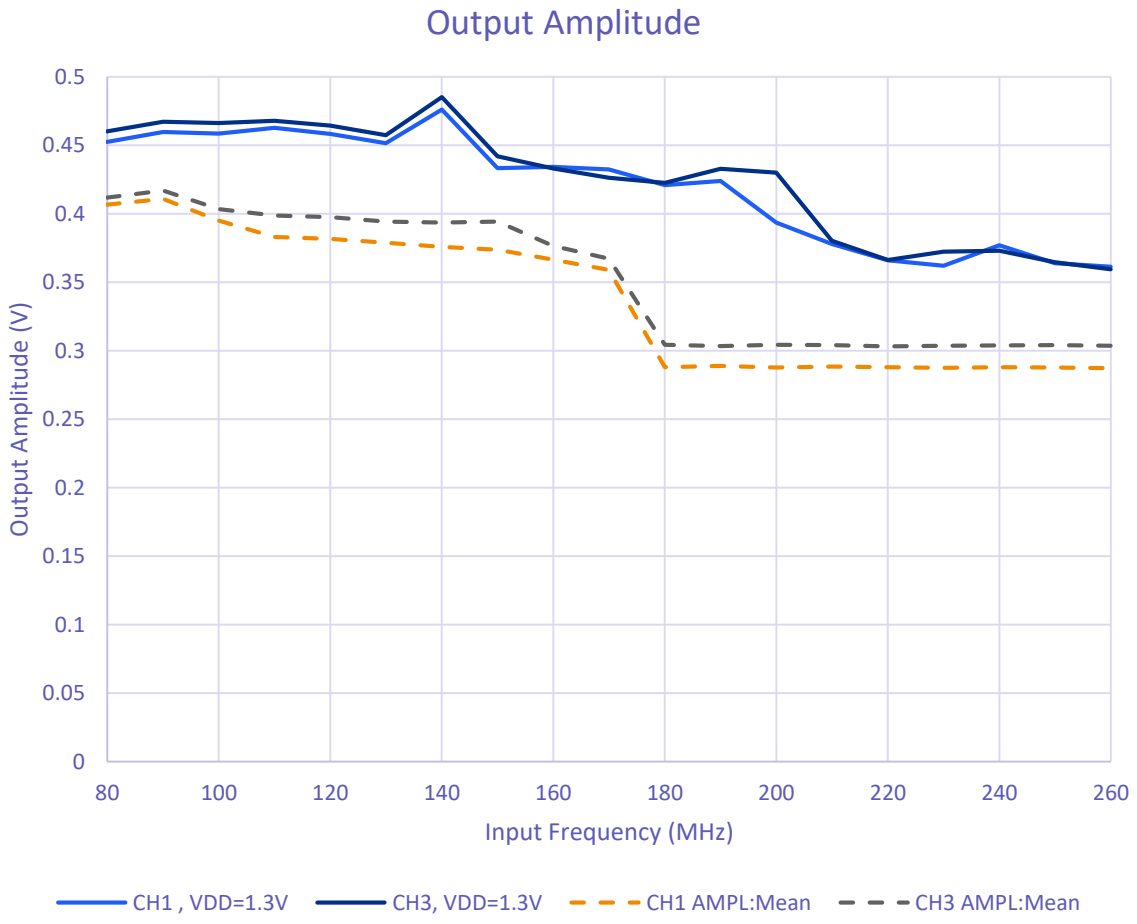
- Output frequency behaves correctly only from 100 to 170 MHz input frequency
- Above this, output jumps to 2.1 GHz and output amplitude drops to ≈0.3 V

# Frequency Scans, Low speed mode, VDD=1.3 V

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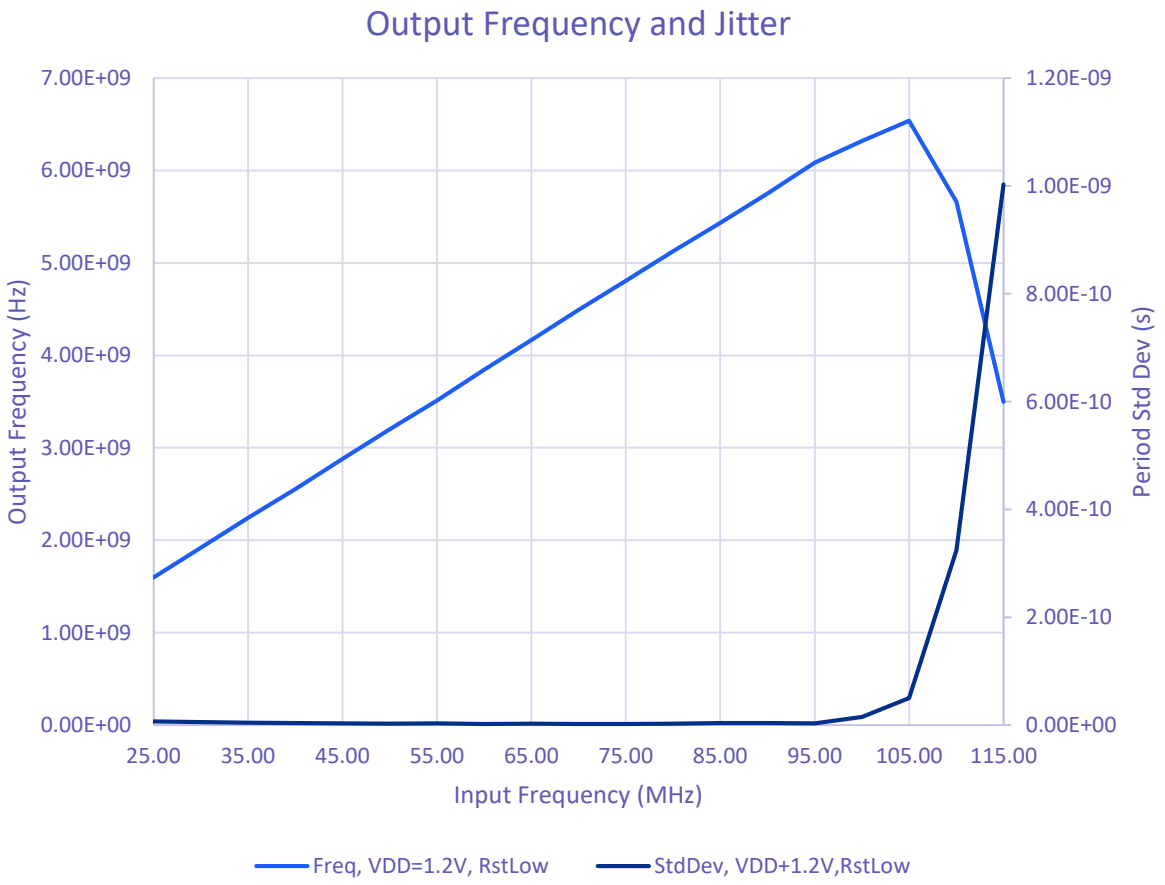
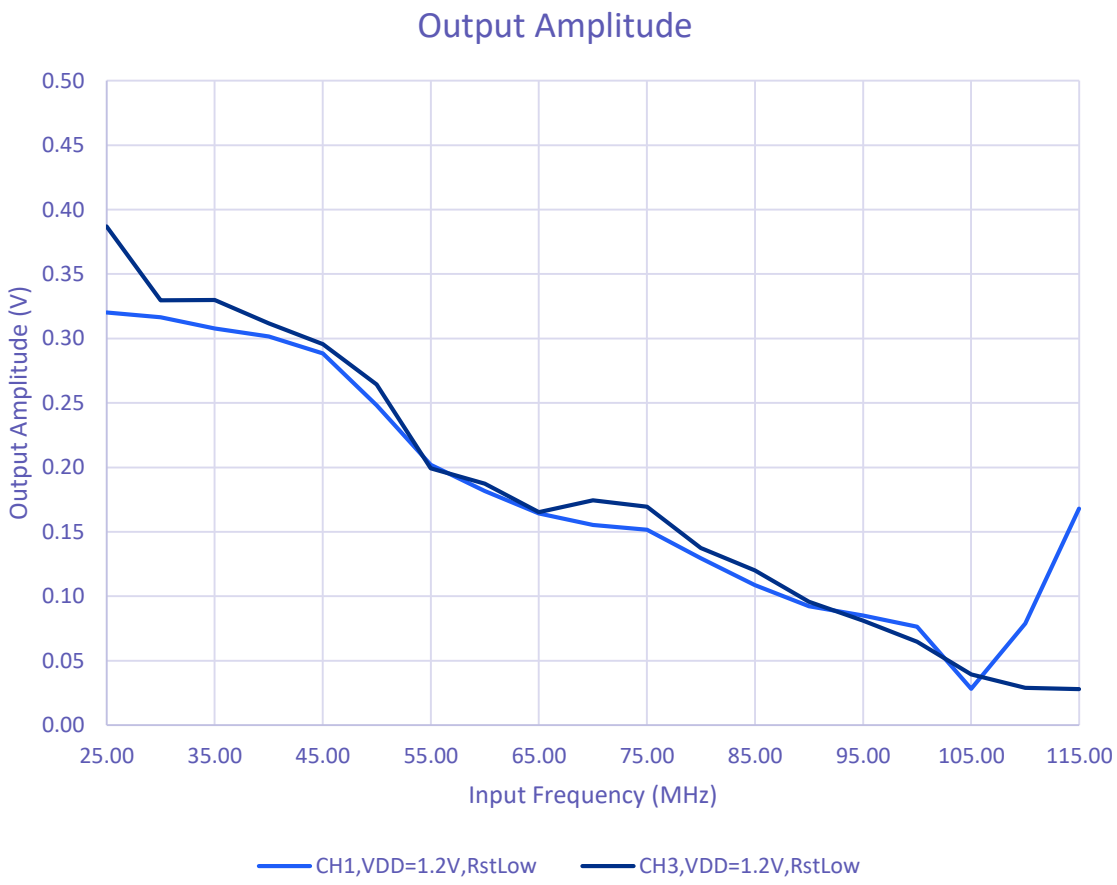
- Note increased output amplitude at VDD=1.3V
- At VDD=1.3V the output frequency behave correctly only from 150 to 240 MHz input frequency

# Automated Frequency Scans, High speed mode

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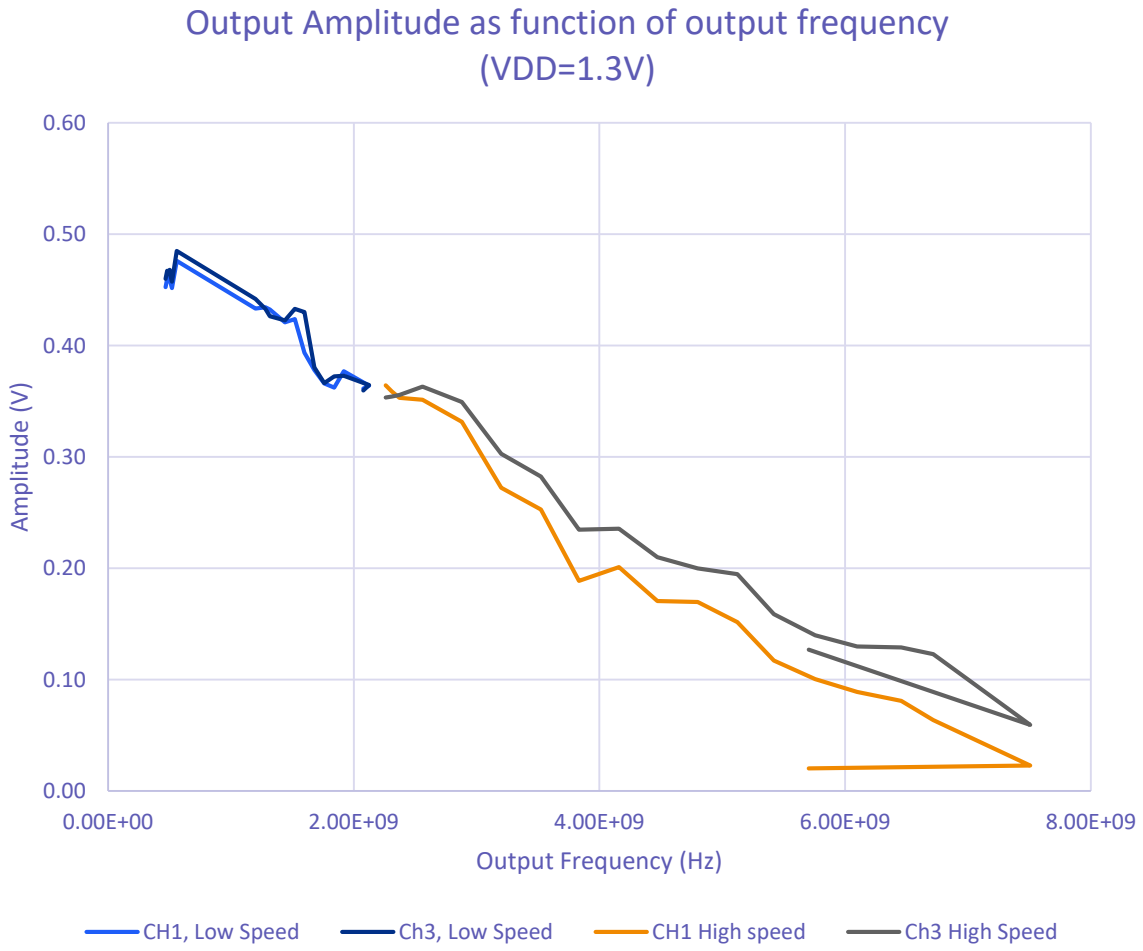
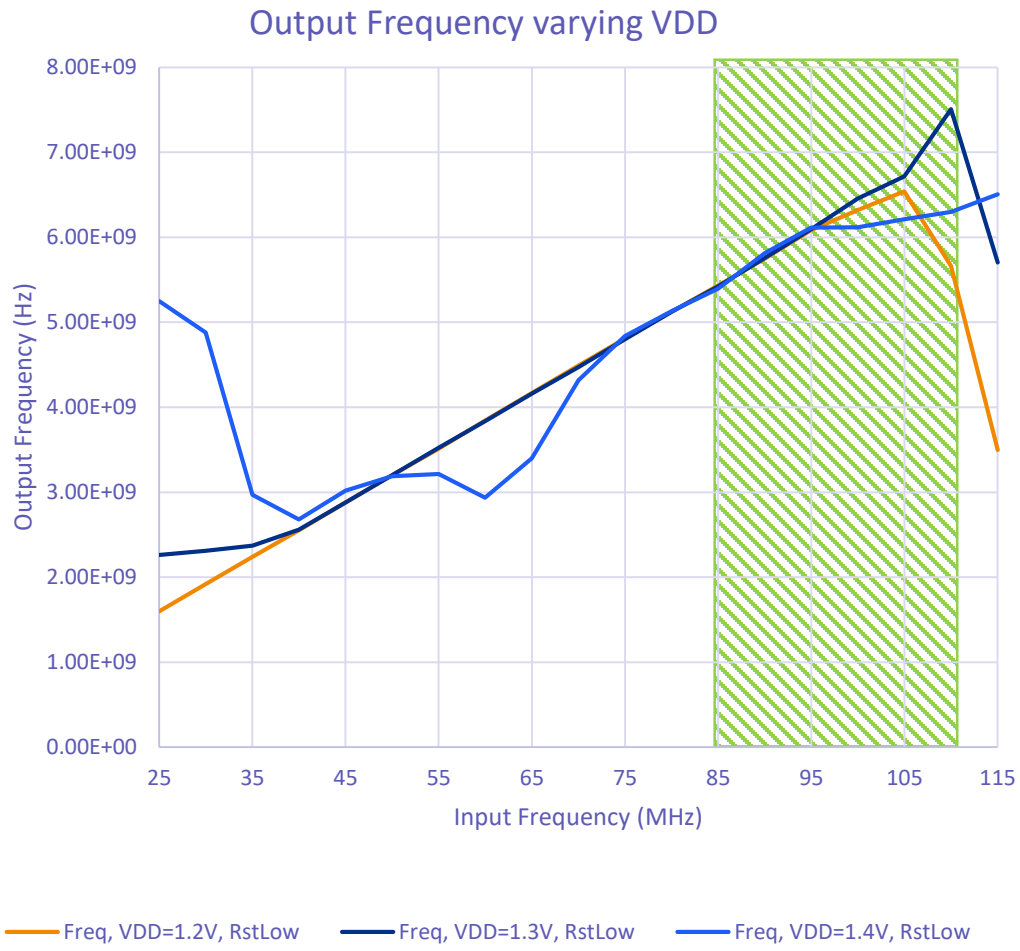
- Output frequency behaves correctly over wide range, but stops slightly short of 7GHz maximum.
- Output amplitude is very attenuated at this frequency, 40 mV@ 6.5 GHz = 13 Gbits/s, 140 mV @ 5.1 GHz = 10.2 Gbits/s

# PLL Summary

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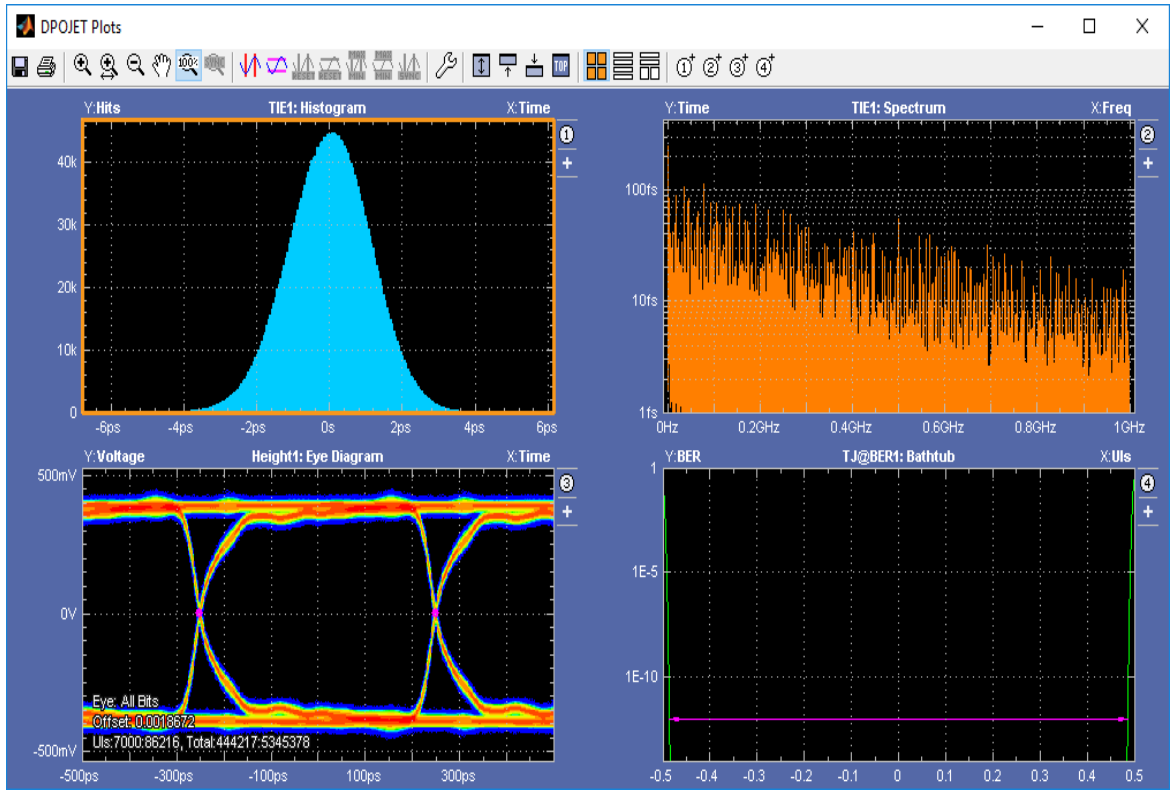
- The output amplitude decreases rapidly with increasing output frequency.
- The PLL upper frequency range can be increased slightly by increasing VDD to 1.3V.
- PLL will lock at much lower frequencies than target specification.

# CTLE Tests

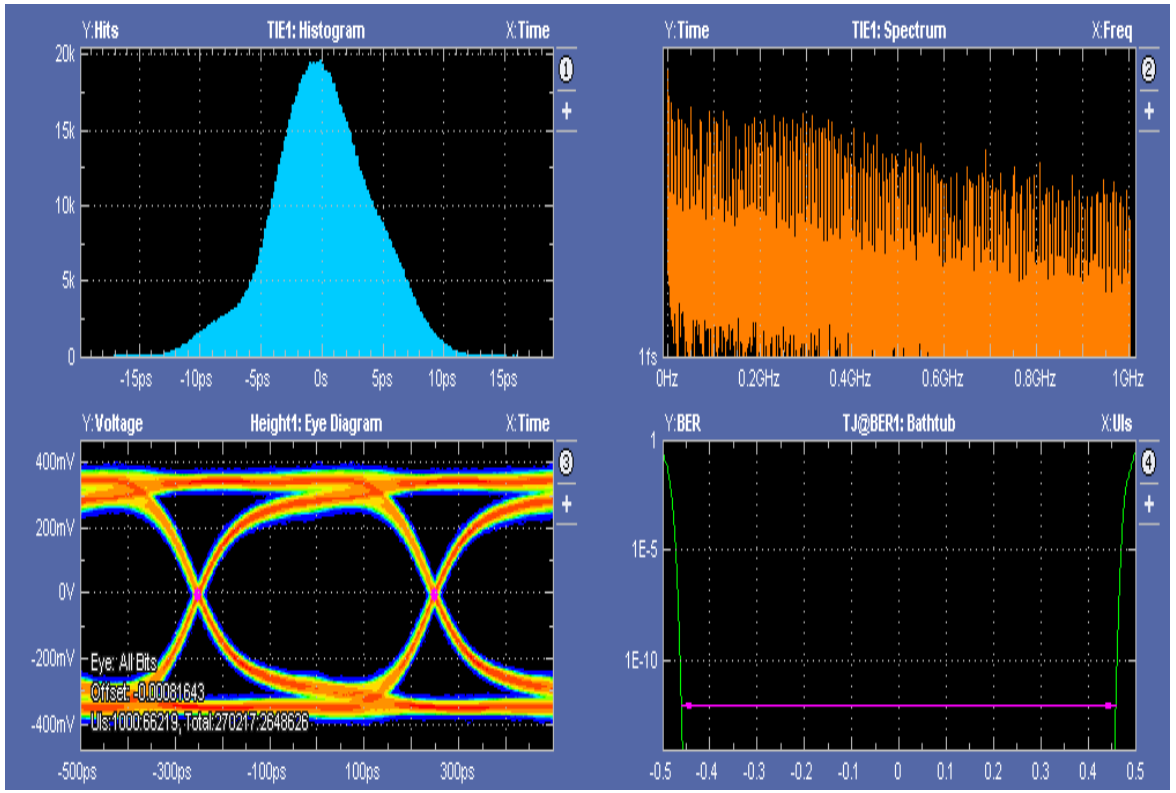
- KCU105 is programmed with Xilinx Integrated Bit Error Ratio Tests (IBERT) IP.
  - Typically IBERT tests a signal looped out of the FPGA and back into the FPGA.
  - FPGA outputs can supply signals without looping back to FPGA inputs, viewing signal on a 33 GHz bandwidth Tektronix MSO73304DX ’scope.
  - Output pattern can be 7 bit, 9 bit… 31 bit PRBS.
    - Fully tests Multi Gigabit links.
    - ‘scope can reconstruct and measure the eye diagram.
  - Output pattern can be a fast clock (alternate 10101010)
    - Can be characterised using standard scope measurements.
- Firmware built for 2, 4, 5, 6, 8, and 10 Gbits/s.

# 2 GBits/s, VDD=1.2V

KCU105 direct to ’scope (72 inch cables)




KCU105 to DUT to ’scope (72 inch cables)




- The oscilloscope constructs the eye diagram.
- Note that the signal from the DUT has somewhat slower edges.

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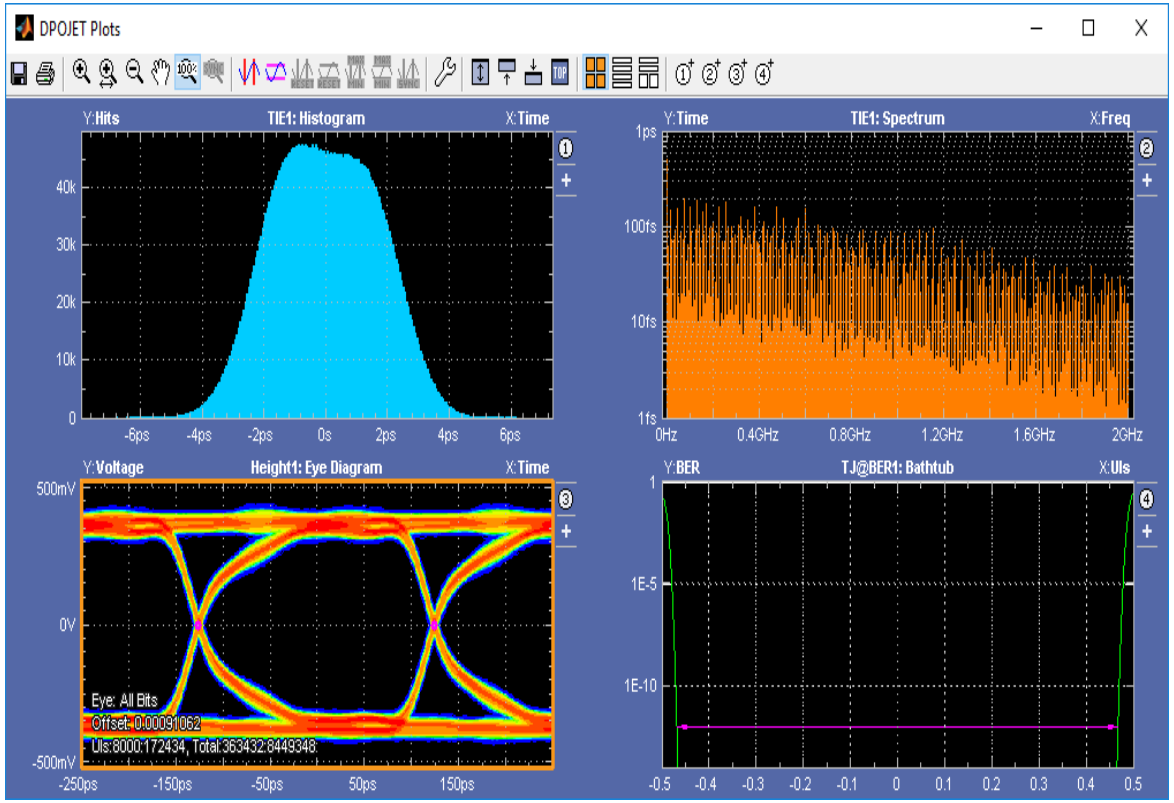
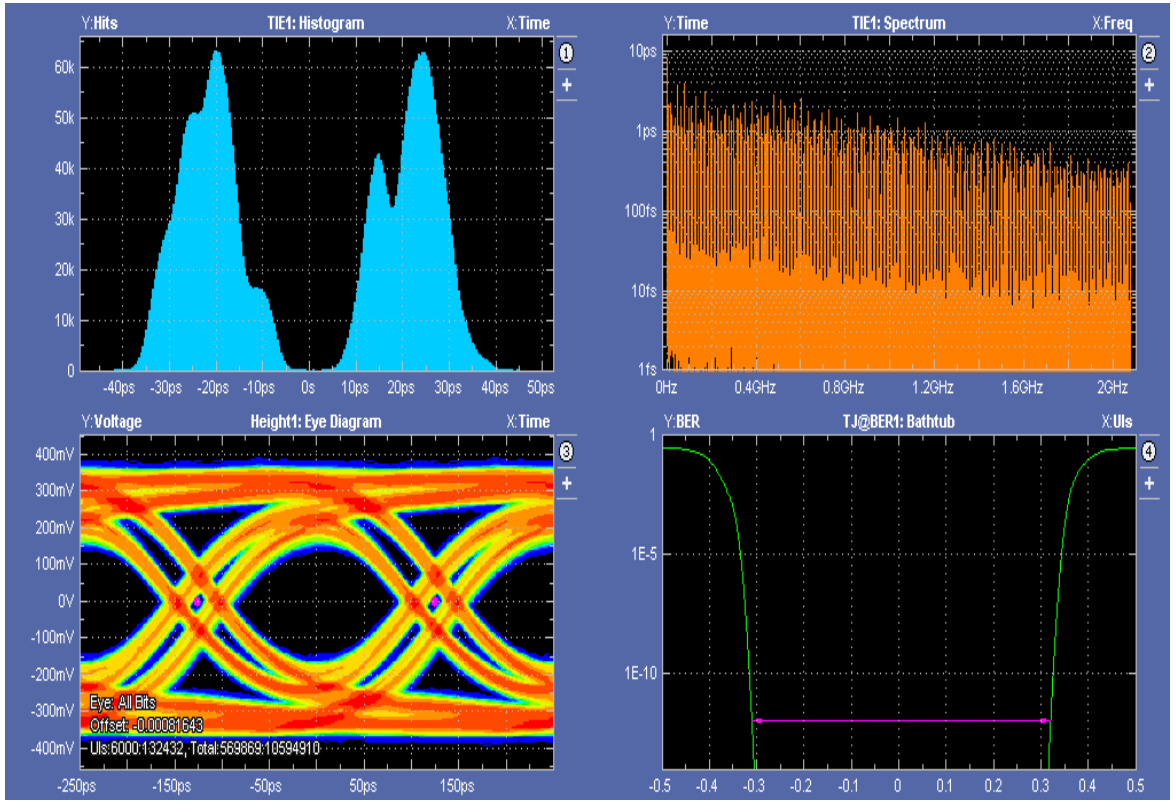
# 4 GBits/s, VDD=1.2V

KCU105 direct to ’scope (72 inch cables)




KCU105 to DUT to ’scope (72 inch cables)




- The signals from the DUT now clearly slower edges.
- The eye has started to close due to different preceding bits

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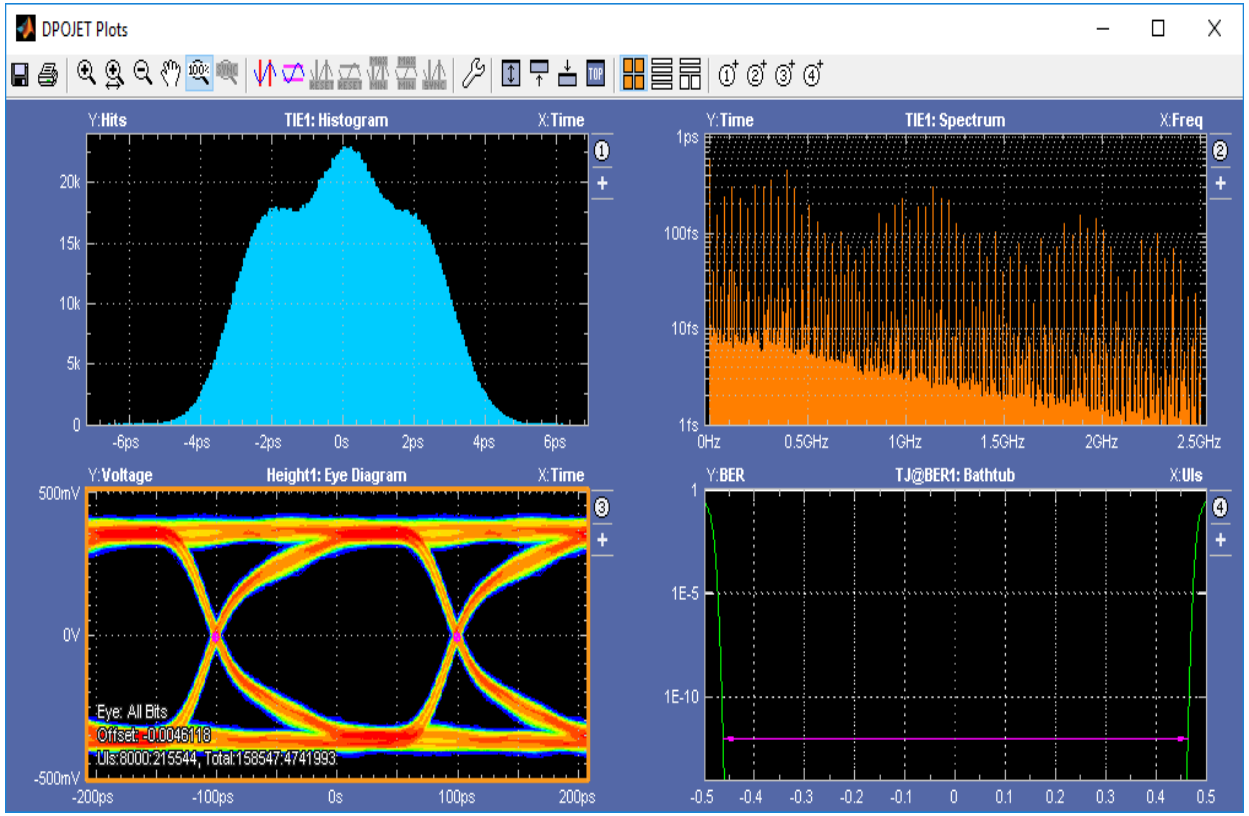
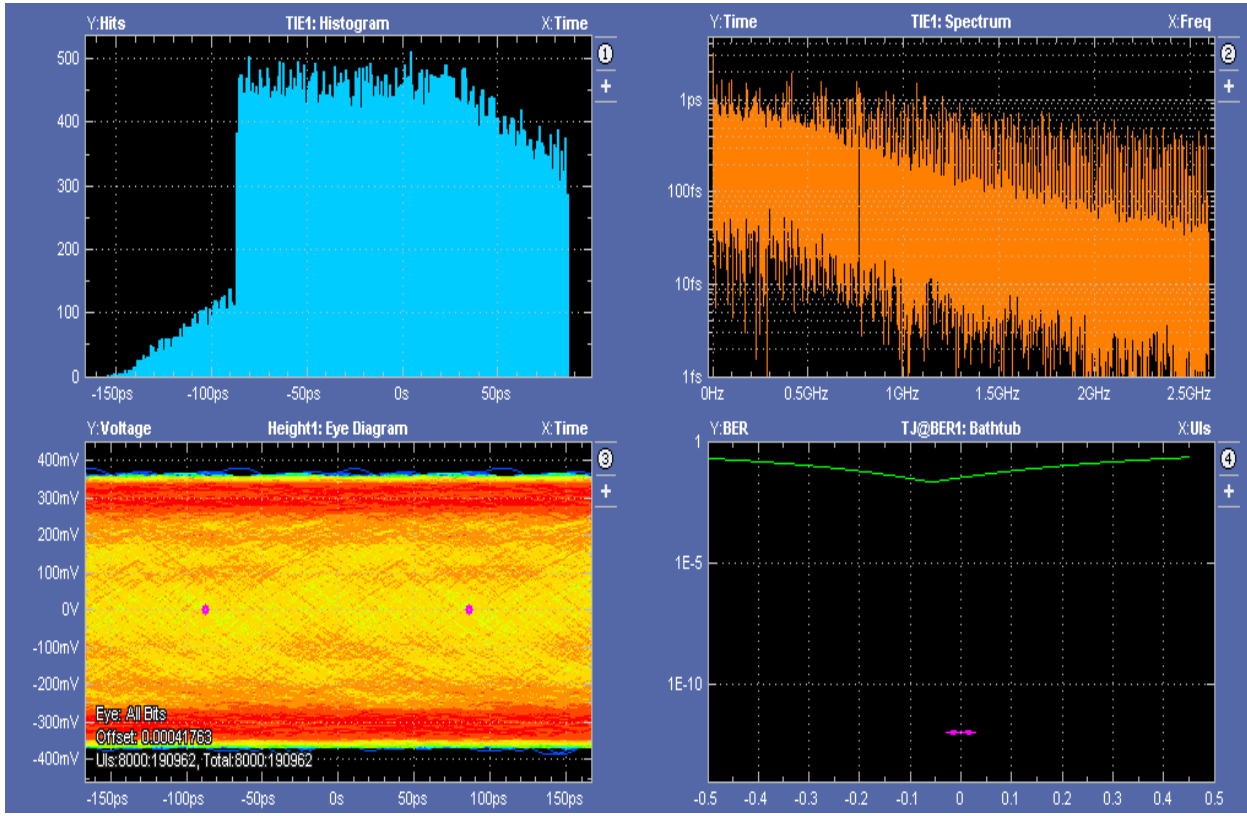
# 5 GBits/s, VDD=1.2V

KCU105 direct to ’scope (72 inch cables)




KCU105 to DUT to ’scope (72 inch cables)

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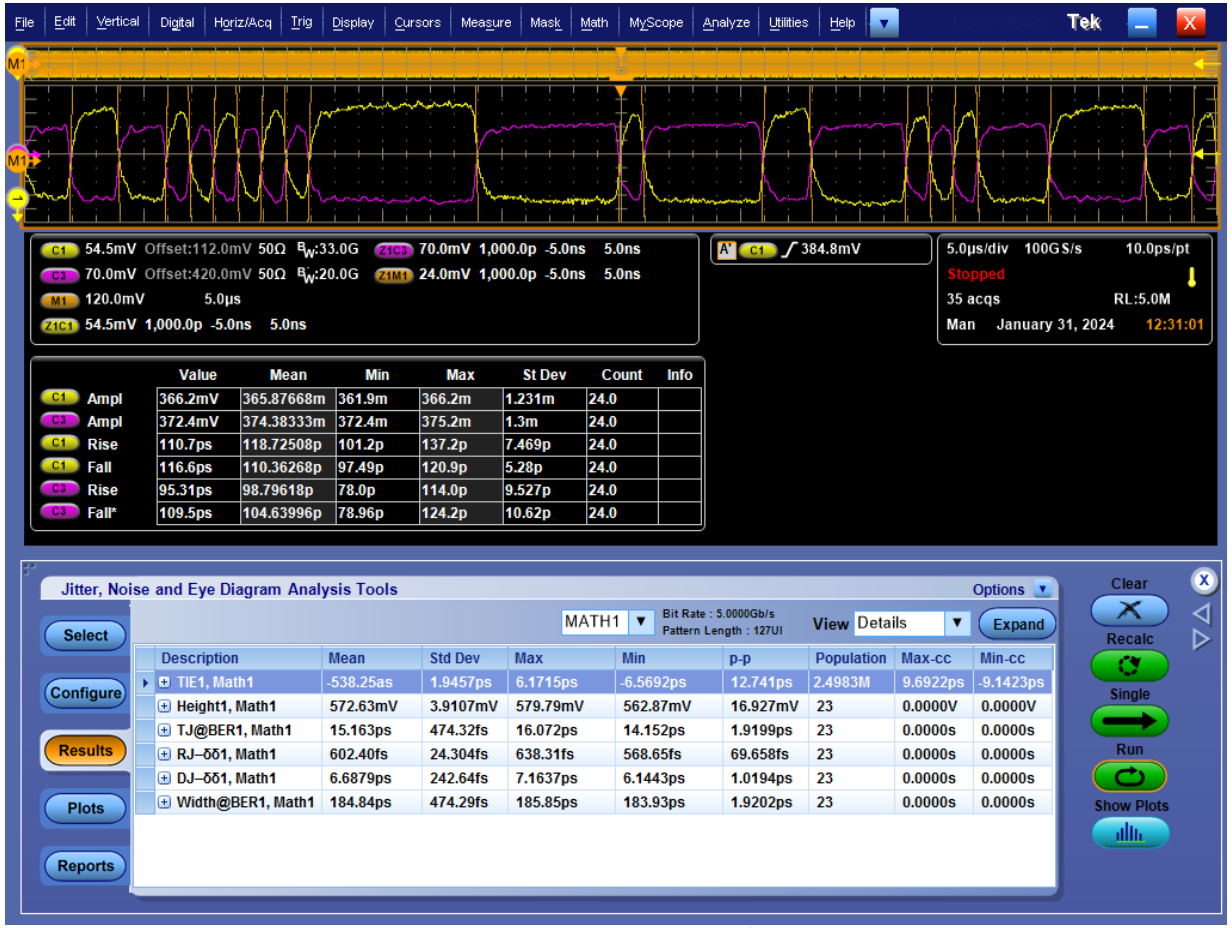
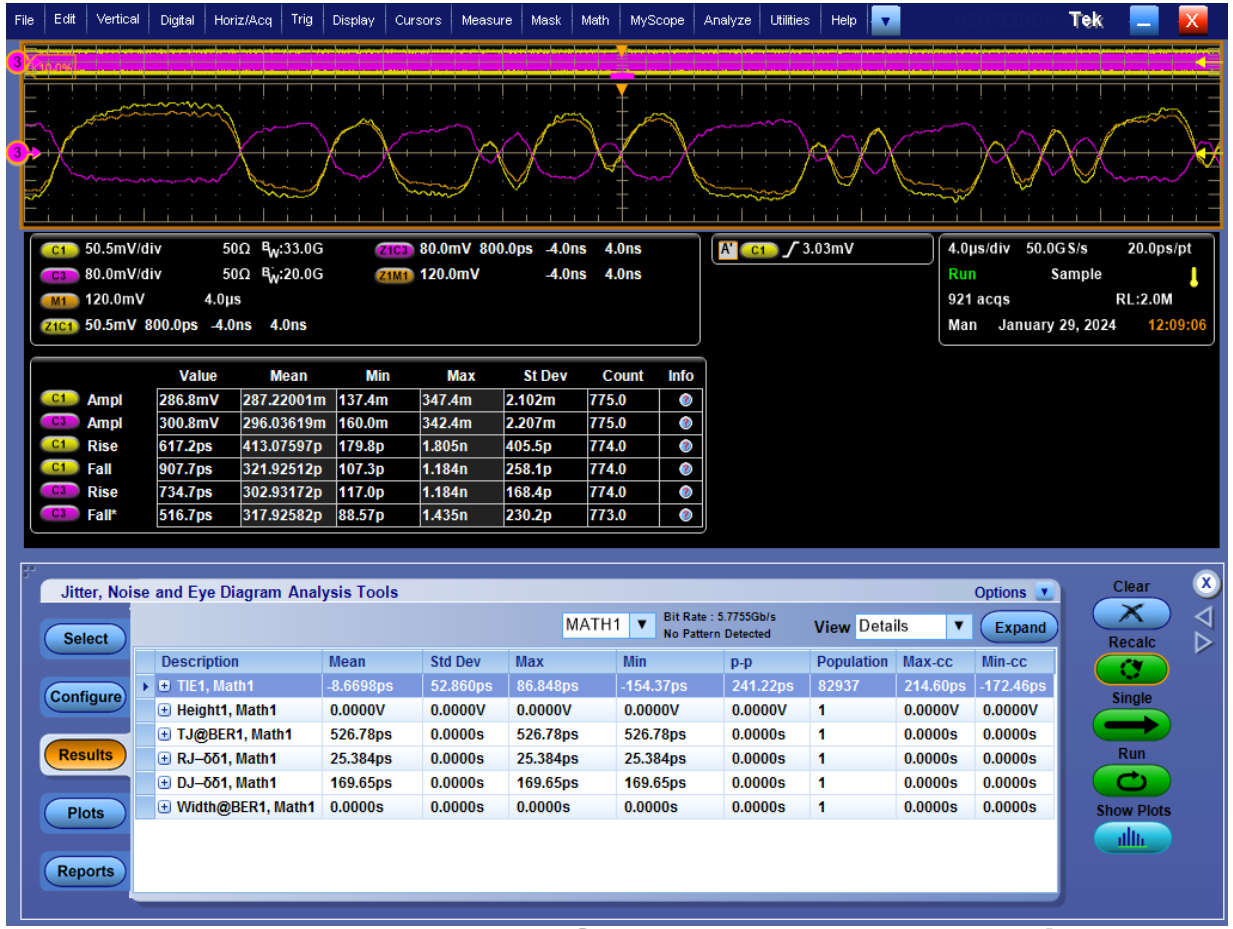
- The eye directly from the KCU105 remains open.
- The ‘scope cannot reconstruct the eye from the DUT.

# 5 GBits/s, VDD=1.2V

KCU105 direct to ’scope (72 inch cables)




KCU105 to DUT to ’scope (72 inch cables)

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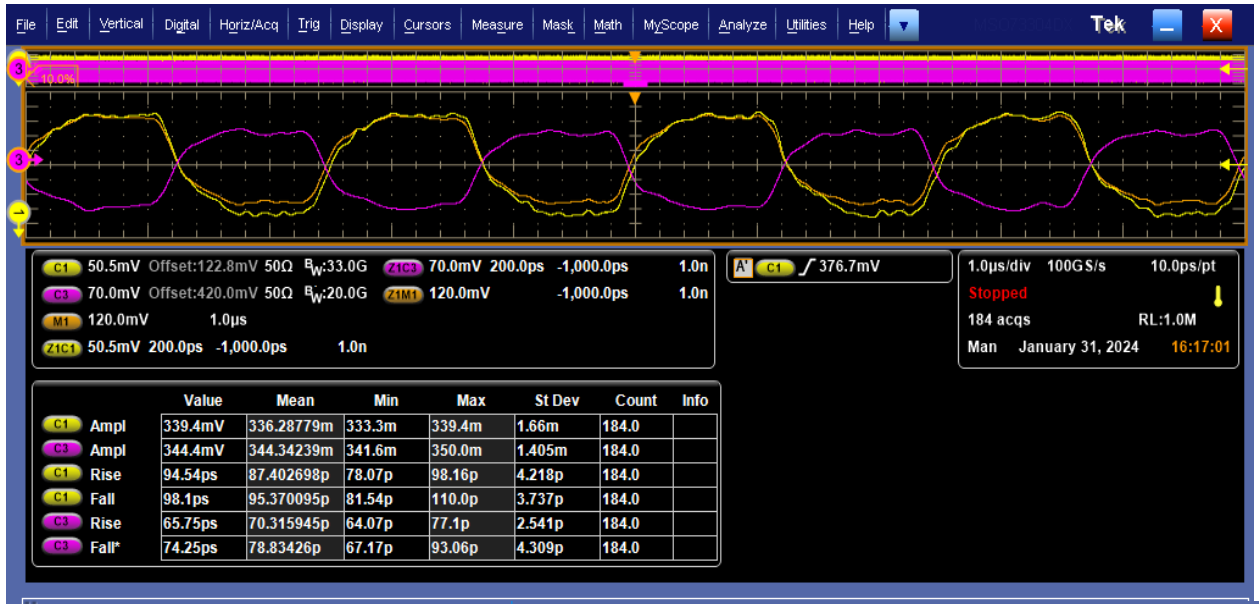
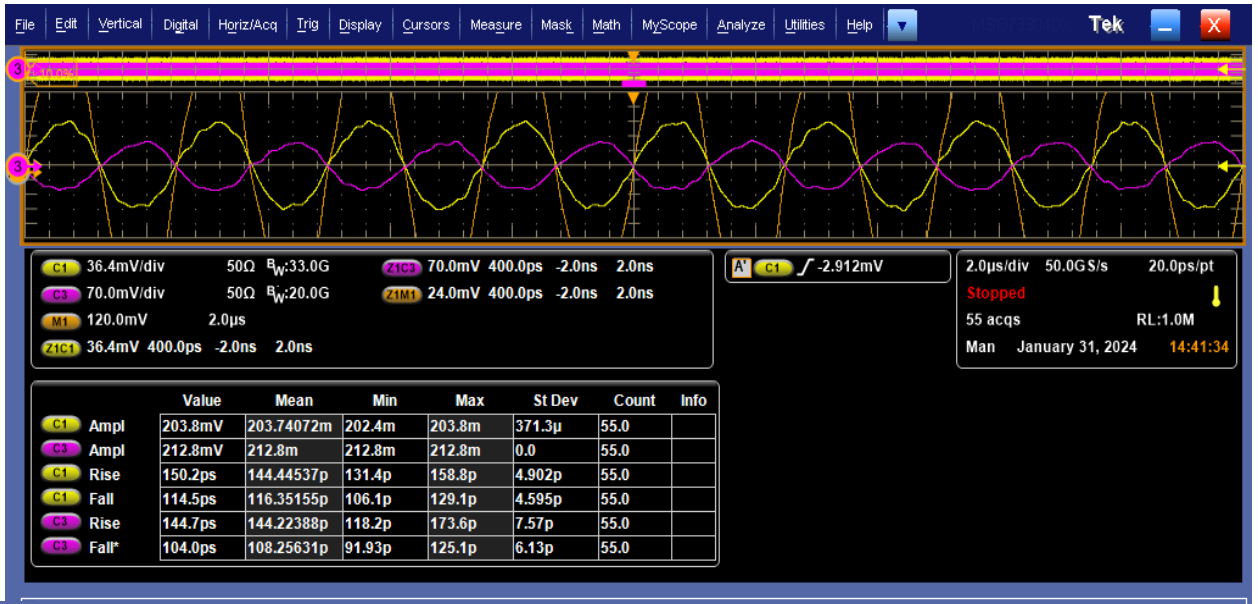
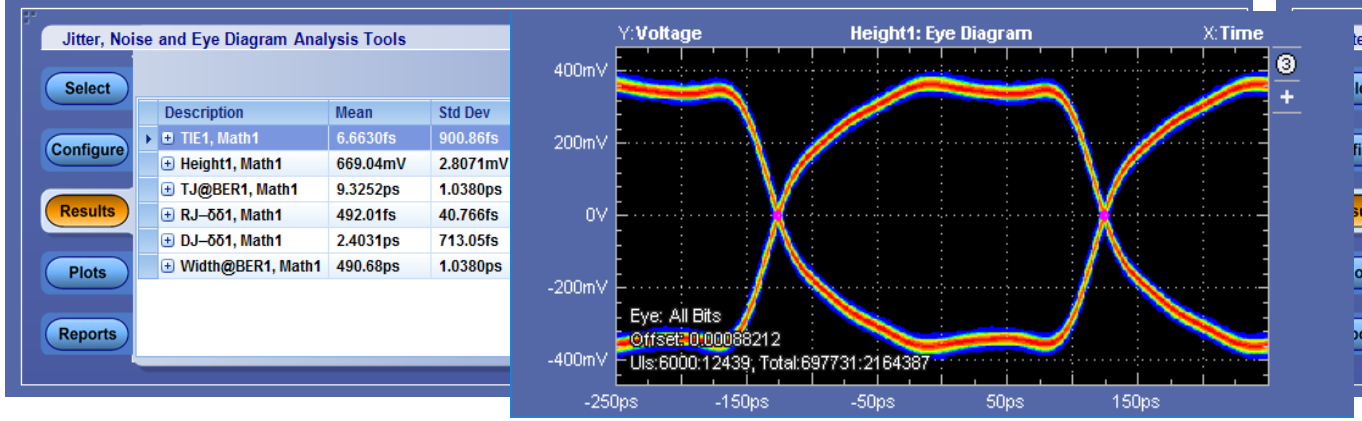
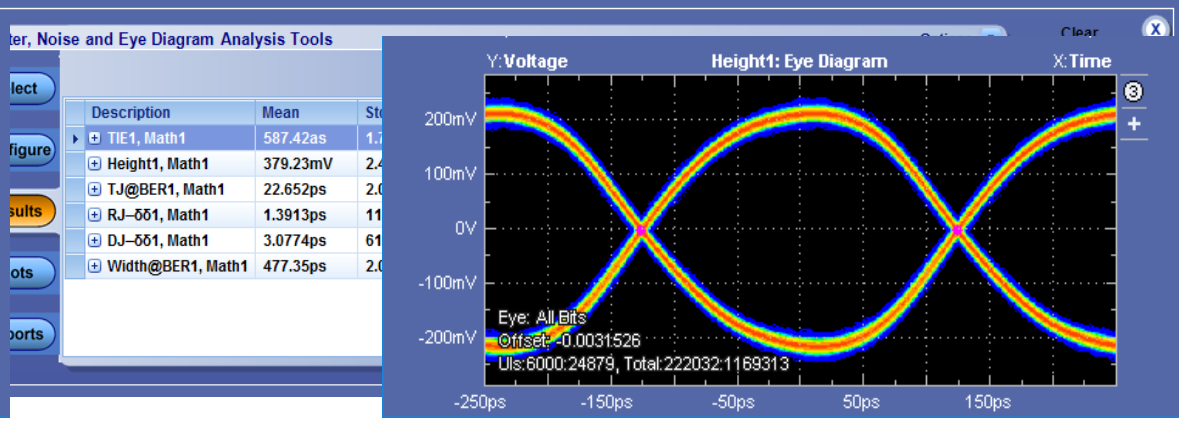
- The ‘scope cannot reconstruct the eye from the DUT - but the KCU105 could.
- Note how lone 1’s only just cross the midpoint.

# Fast clock pattern, 4 Gbits/s, 2 GHz

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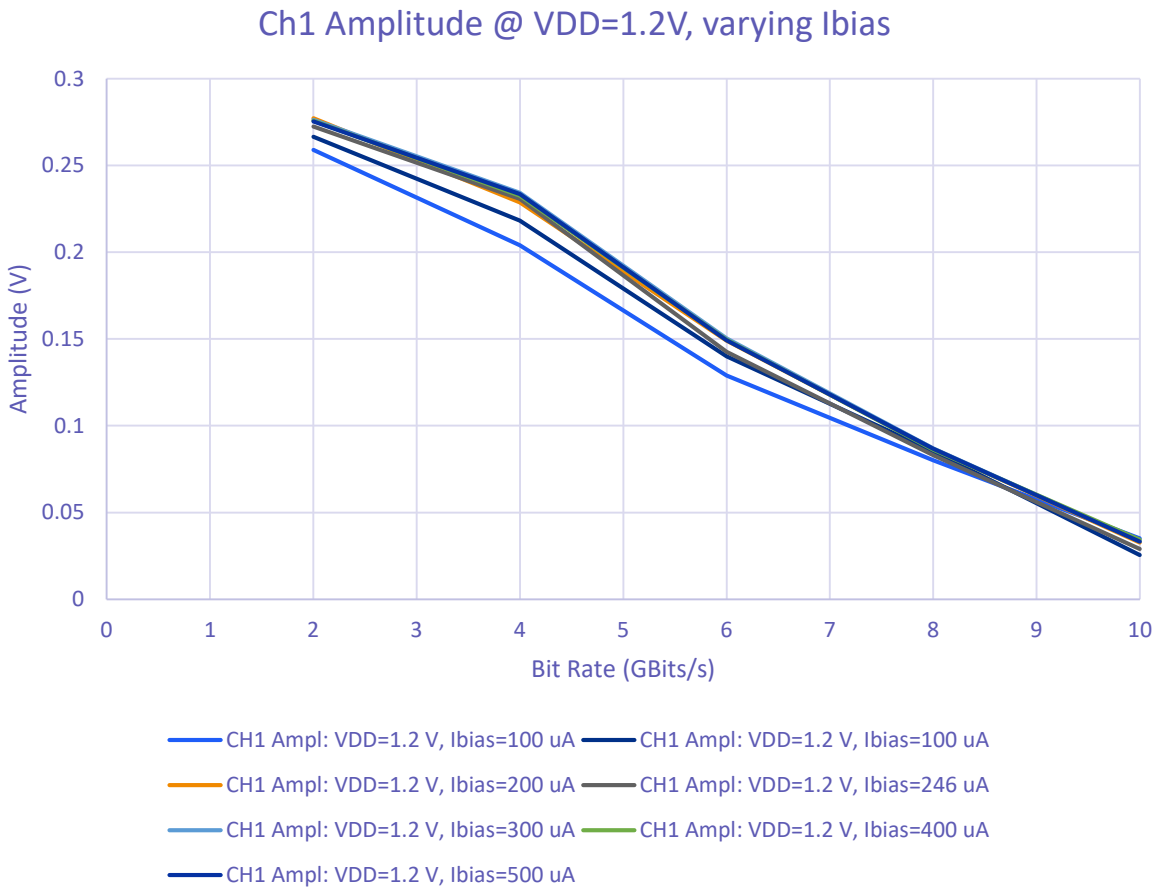
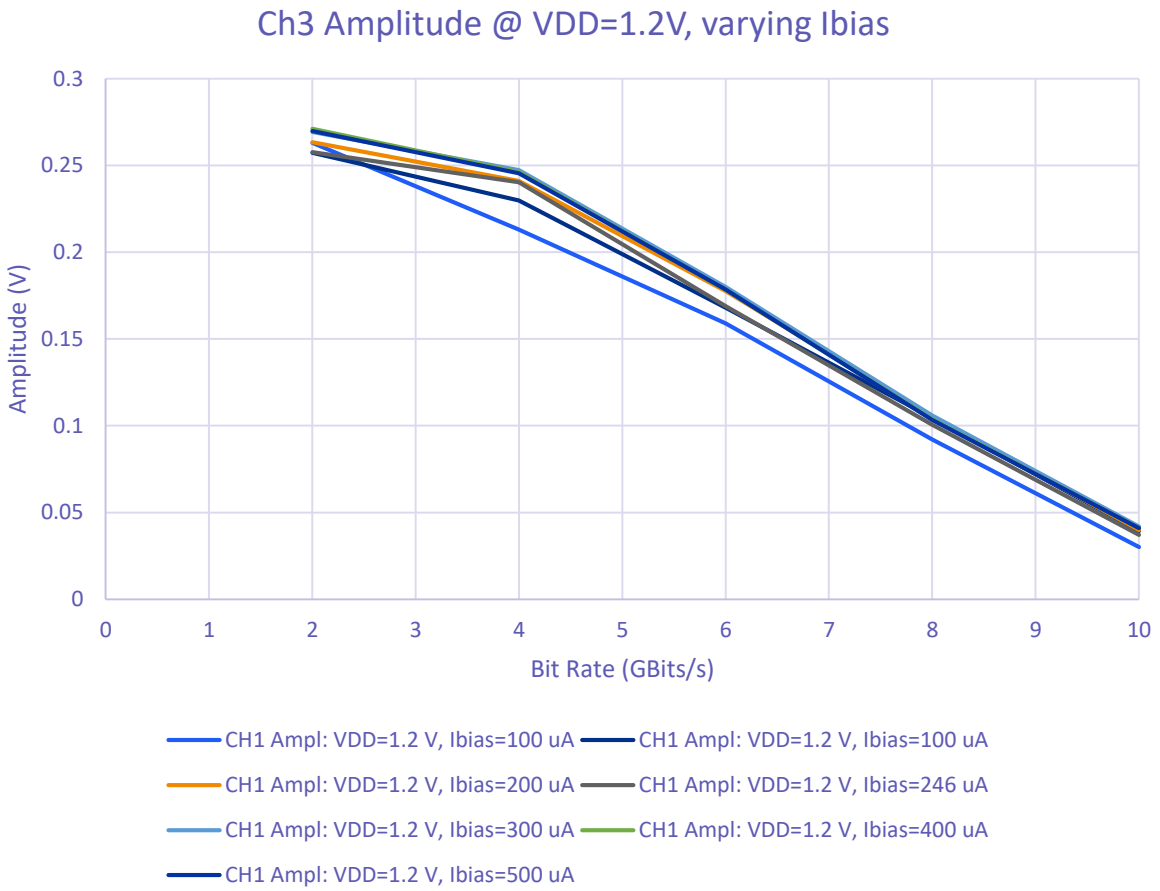
- Signal from DUT nearly sinusoidal and lower amplitude.
- Can be characterised by conventional scope measurements.

# Varying $I_{BIAS}$ operating point

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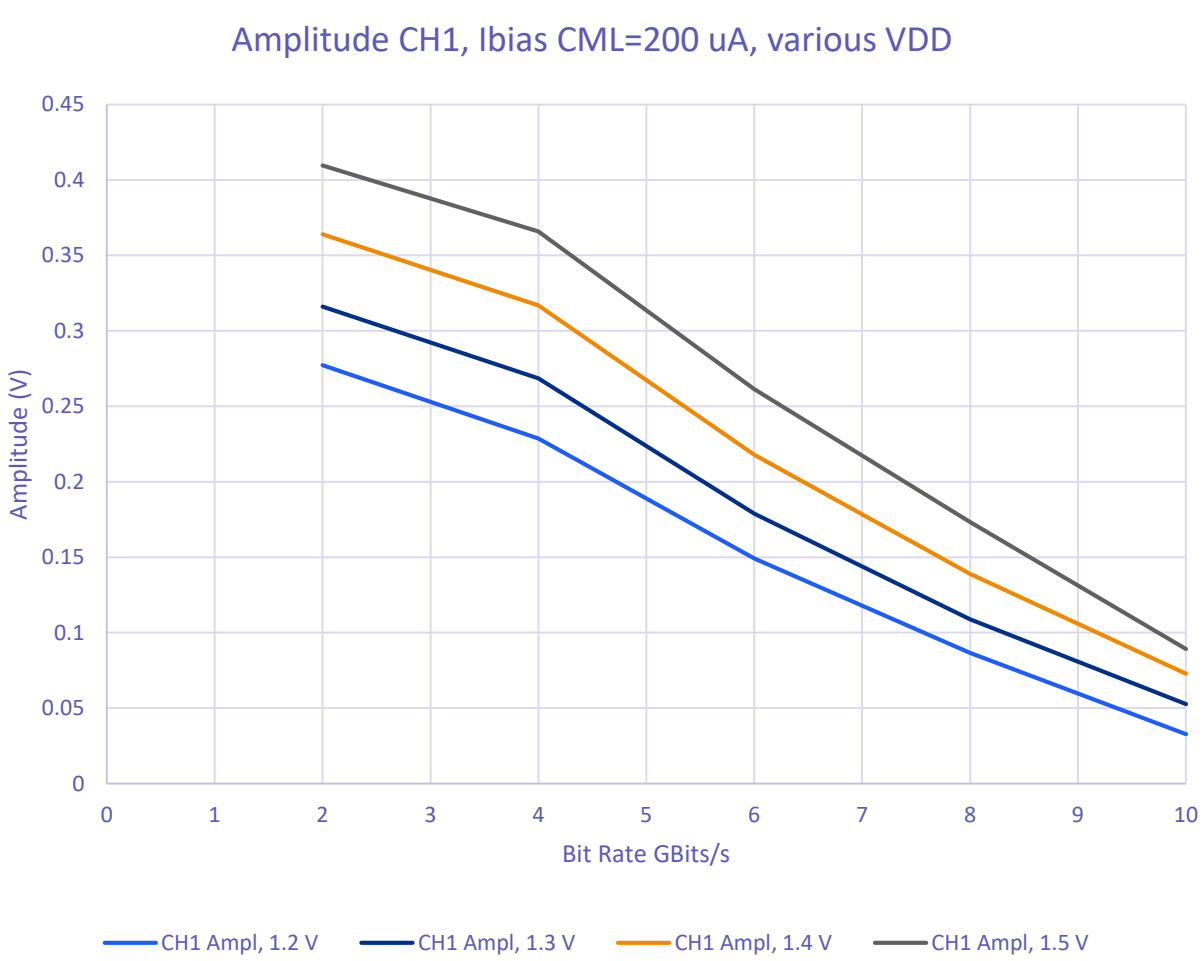
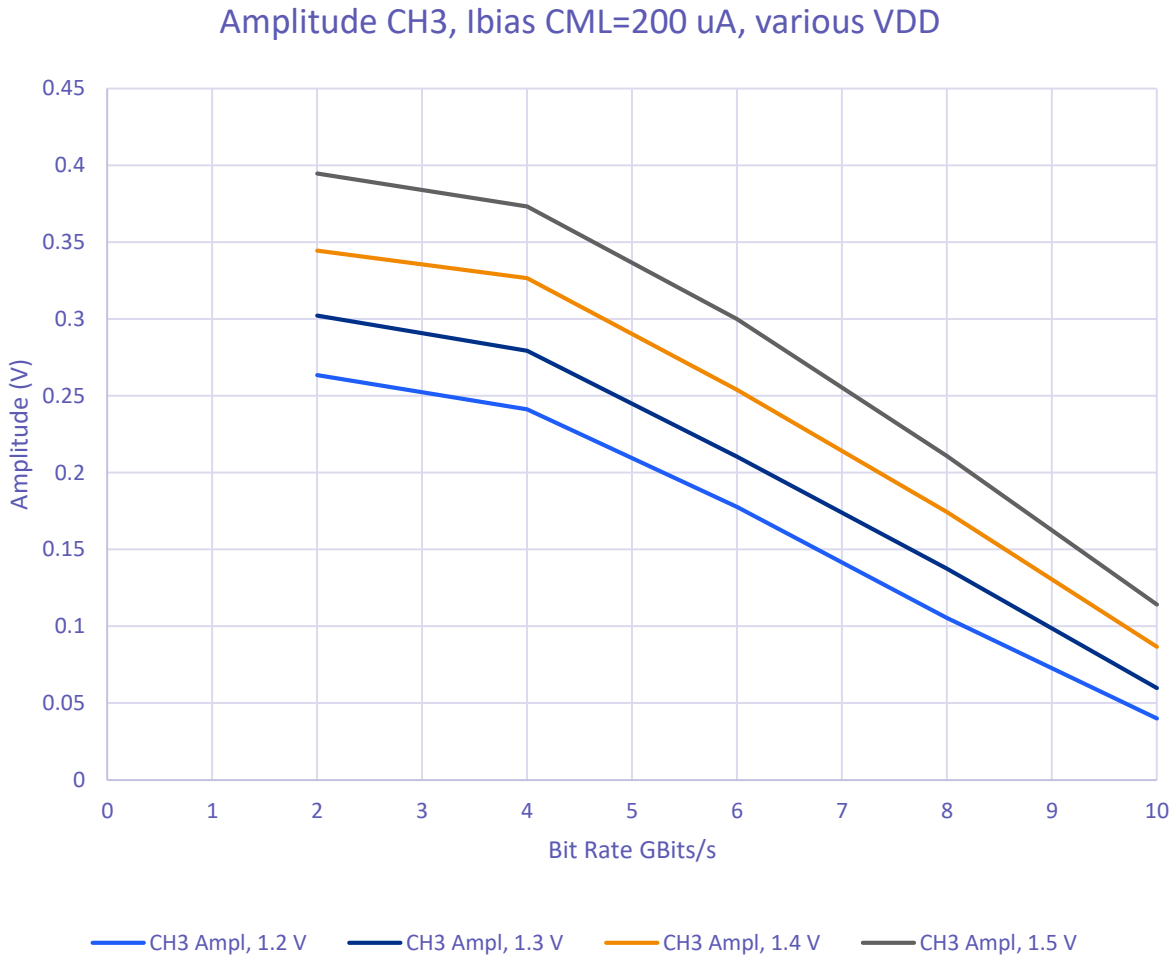
- Increasing $I_{BIAS}$ slightly increases amplitude.,
- But does not increase bandwidth.

# Varying VDD operating point

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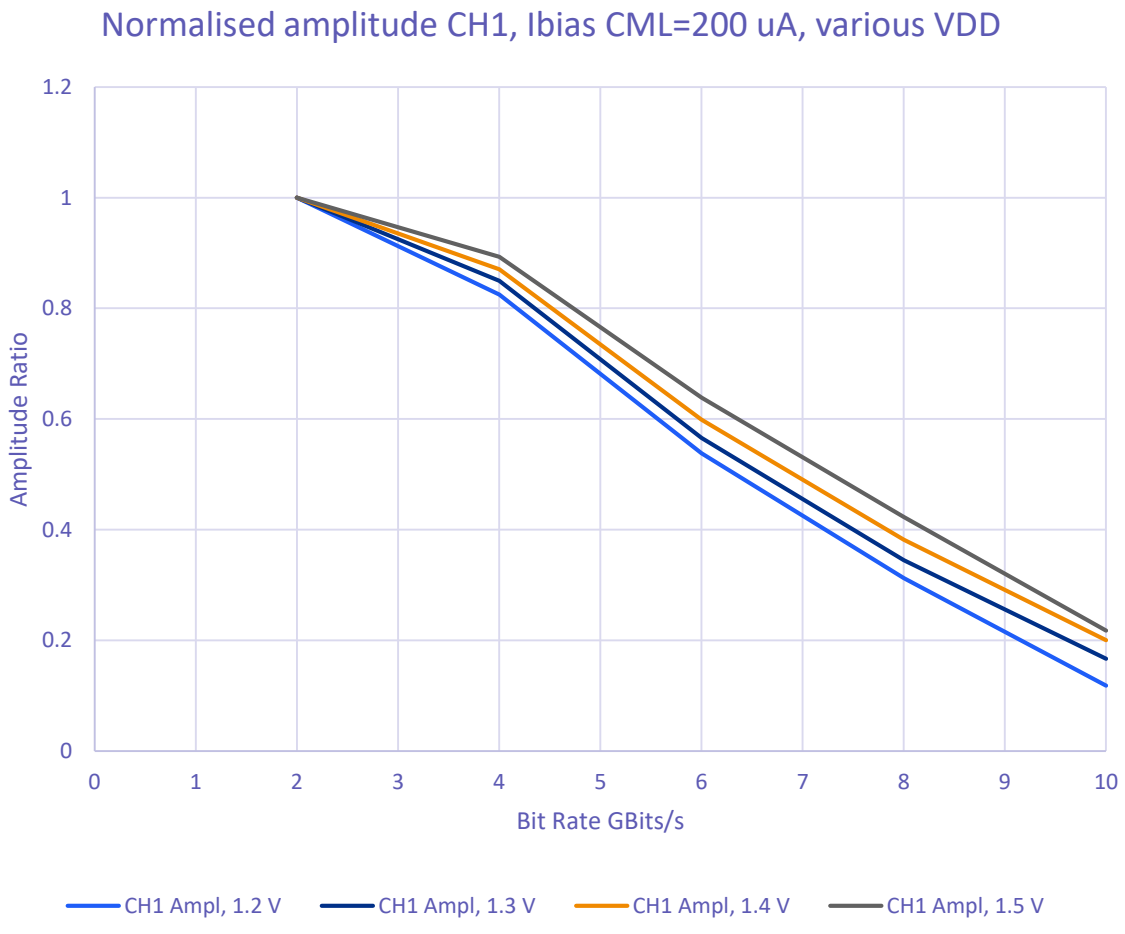
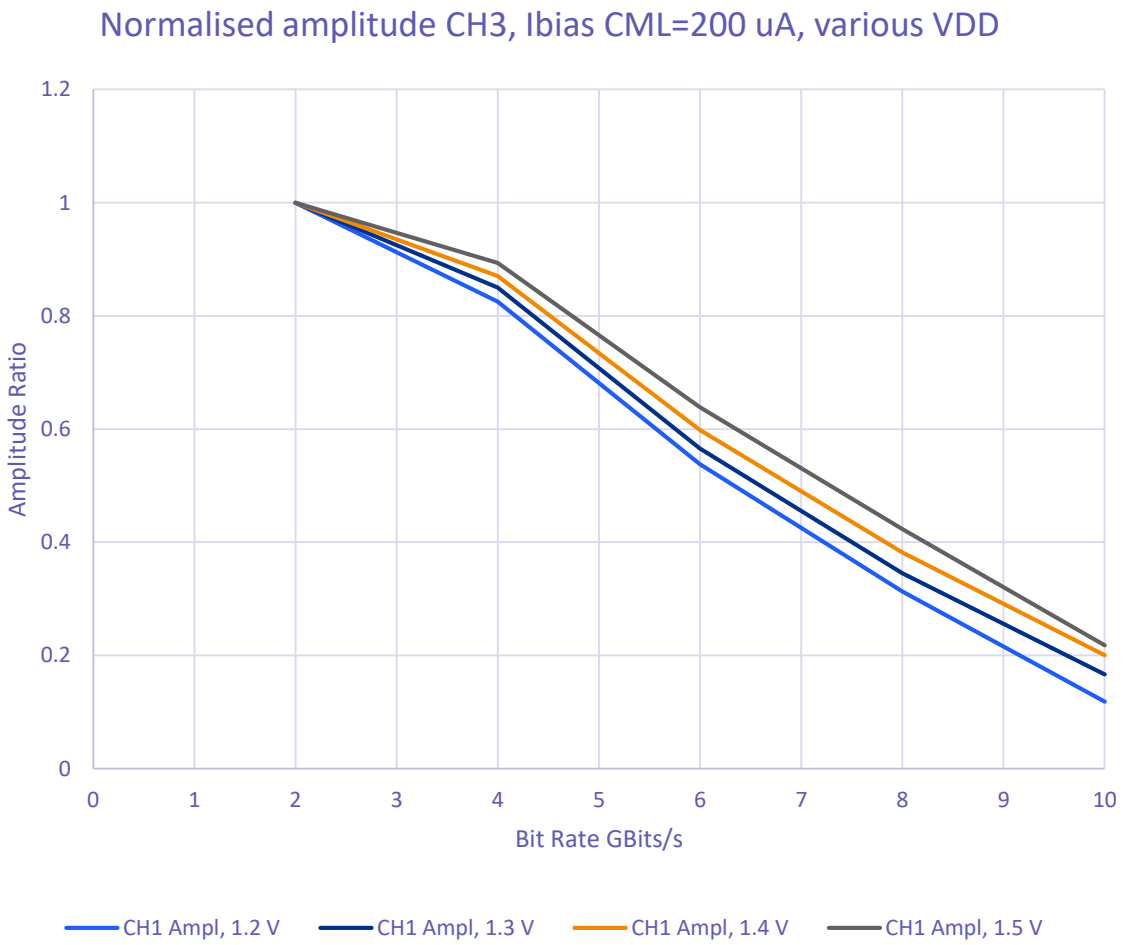
- Increasing VDD significantly increases amplitude,

# Varying VDD, Normalising by 2 Gbits/s value

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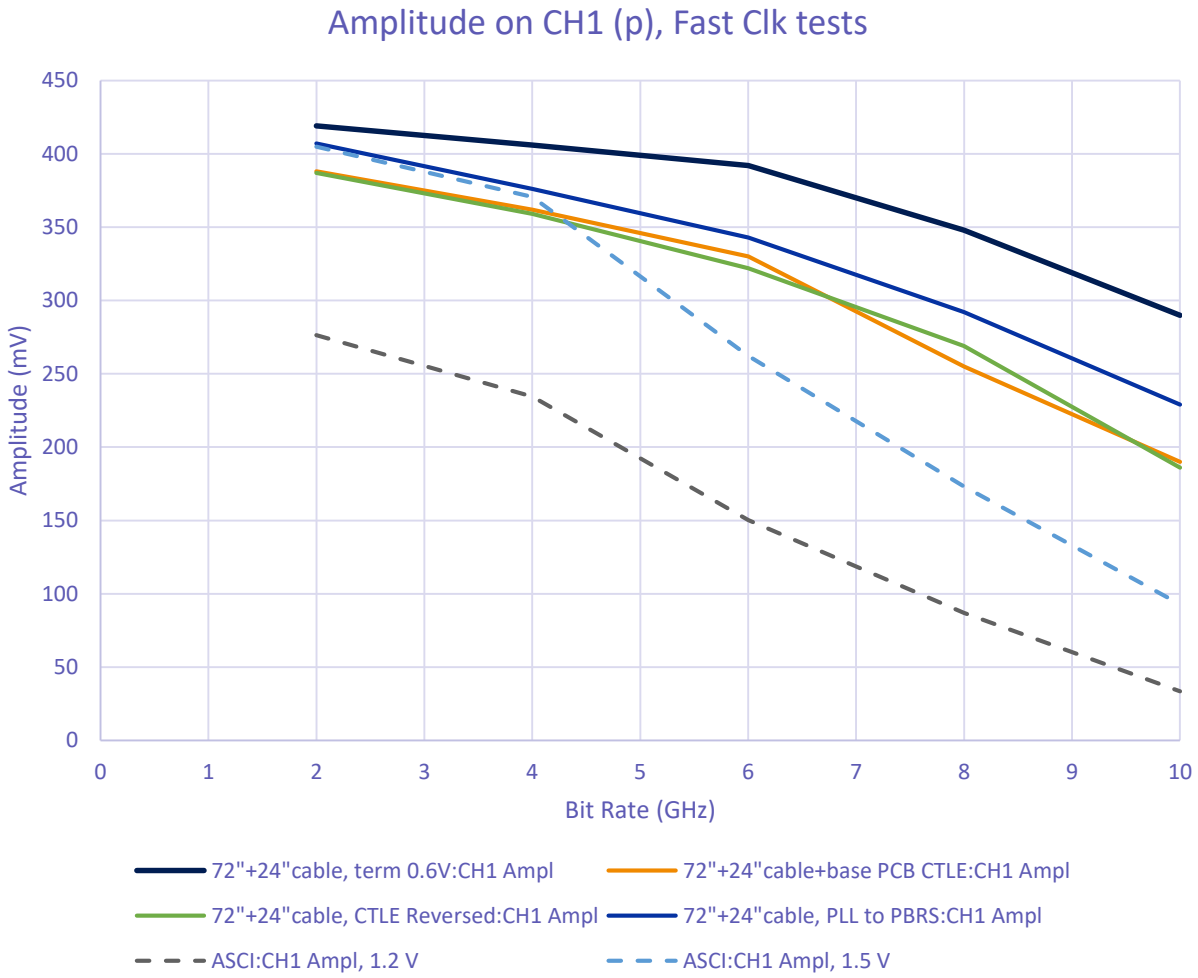
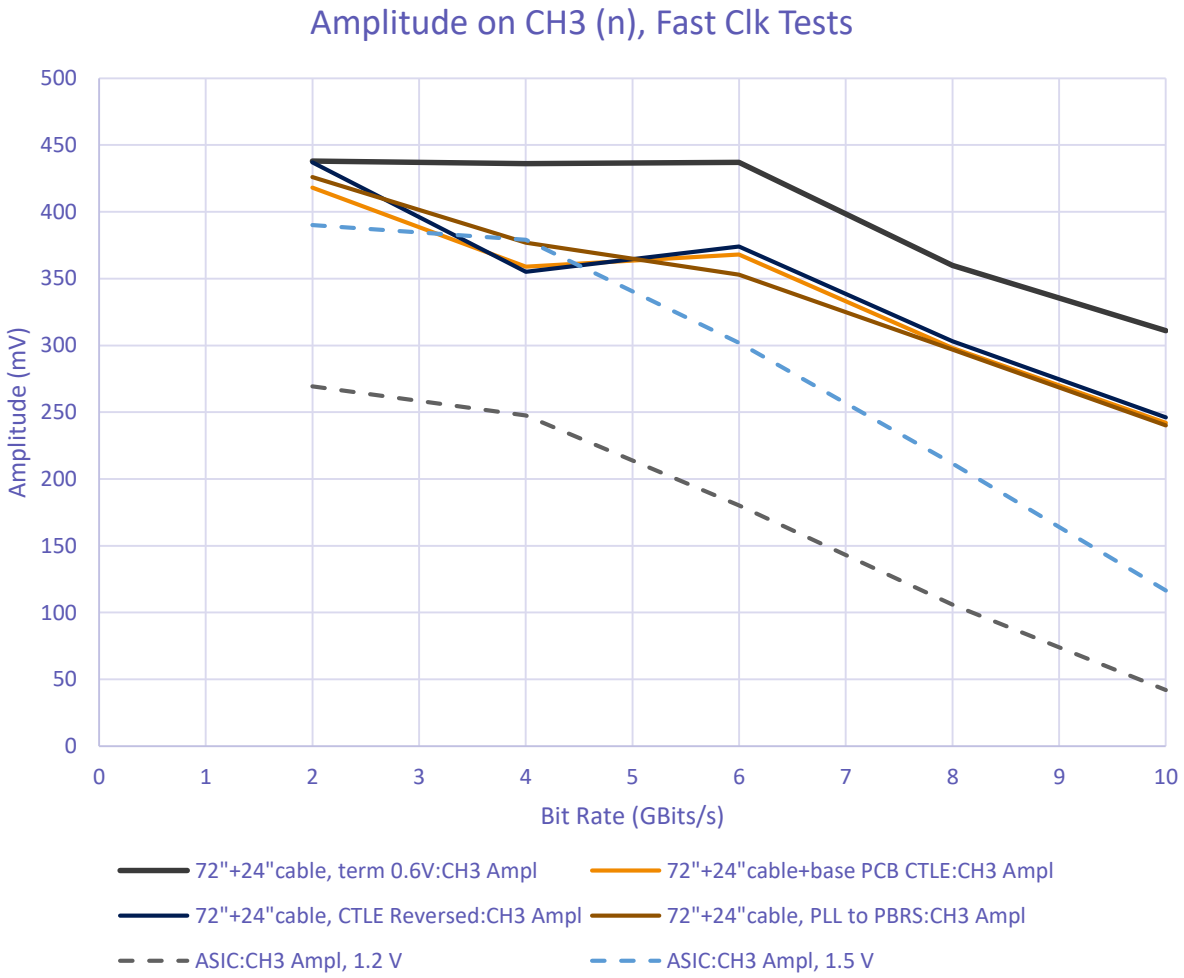
- Increasing VDD somewhat increases bandwidth

# Comparison with bare PCB with direct wire bonds

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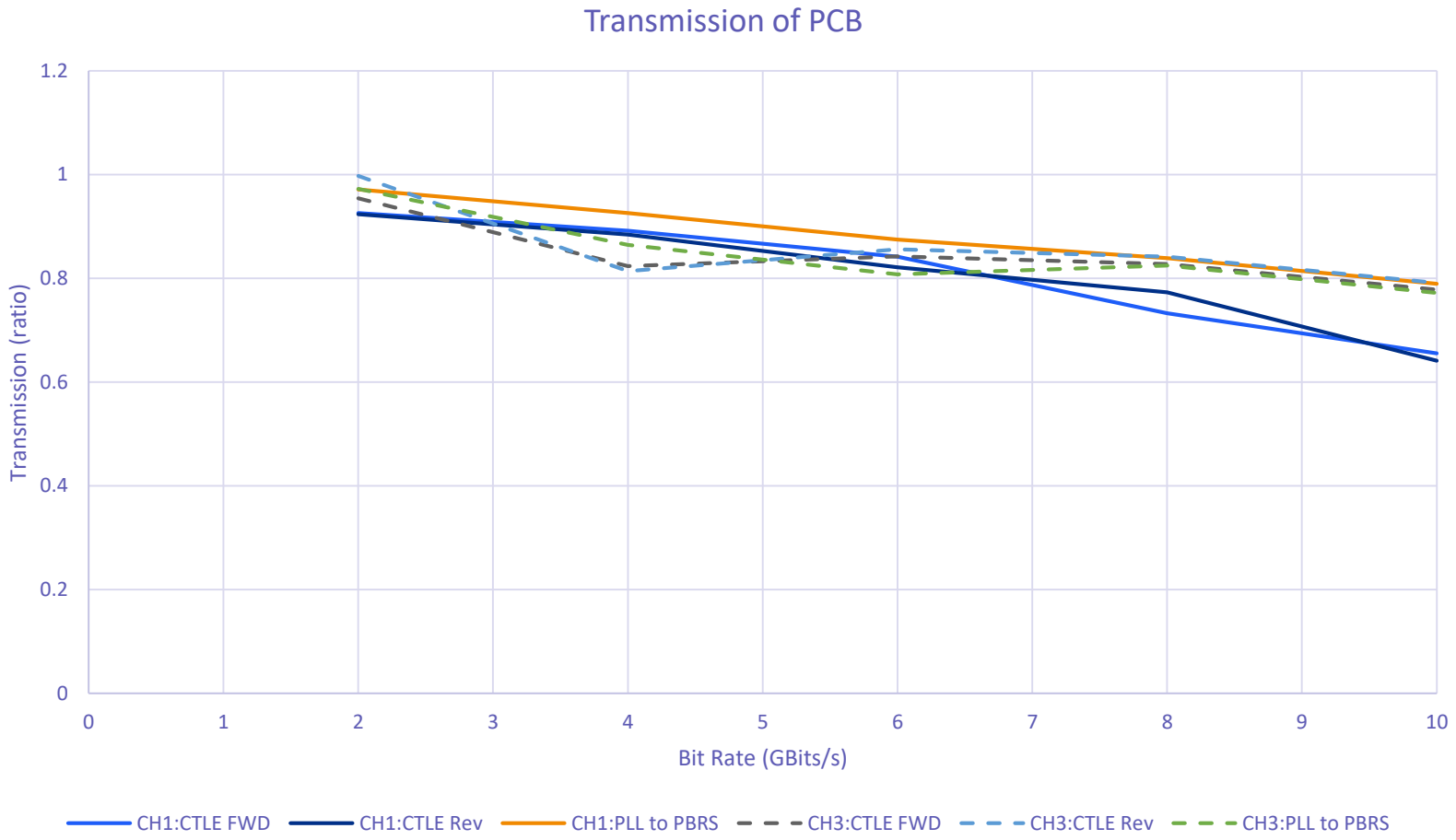
- Bold curve is direct from KCU105,
- Dotted are using the DUT.

# PCB Loss

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- For most signals total path in and out gives 80% transmission, estimate 90 % transmission on each leg.
- For CTLE P side loss is worse. Not understood.

# Questions?