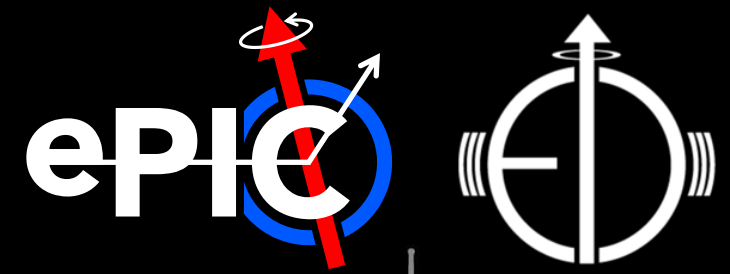




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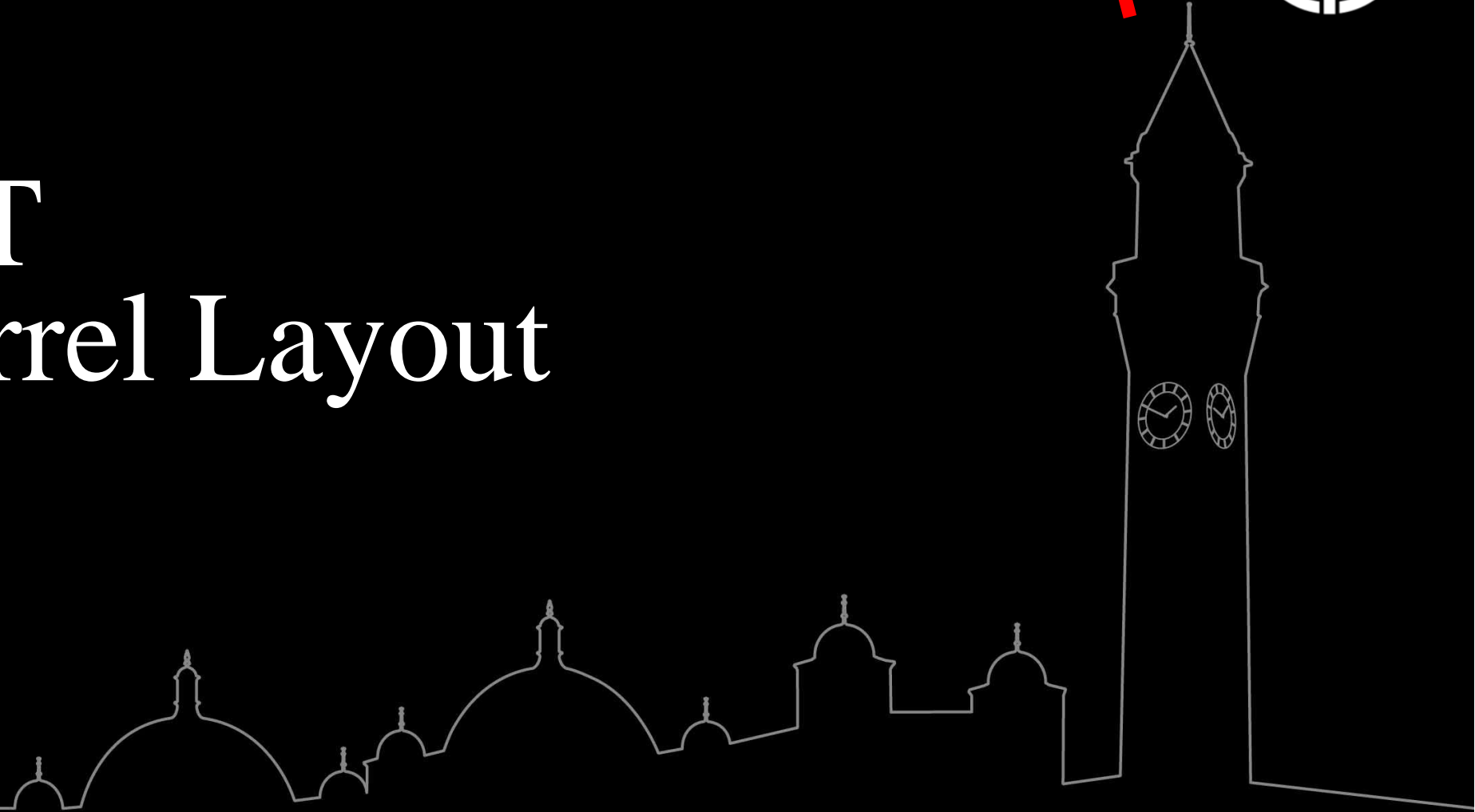


# ePIC SVT Outer Barrel Layout

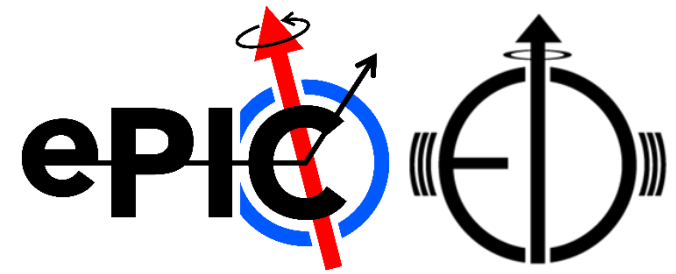
James Glover

EIC-UK WP1 (MAPS)

Wed, 20<sup>th</sup> March 2024



# Previous layout presentations

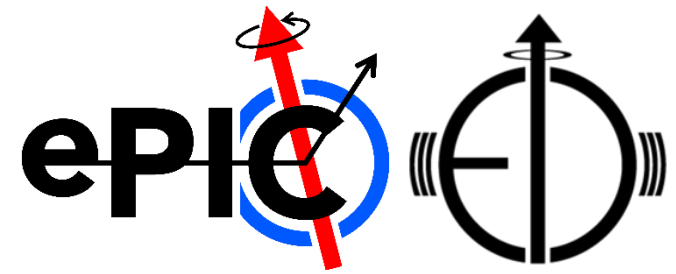


There has been a small series of presentations already on this CAD work:

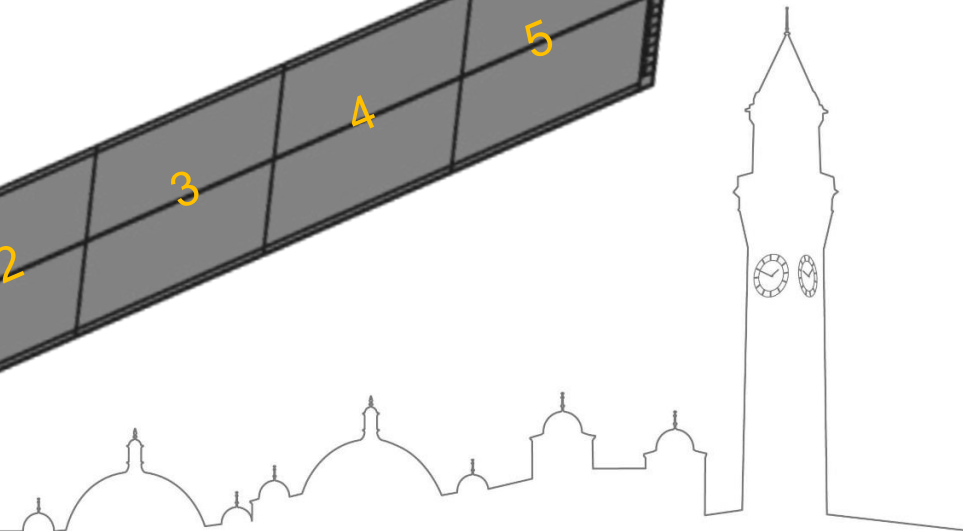
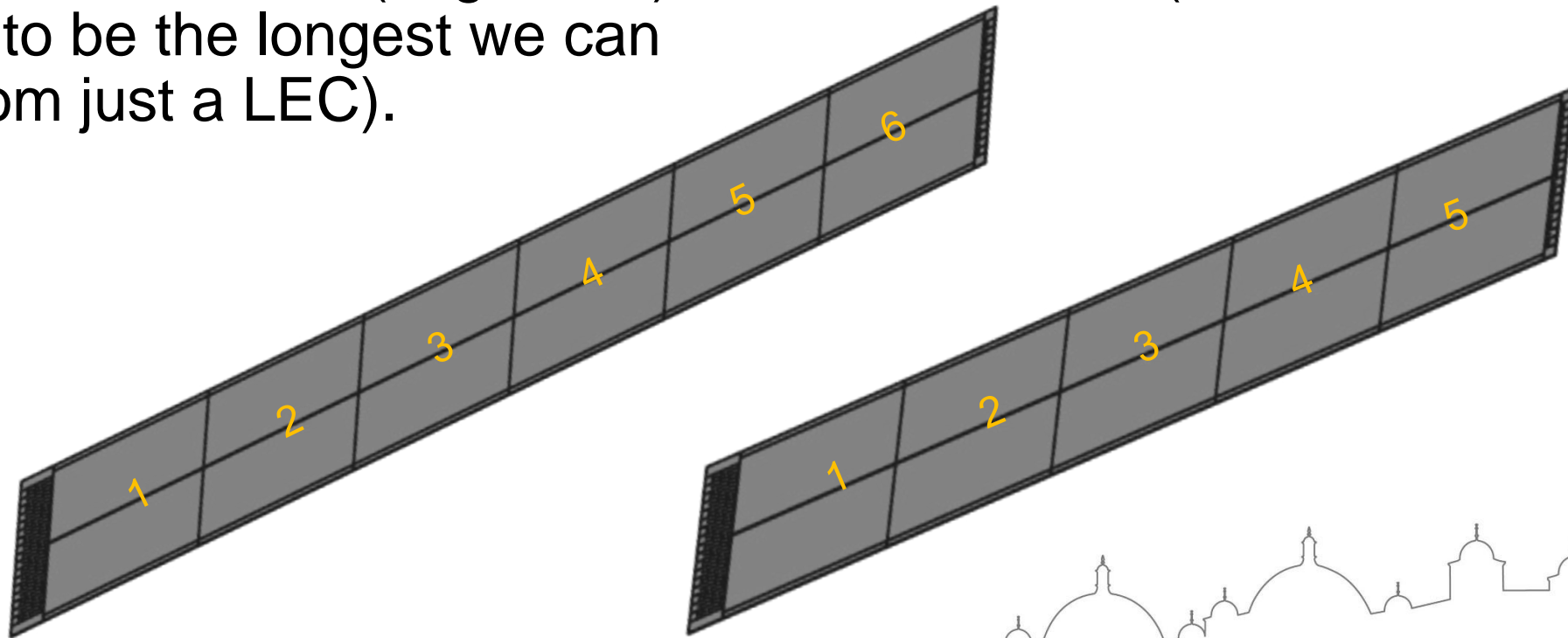
- 13Sep'23, EIC-UK WP1 meeting, J. Glover “Outer Barrel Layout Options”, <https://indico.bnl.gov/event/20497/>
- 27Sep'23, EIC-UK WP1 meeting, J. Glover “Update on layout studies”, <https://indico.bnl.gov/event/20654/>
- 12Oct'23, EIC-UK Meeting on outer layer mechanics, J. Glover “Current status of sensor geometry and associated layout concepts”, <https://indico.bnl.gov/event/20728/>
- 28Nov'23, ePIC SVT DSC meeting, J. Glover, “Update on OB stave layout and first thoughts on FPC”, <https://indico.bnl.gov/event/21355/>
- 20Marc'24, EIC-UK WP1 F2F meeting, J. Glover, “Layout (SVT with emphasis on OB)”, <https://indico.bnl.gov/event/22344/>



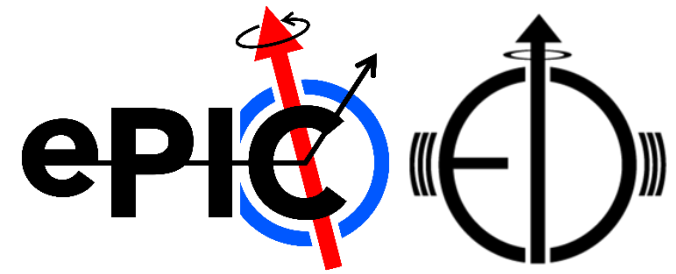
# 2 EIC-LAS lengths



- A segment is the name for the collection for stitched RSUs with both a left endcap (LEC, for power and data connections) and right endcap (REC, to terminate the stitching plan).
- Plan to have EIC-LAS (segments) with 5 or 6 RSUs (6 RSUs is believed to be the longest we can power from just a LEC).



# Including space for the AncASIC



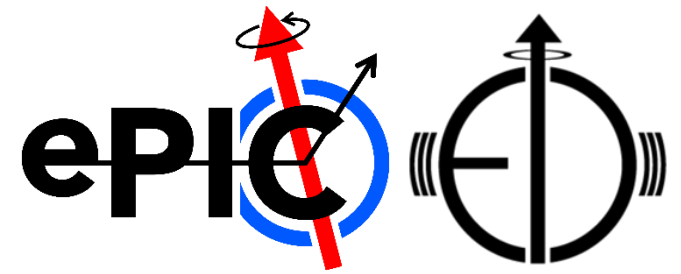
- A volume (10×10×5 mm) has been added to the design to account for the space needed to include the ancillary ASIC (AncASIC).
- Currently a 4.5 mm gap has been left between the LEC and the AncASIC.

A “module” consisting of 2 EIC-LAS (side-by-side), each with an AncASIC.



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# Clustering EIC-LAS in groups of 4



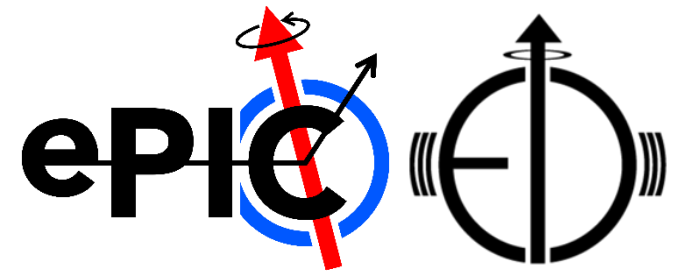
The flexible printer circuit (FPC) will be the interconnect between clusters of EIC-LAS. This needs:

- To enable the readout of data from many EIC-LAS to 1 VTRx+\*.
- Host the current to voltage regulation (for each EIC-LAS) and interconnections within a SP chain (AncASIC).
- Clusters of 4 EIC-LAS per SP chain work well with VTRx+ readout.



\* 4 read-out channels per VTRx+.

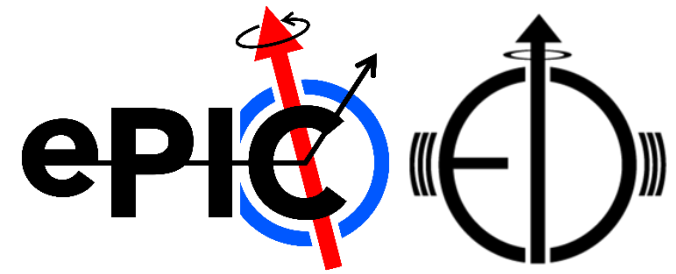
# Preferred stave layouts



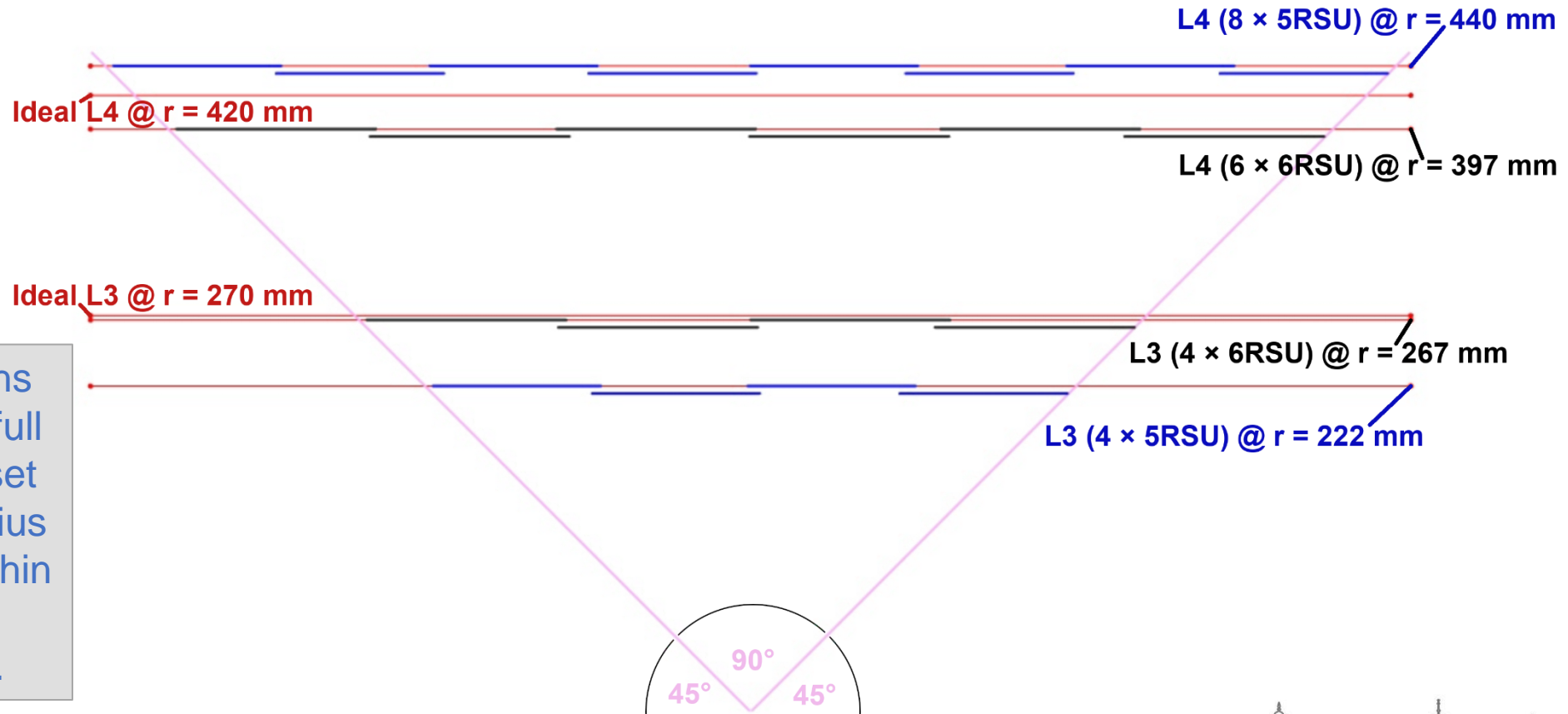
- Currently, it is preferred to use staves made of modules (2 EIC-LAS wide).
  - **L3** staves fit well when constructed from **4 modules** (in length), with EIC-LAS of **6RSUs**.
    - Totalling 8 EIC-LAS. 2 clusters of 4, aka **2 FPCs/stave**.
  - **L4** staves fit well when constructed from **8 modules** (in length), with EIC-LAS of **5RSUs**.
    - Totalling 16 EIC-LAS. 4 clusters of 4, aka **4 FPCs/stave**.
- Some active area (RSU) overlap required to keep full to keep full coverage (in Z-axis).
  - More overlaps needed to bring L4 down to required length (due to radii limitations).



# From Fri 15<sup>th</sup> March 2024

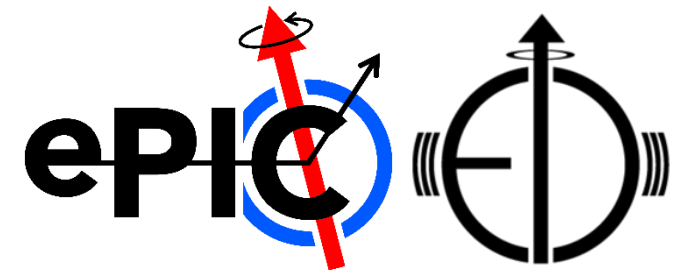


With the change to the stave lengths, what would be the best radii\*?

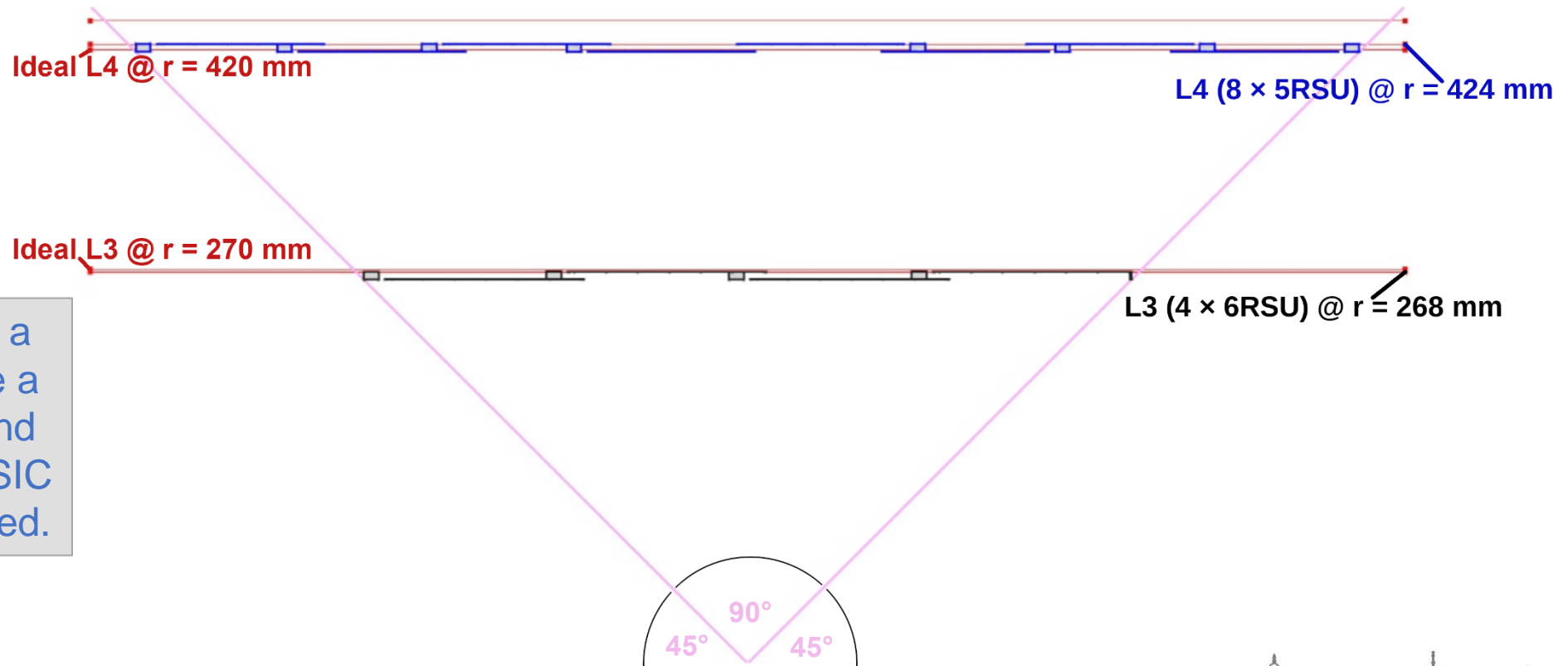


\* Module lengths overlapped for full coverage and set to minimum radius they could fit within the expected support cone.

# As of Wed 20<sup>th</sup> March 2024



Addition of AncASIC and fixing overlap to keep stave close to ideal radii.

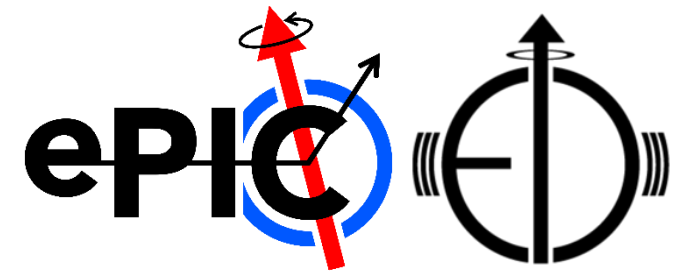


All modules on a stave now have a fixed overlap and space for AncASIC has been included.

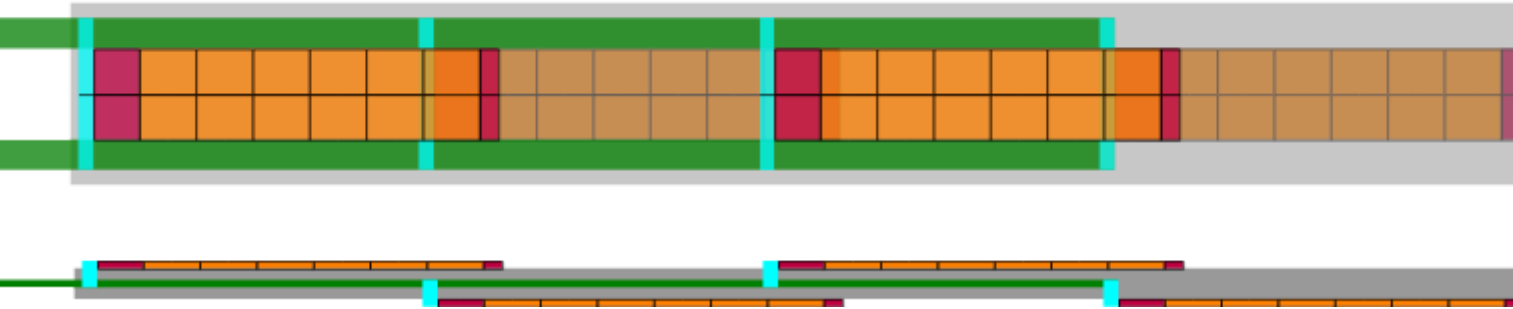




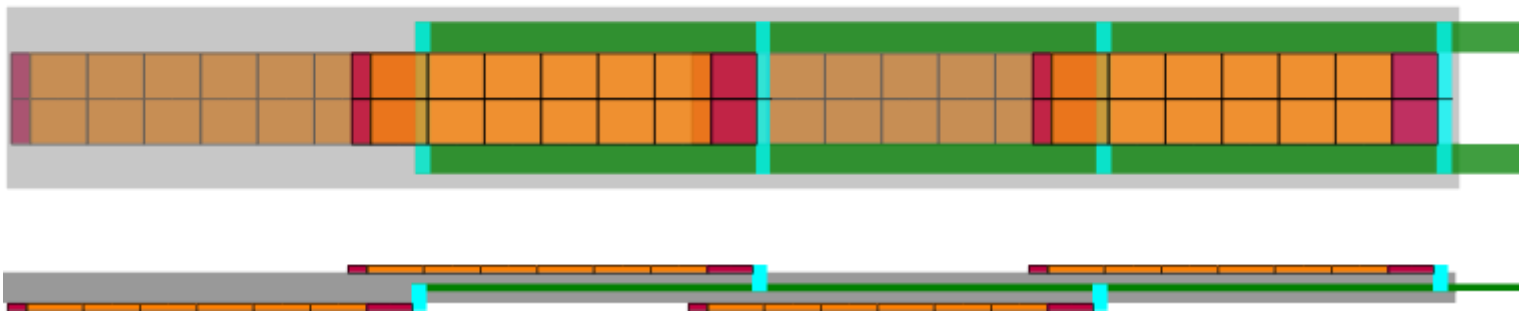
# L3 – Single sided readout



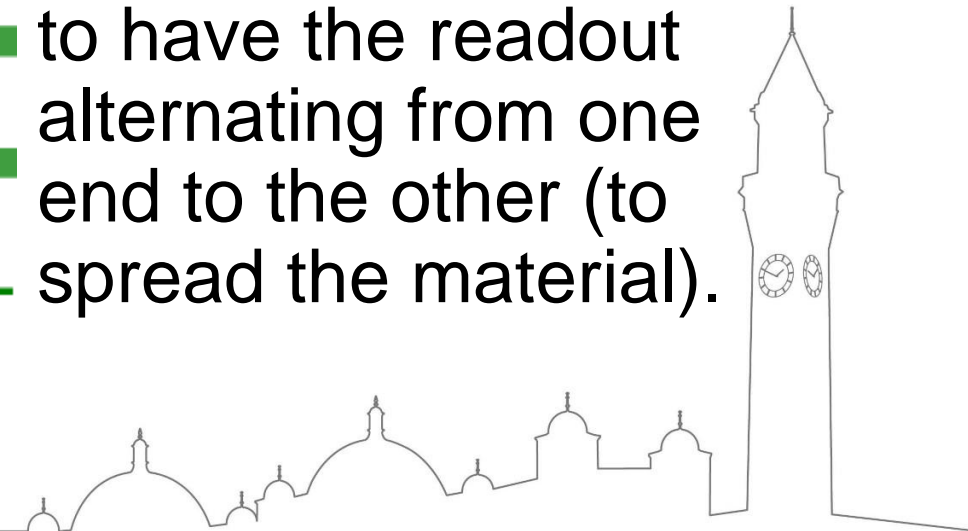
Layer 3 (EIC-LAS w. 6\*RSU) Stave N



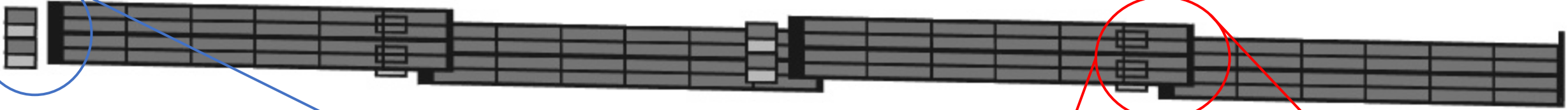
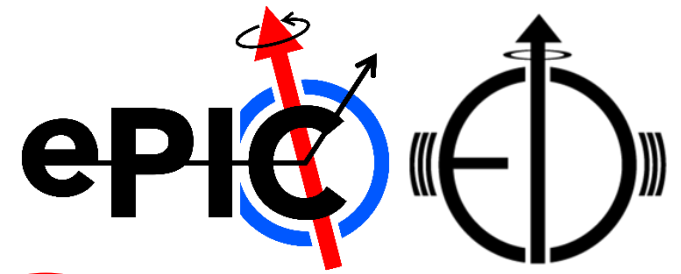
Layer 3 (EIC-LAS w. 6\*RSU) Stave N+1



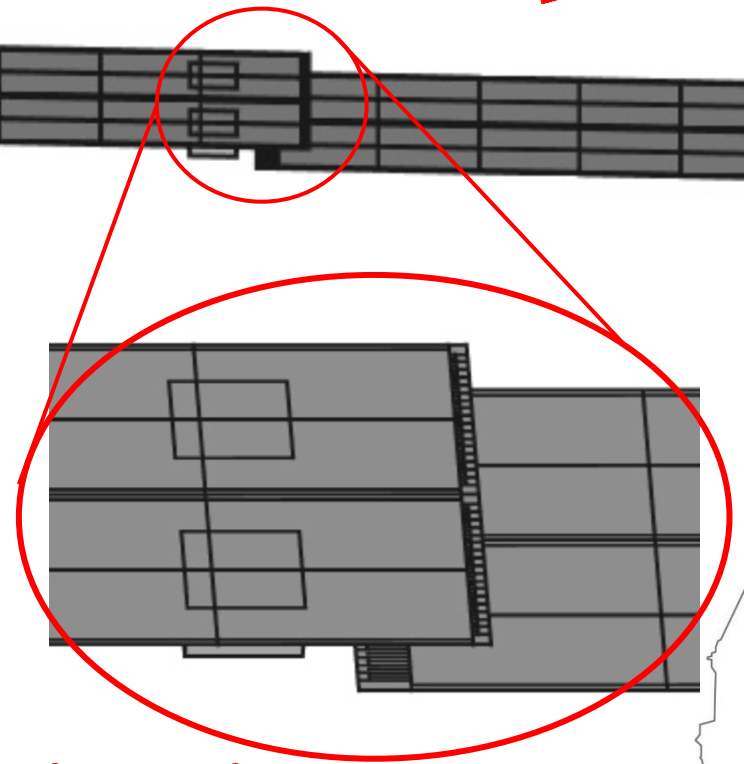
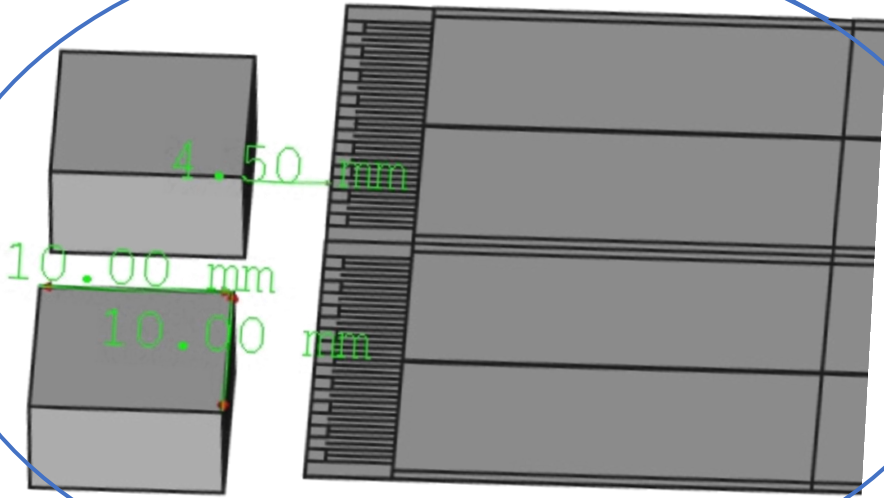
- To increase the active length readout for both FPCs can be on the same EOS side.
- This would require neighbouring staves to have the readout alternating from one end to the other (to spread the material).



# L3 – Spacing details



AncASIC set-up as a 10x10 mm chip. Spaced 4.5 mm from the EIC-LAS.

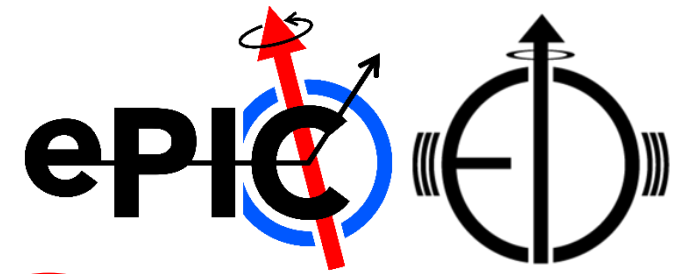


Active area overlap of 23% of an RSU length (~4.98 mm).

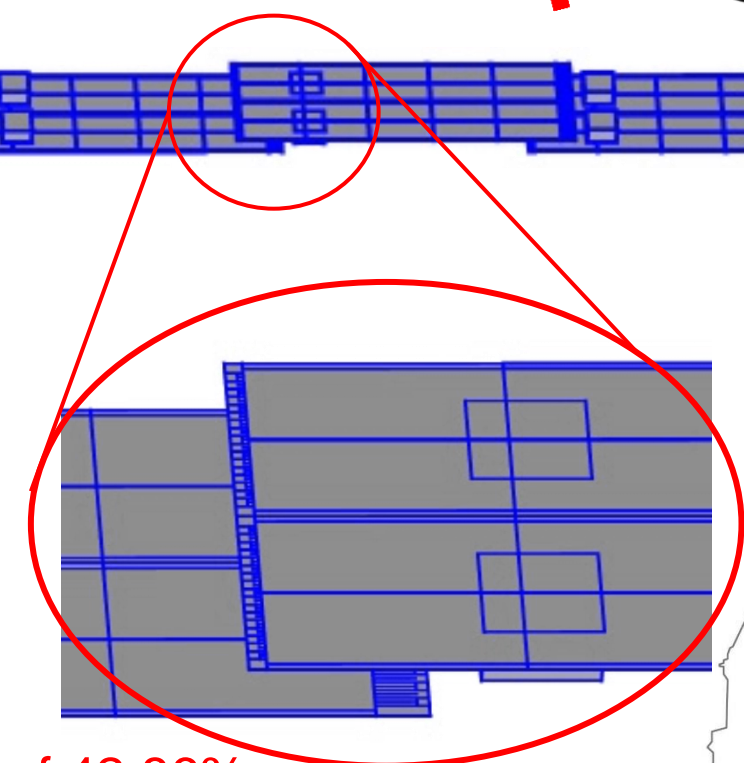
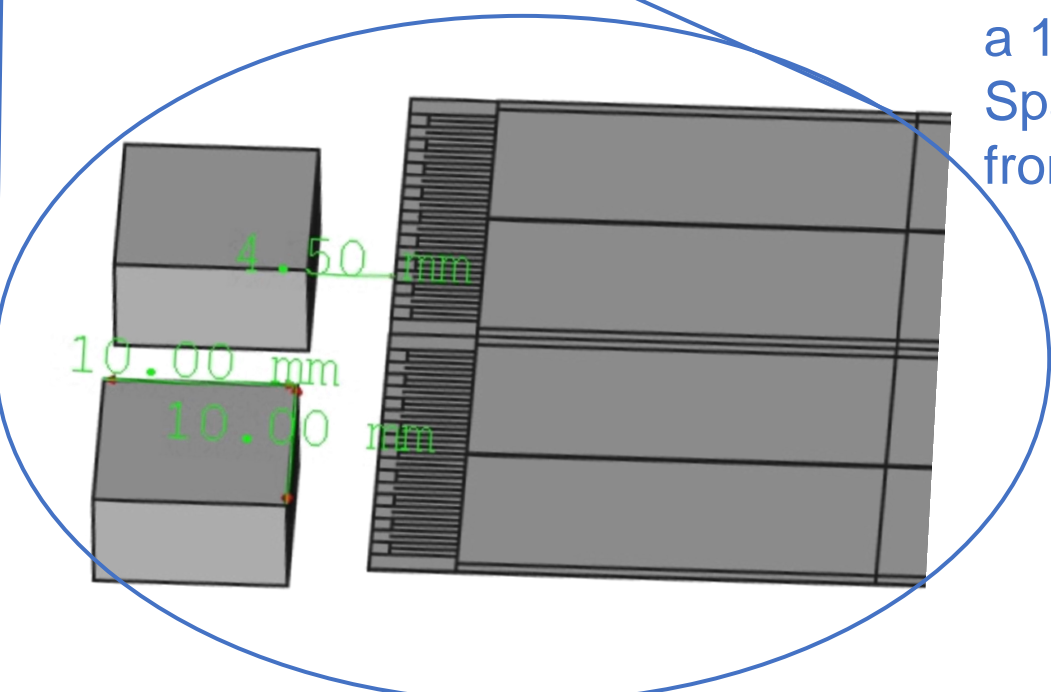
- RSU length: 21.66 mm
- RSU width: 19.56 mm



# L4 – Spacing details



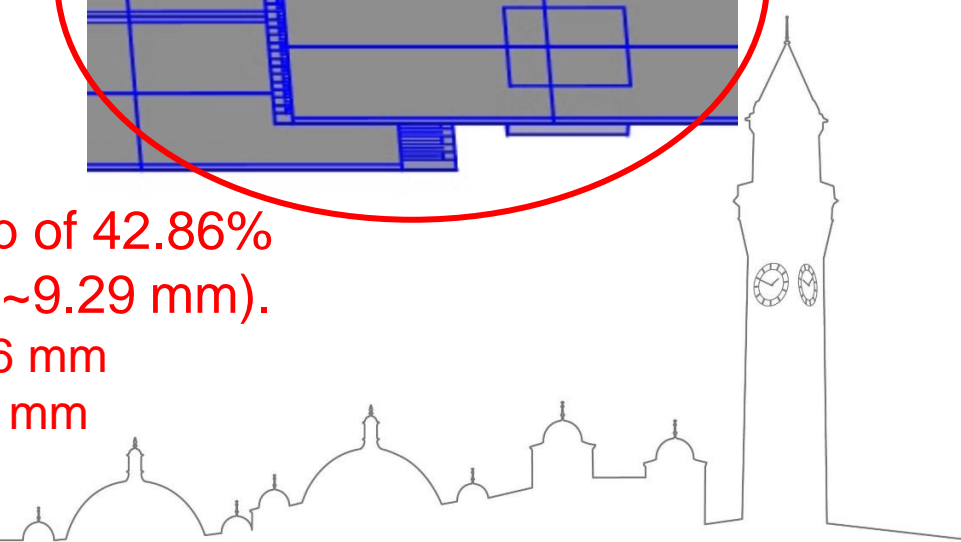
AncASIC set-up as a 10x10 mm chip. Spaced 4.5 mm from the EIC-LAS.



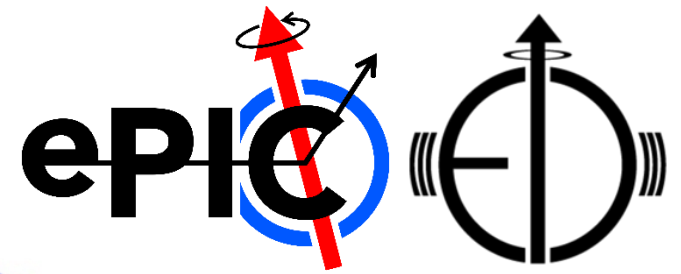
Active area overlap of 42.86% of an RSU length (~9.29 mm).

- RSU length: 21.66 mm
- RSU width: 19.56 mm

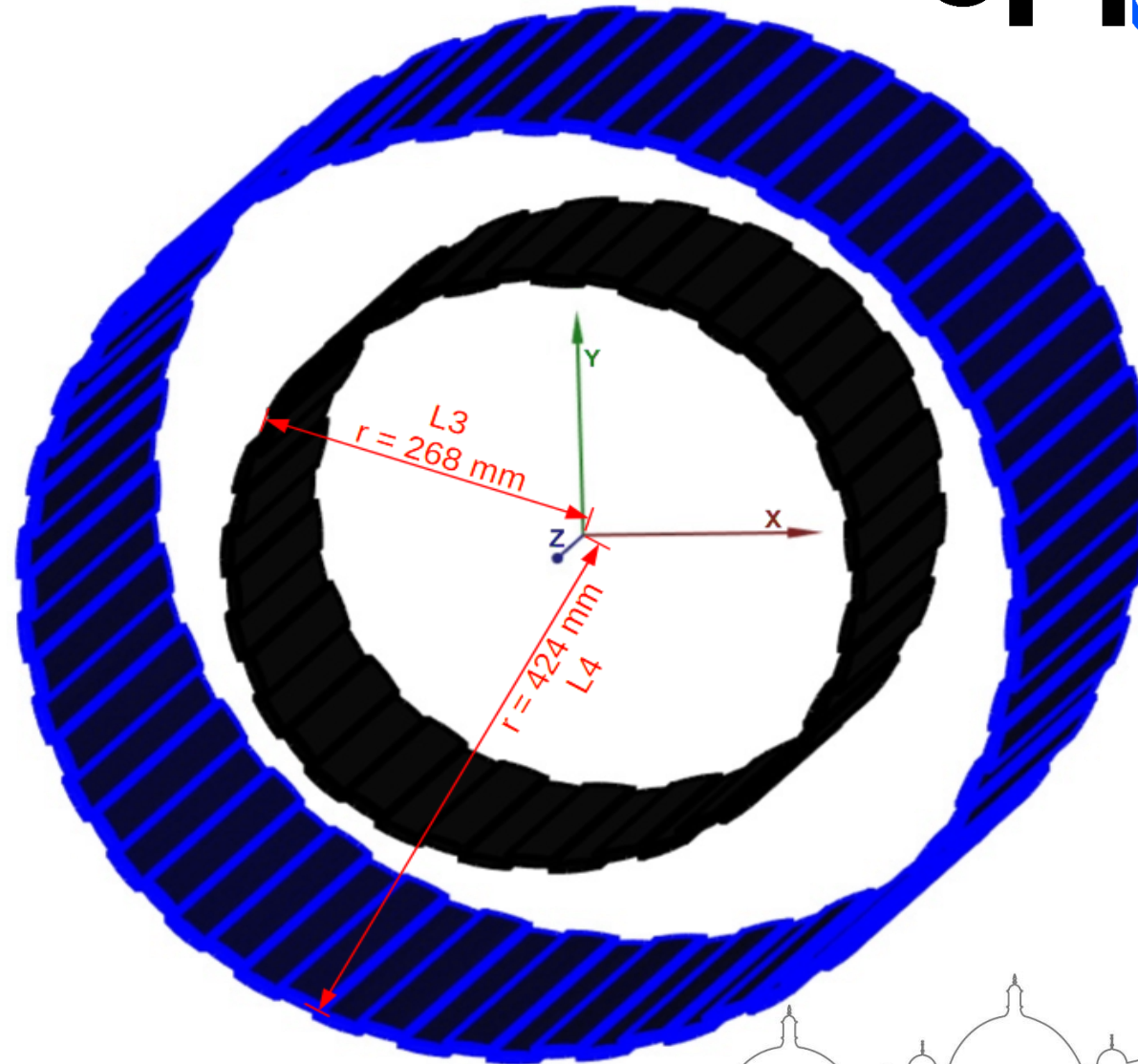
L4 will have double-sided readout.



# Outer barrel

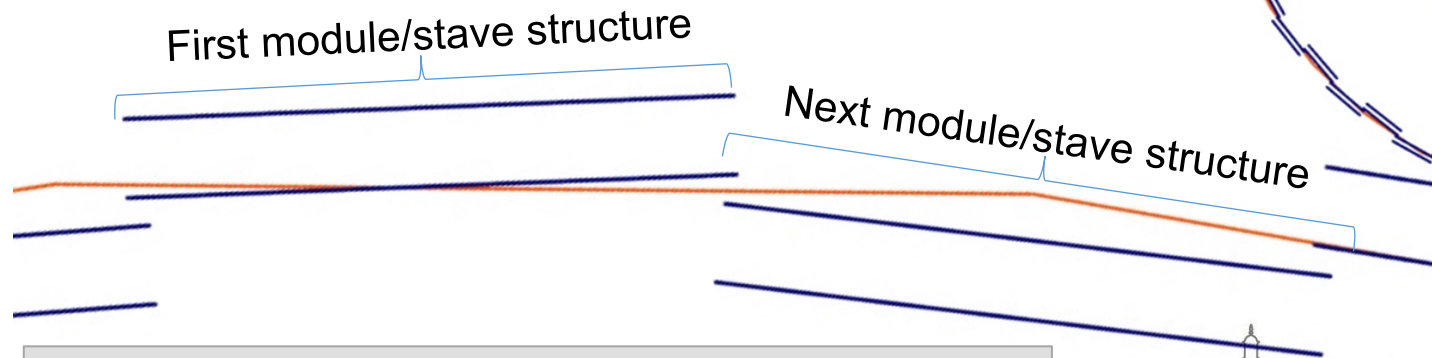
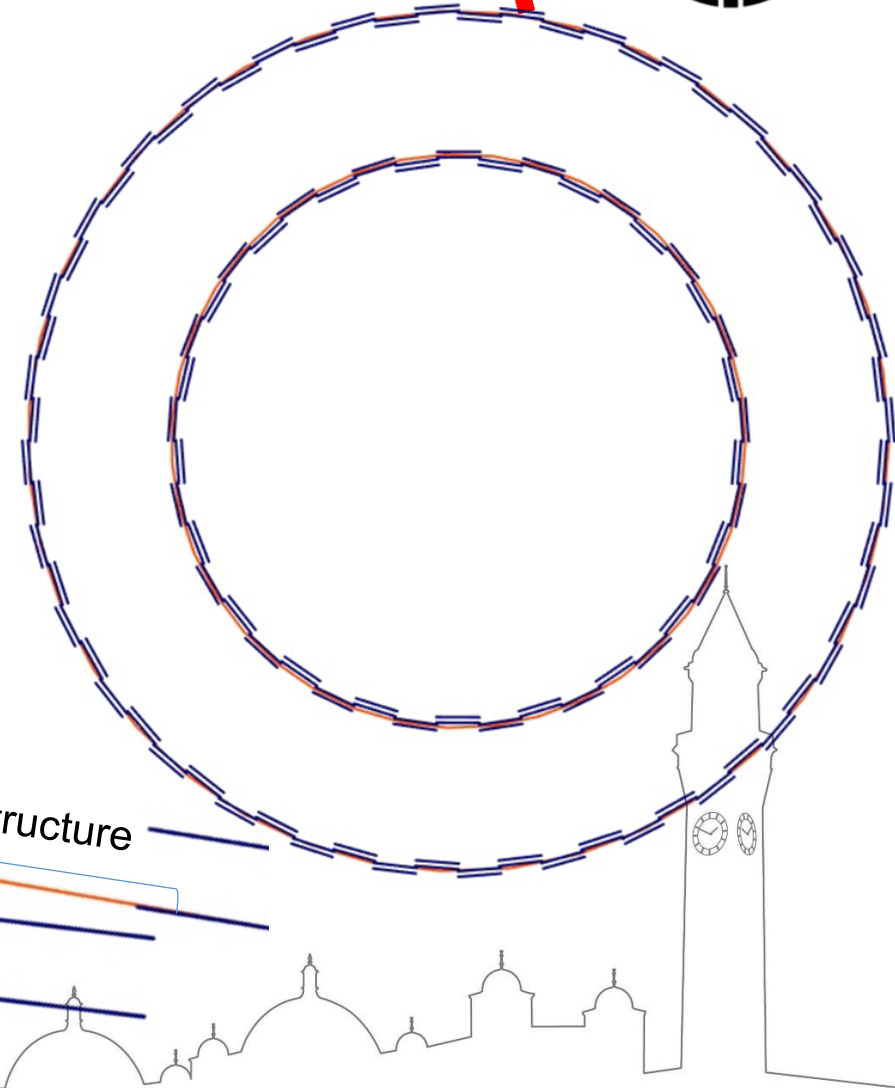
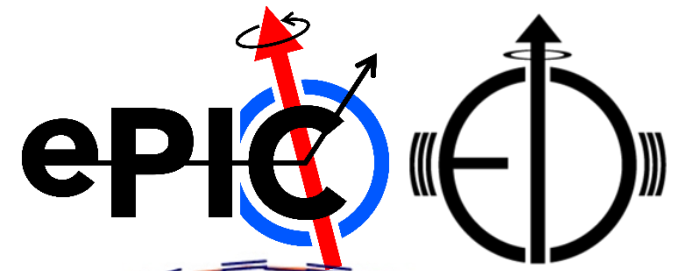


- 2 stave-based layers (L3 and L4) of stitched MAPS.
- Stave repeated around the Z-axis until number of staves fully cover the circumference (at required radii).



# Castellated layout

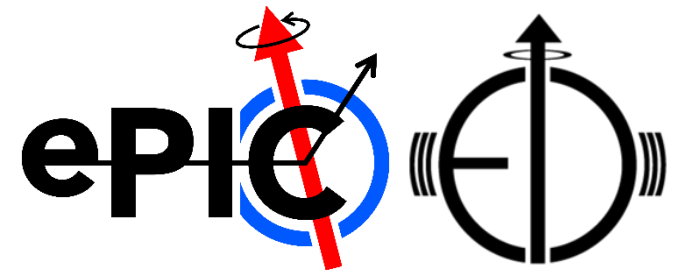
- Alternating inner/outer structure.
  - Easier mounting/replacing (at most 3 staves removed to replace 1).
  - Preferred\* for its “easier” mounting/replacing of staves.
- Number of staves **must be even**.
- Some overlap of staves (in both designs).
  - To account to dead area at the sensor’s edge.



\* Following layouts will focus on this structure.

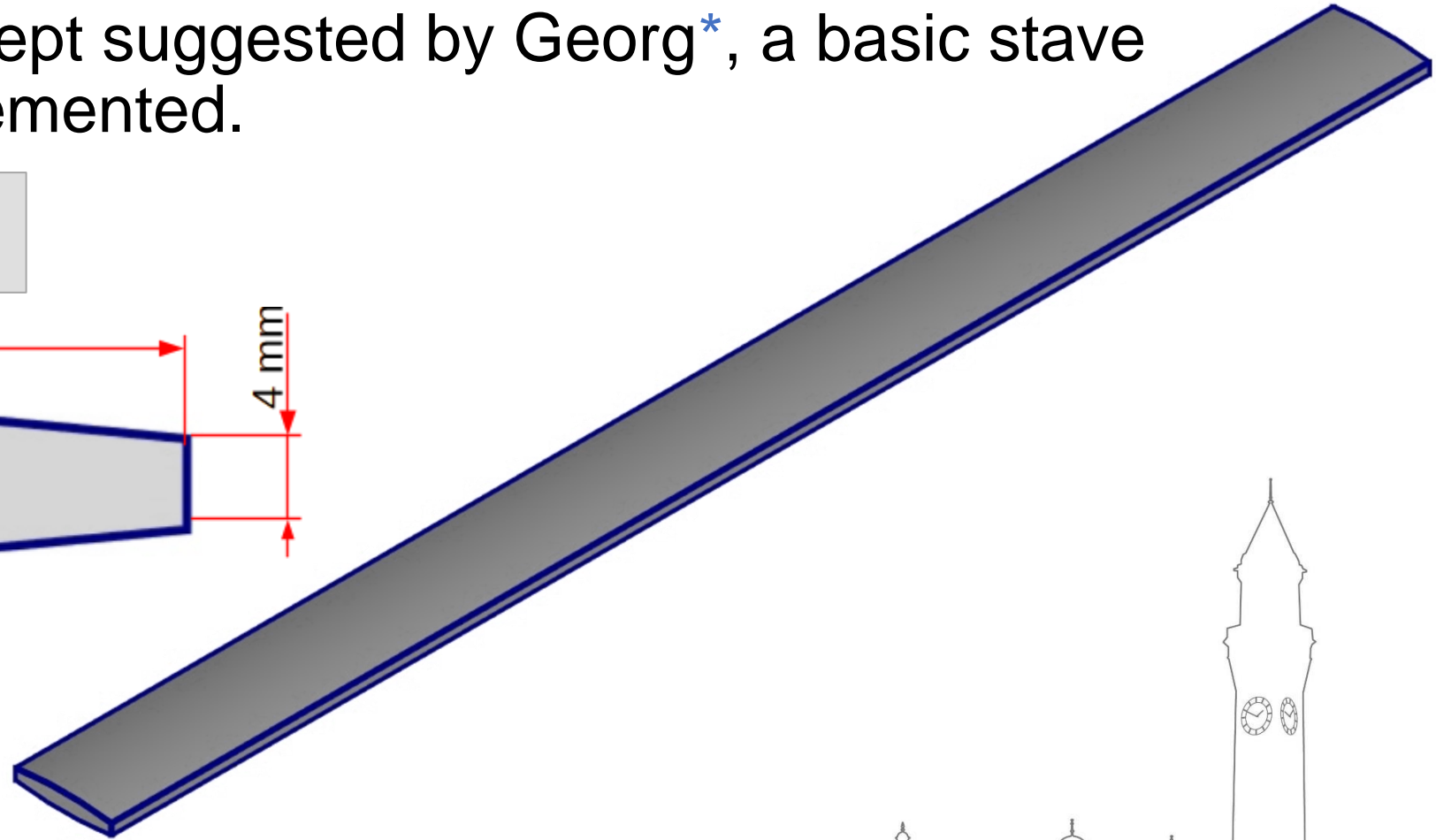
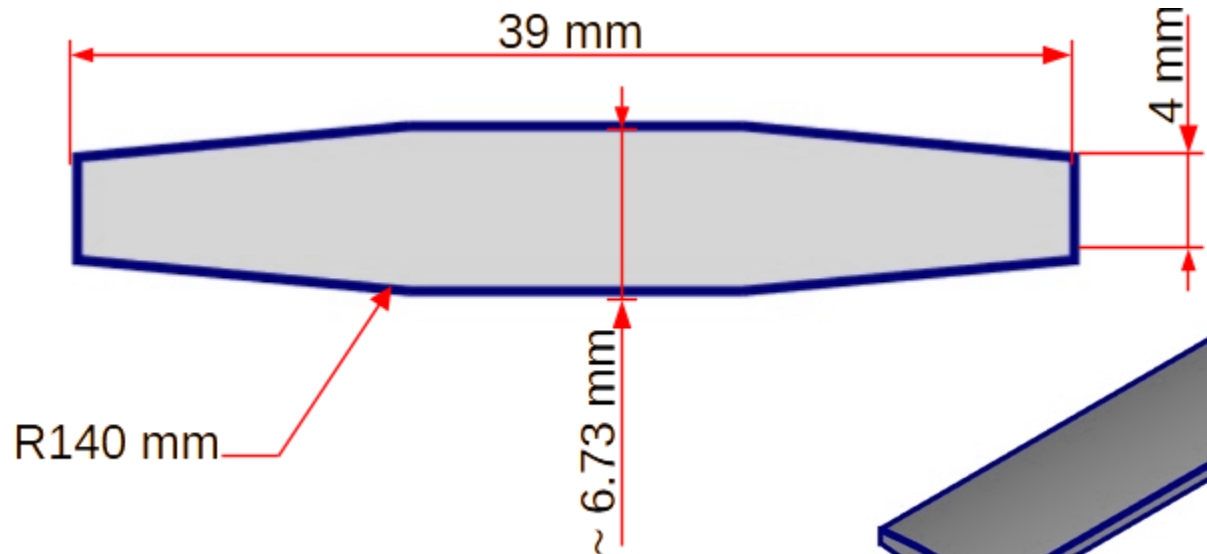


# Conceptual stave structure

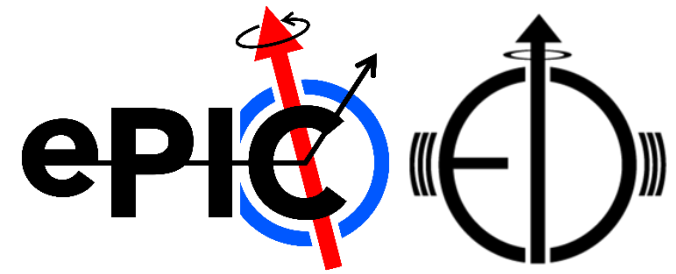


Based on a curved concept suggested by Georg\*, a basic stave structure has been implemented.

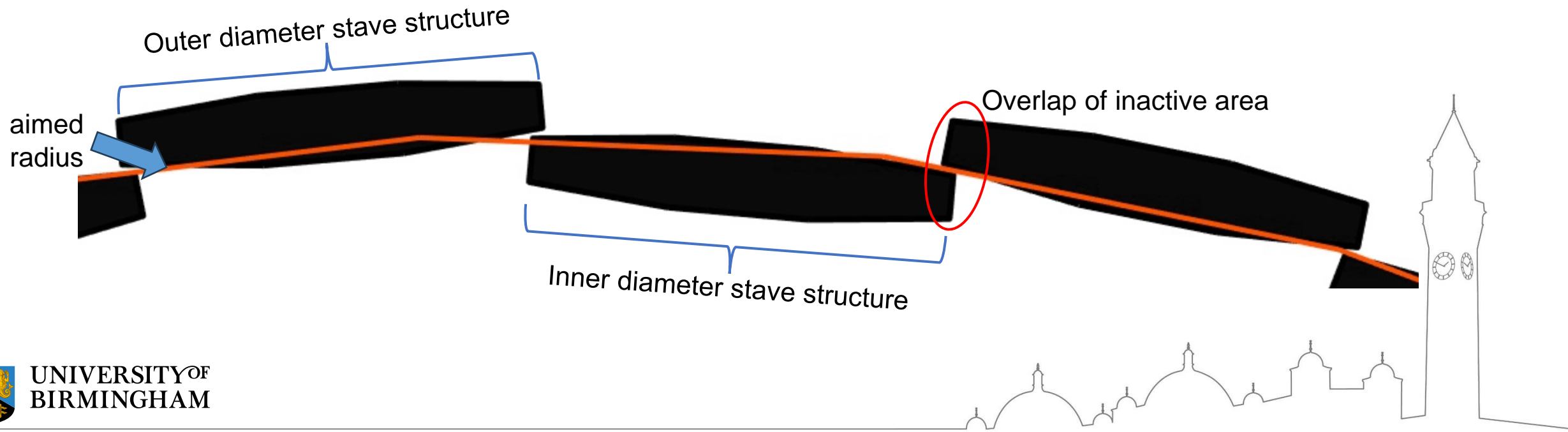
Curved surface width = 39.127 mm  
2 segment width =  $2 \times 19.56 = 39.12$  mm



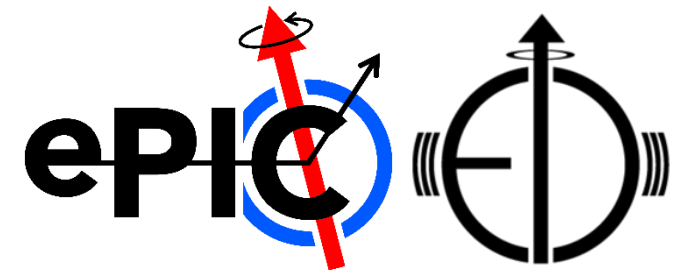
# Constructing the barrel layers



- From the [radii shown previously](#), repeated a structure of castellated pairs to obtain maximum (azimuthal) coverage.
- Observe how well pairs of staves fit at each radii.



# Structural findings



Layer	Radial Aim	Inner Radii	Outer Radii	#RSU per EIC-LAS	#Staves per layer	#EIC-LAS per layer
L3	268 mm	261 mm	274 mm	6RSU-LAS	44	352 (8/stave)
L4	424 mm	417 mm	430 mm	5RSU-LAS	70	1120 (16/stave)

Azimuthal overlap between neighbouring staves is 200-400  $\mu\text{m}$ .  
(200  $\mu\text{m}$  of dead-space runs along the edge of the silicon)

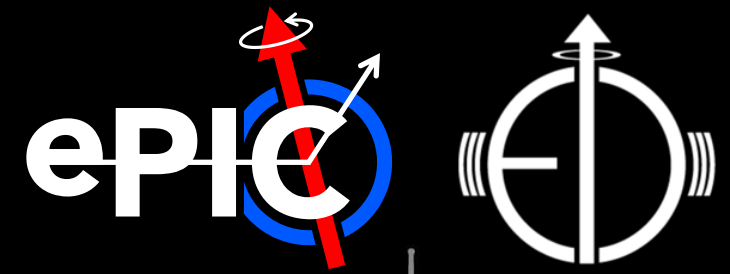
Reducing L4 radius to 420 mm, overlaps become (O)600  $\mu\text{m}$ .







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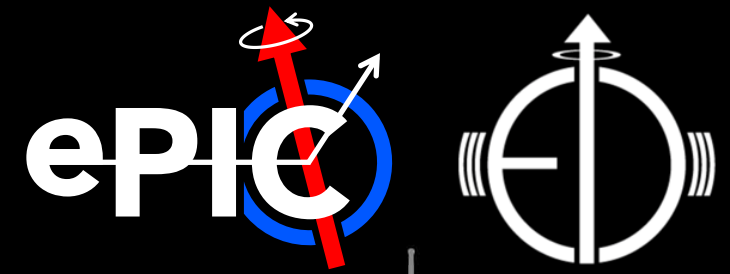
# Thank you very much!

Any questions?





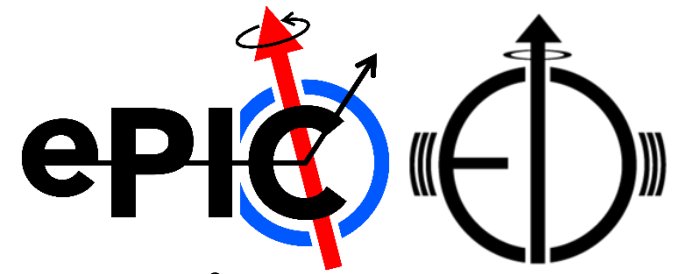
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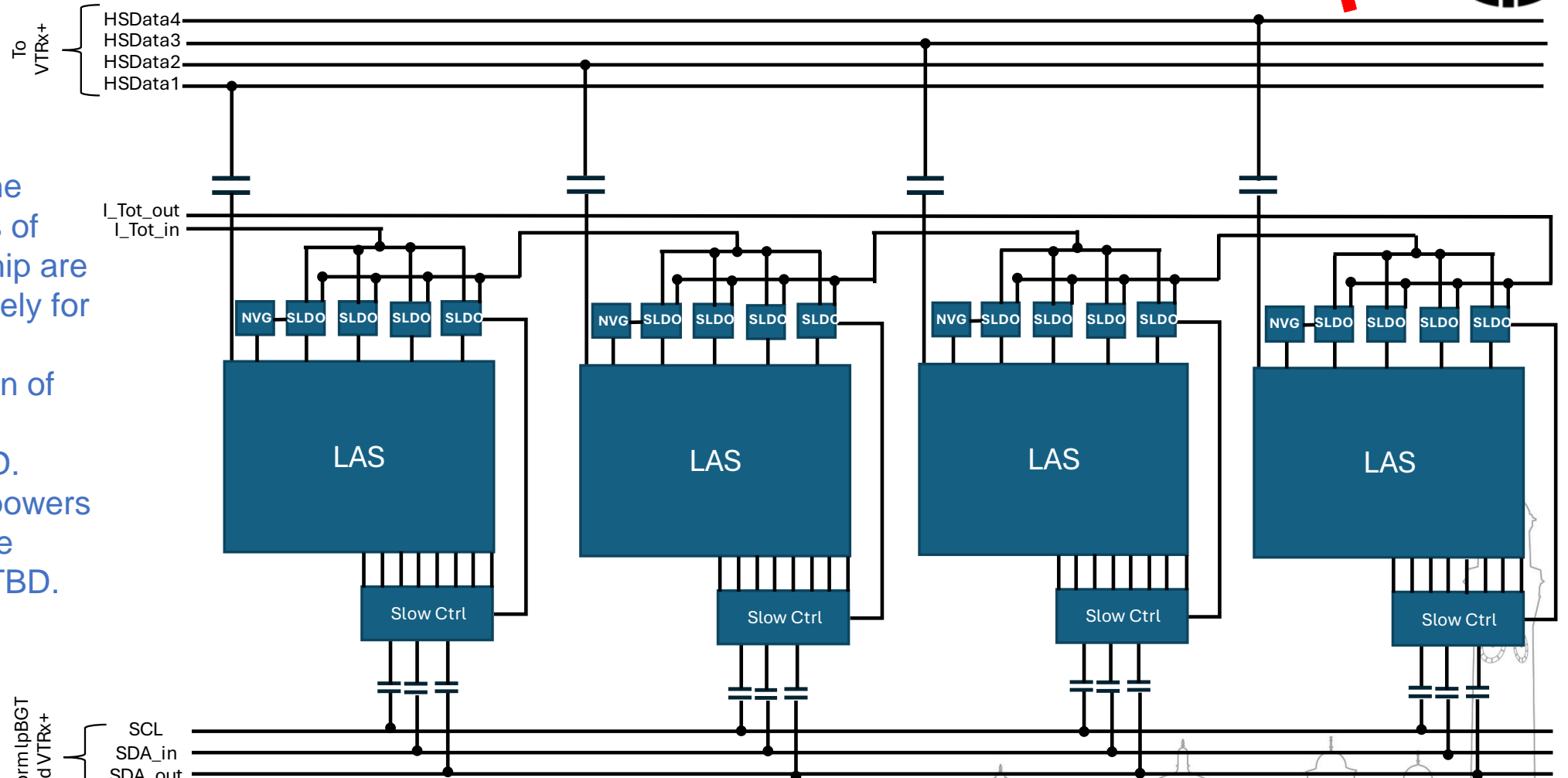
Additional (support) slides



# EIC-LAS connections on FPC



- On this slide the three functions of the ancillary chip are shown separately for clarity.
- Precise location of AC-coupling capacitors TBD.
- Which SLDO powers what part of the auxiliary chip TBD.



Schematic drawing by Marcello Borri (STFC)

