ROC reinstallation and ladder tests – South side –

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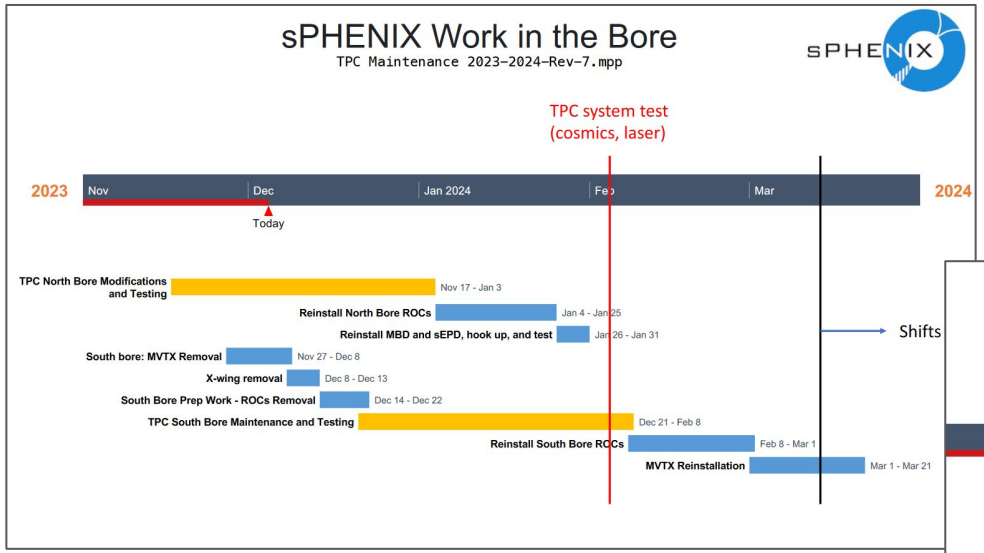
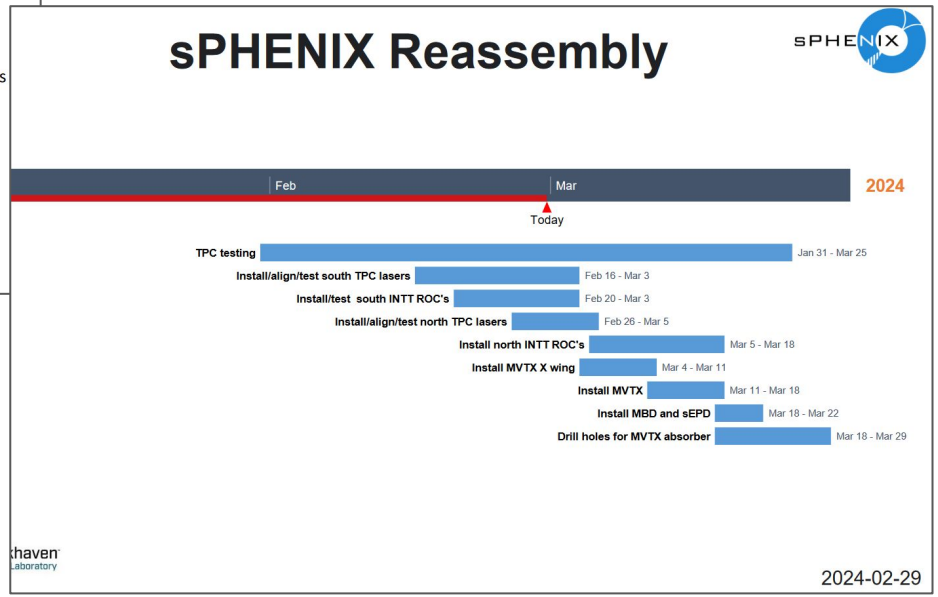
Schedule

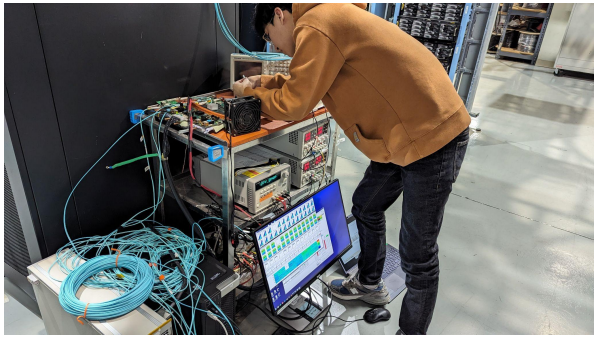


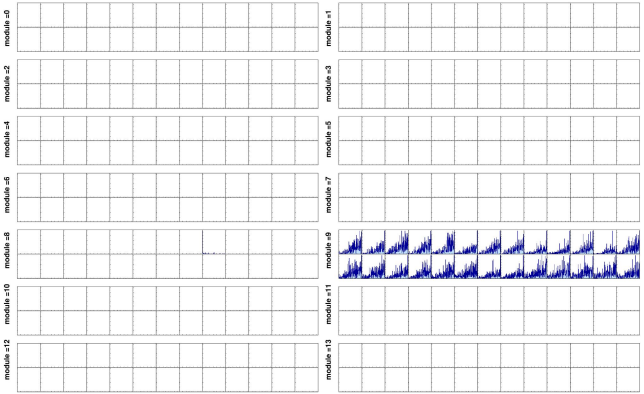
Schedule shown in the last collaboration meeting (Dec/2023).
21 (south) and 22 (north) days were given for us.

The latest schedule.



Diary





The first noise data (Feb/24, Run30273, intt0, bias ON)

before reinstallation: Tests with the rack room testbench.

Feb/22: ROC reinstallation started/

Feb/23: 8 ROCs were placed. Cooling started working. LV/HV tests done.

Feb/24: The first ladder test but failed.

Feb/25: Discovery: FPHX needs power😅

Feb/27: 2 Shifts work (morning–afternoon, afternoon-night) stated. Testing intt2 ladders completed.

Feb/28: ROC-0S was changed from #18 to #6(?). Testing RC-1S ladders finished.

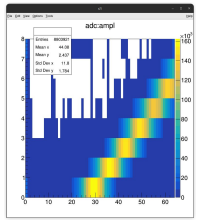
Feb/29: FPHX power cable of RC-0S J2A was found to be unconnected. Testing intt3 ladders was over.

Mar/1: Raul was back and took calibration data immediately.

Mar/4: Testing intt0 and intt1 ladders was finally done. **All ladders on the south side were tested and reasonable pedestal distributions were obtained.**

All works were proceed in 8 weekdays + 2 weekend.

We are halfway there!



ROC reinstallation

ROC reinstallation was done mainly by Jeff and Rachid (correct?). They used the reinstallation checklist, so we should have information.

There is no major change of ROCs, and cable assignments.

Unfortunately, we didn’t have enough time to make HV maps. They are almost same as last year, but some may be changed (Rachid knows well).

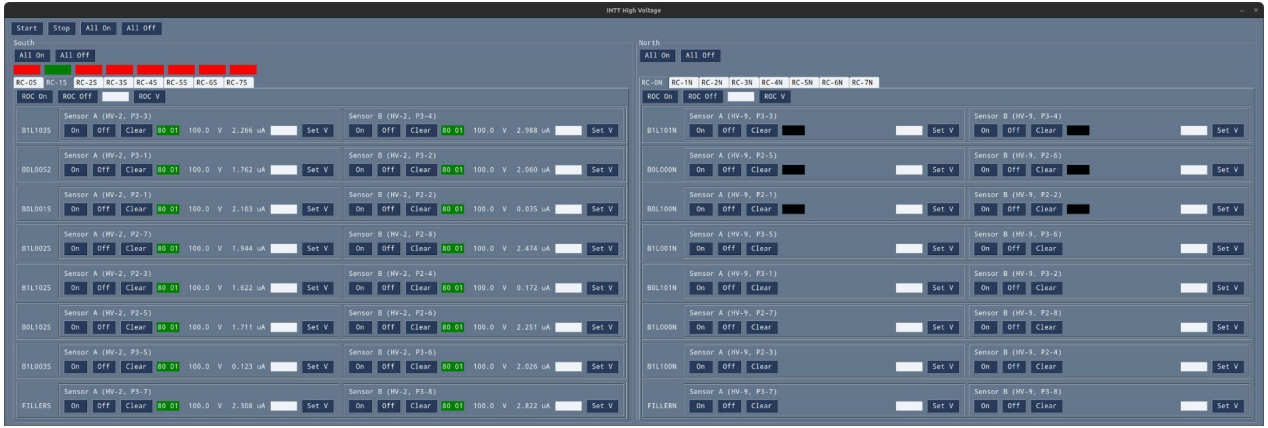
Rachid and Steve worked on grounding. It has to be reported in the INTT meeting.

LV / HV

They worked well basically.

LV sometimes showed strange behavior (due to ROC GND?). Any news?

HV GUI works without any problems. The ladder labels need to be updated if possible. Logging feature is coming.



Ladder map (/home/phnxrc/INTT/map_ladder/2024)

intt0

FELIX CH	ROC	ROC port	Ladder
0	RC-0S #18	D2	B1L101S
1		C1	B0L101S
2		C2	B1L001S
3		C3	B1L000S
4		A2	B1L100S
5		B1	B0L000S
6		A1	B0L100S
7	RC-1S #19	C2	B1L103S
8		C1	B0L002S
9		A1	B0L001S
10		B3	B1L002S
11		A2	B1L102S
12		B1	B0L102S
13		D2	B1L003S

Change from last year:
- B1L000S: B3 → C3

intt1

FELIX CH	ROC	ROC port	Ladder
0	RC-0S SE2	C2	B1L105S
1		C1	B0L104S
2		A2	B0L103S
3		B3	B1L004S
4		A1	B1L104S
5		B1	B0L003S
6		D2	B1L005S
7	RC-1S SW5	C2	B1L107S
8		C1	B0L005S
9		A1	B0L004S
10		B3	B1L006S
11		A2	B1L106S
12		B2	B0L105S
13		D1	B1L007S

Change from last year:
- B1L006S: B2 → B3
- B0L105S: B1 → B2

intt2

FELIX CH	ROC	ROC port	Ladder
0	RC-0S #29	A1	B0L106S
1		B1	B0L006S
2		C1	B0L107S
3		A2	B1L108S
4		B2	B1L008S
5		C2	B1L109S
6		D1	B1L009S
7	RC-1S #23	A1	B0L007S
8		B3	B0L108S
9		C1	B0L008S
10		A2	B1L110S
11		B2	B1L010S
12		C2	B1L111S
13		C3	B1L011S

Change from last year:
- none

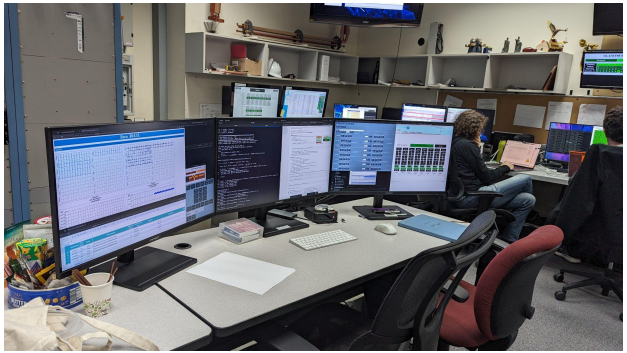
intt3

FELIX CH	ROC	ROC port	Ladder
0	RC-0S #13	A1	B0L109S
1		B1	B0L009S
2		C1	B0L110S
3		A2	B1L112S
4		B3	B1L012S
5		C2	B1L113S
6		D1	B1L013S
7	RC-1S #3	A1	B0L010S
8		B1	B0L111S
9		C1	B0L011S
10		A2	B1L114S
11		B3	B1L014S
12		C3	B1L115S
13		D2	B1L015S

Change from last year:
- none

Ladder tests

We couldn’t take calibration data without Raul unfortunately, we took pedestal data with RCDAQ as ladder tests. So we could check



- LV and HV
- Connection of conversion cables
- Slow control commands (by changing DAC0)
- reaction by FPHX chips
- signals from silicon strips

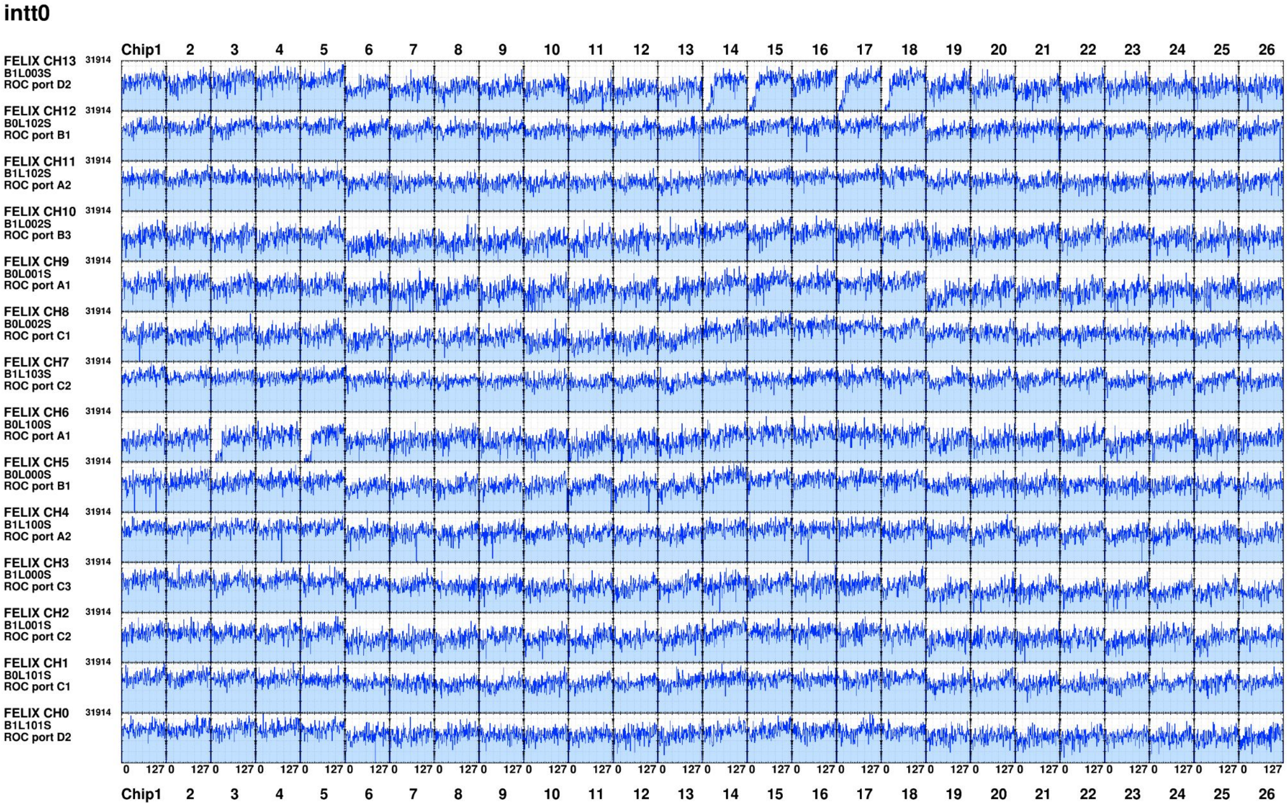
Raw data was stored in the buffer box (/bbox/bbox?/INTT/).Raw data was sent to the SDCC storage (/sphenix/lustre01/sphnxpro/commissioning/INTT/) and decoded. Hit-base ROOT files are in /sphenix/u/nukazuka/INTT/data/root_files/2024. Plots were generated with FelixQuickViewer. You can see them here (SSH tunnel needed).

Ladder tests
(Run 31749, Mar/5 4 pm)

DAC0 = 10
measurement for 3 sec
bias ON
n_collision 128
open_time 128

```
Modebit:
 0     0     0   0
 1     0     0   0    0: 0x36;95: 0x35;
 2     1500  0   0
 3     0     0   0    0: FA;
 4     150   1   3
```

intt0

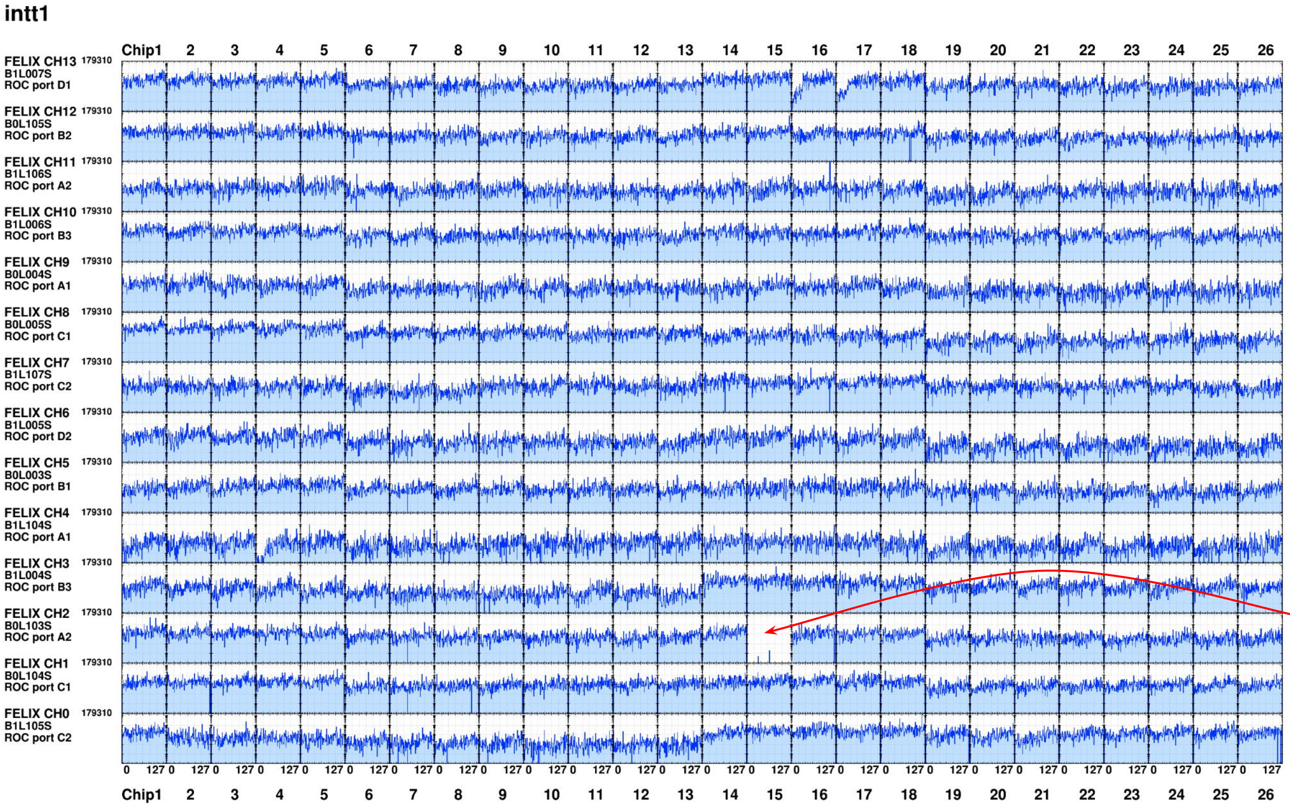


Ladder tests
([Run 31749](), Mar/5 4 pm)

DAC0 = 10
measurement for 3 sec
bias ON
n_collision 128
open_time 128

```
Modebit:
 0      0      0   0
 1      0      0   0    0: 0x36;95: 0x35;
 2      1500   0   0
 3      0      0   0    0: FA;
 4      150    1   3
```

intt1



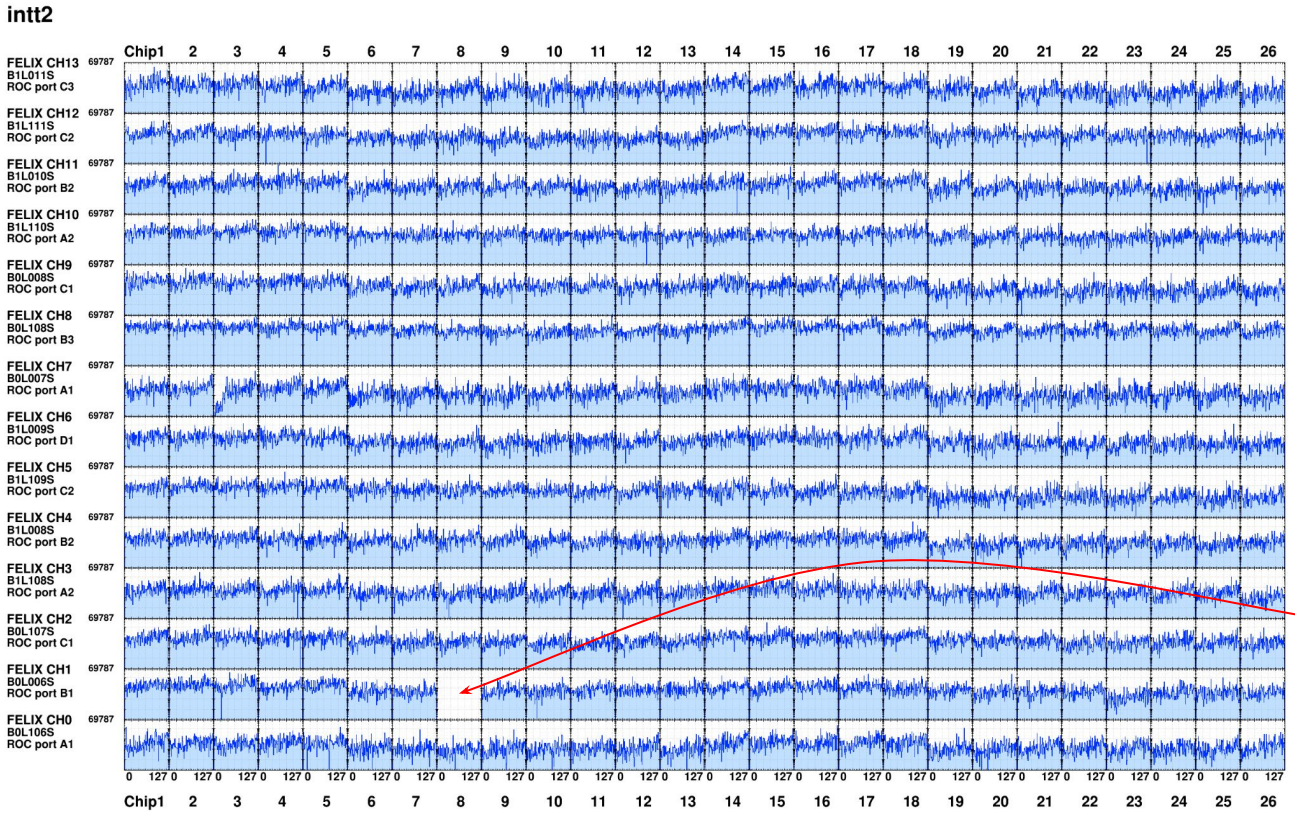
Ch 0 is too noisy and out of control. This chip is not reliable.

Ladder tests
(Run 31749, Mar/5 4 pm)

DAC0 = 10
measurement for 3 sec
bias ON
n_collision 128
open_time 128

```
Modebit:
 0      0       0    0
 1      0       0    0    0: 0x36;95: 0x35;
 2      1500    0    0
 3      0       0    0    0: FA;
 4      150     1    3
```

intt2



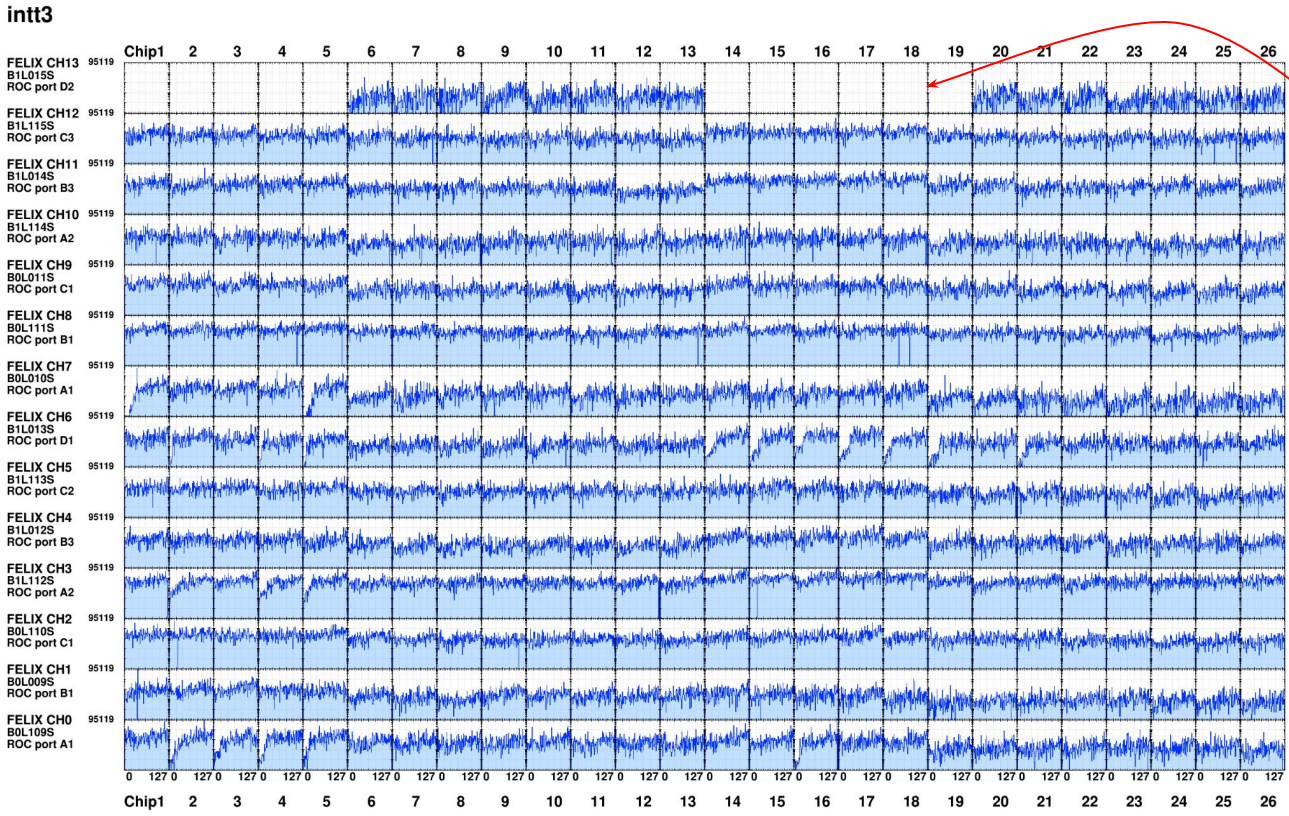
Ch 0 is too noisy and out of control. This chip is not reliable.

Ladder tests
(Run 31749, Mar/5 4 pm)

DAC0 = 10
measurement for 3 sec
bias ON
n_collision 128
open_time 128

```
Modebit:
 0      0      0   0
 1      0      0   0    0: 0x36;95: 0x35;
 2      1500   0   0
 3      0      0   0    0: FA;
 4      150    1   3
```

intt3

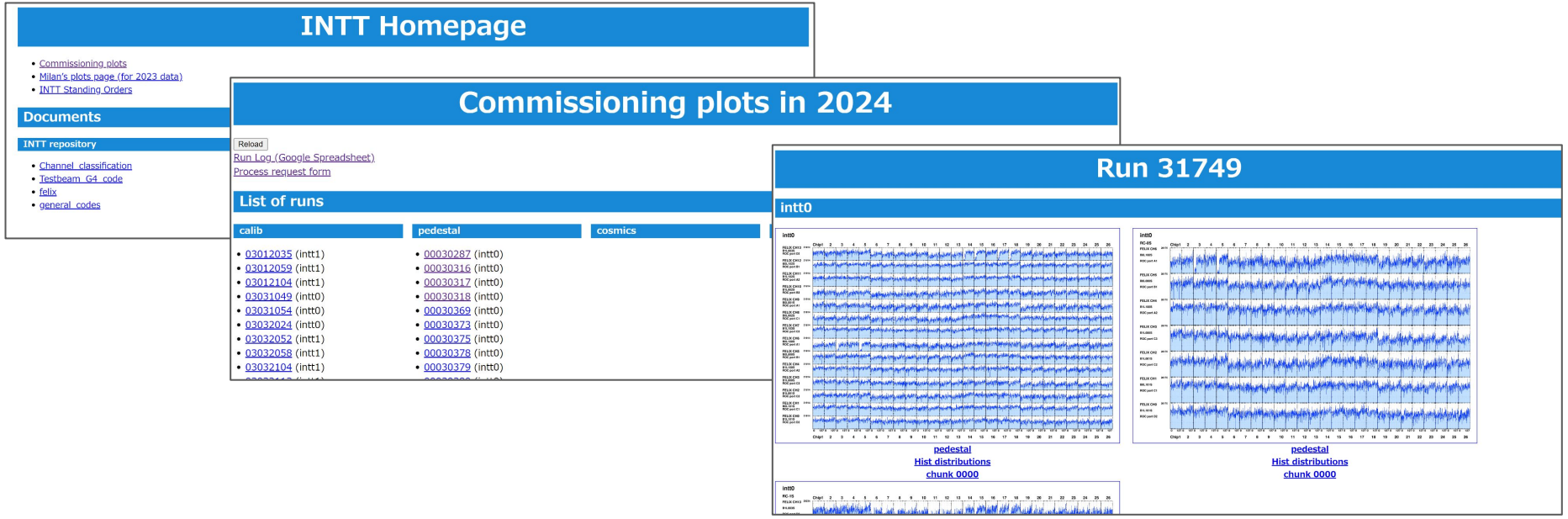


These missing chips are same as last year.

Plots

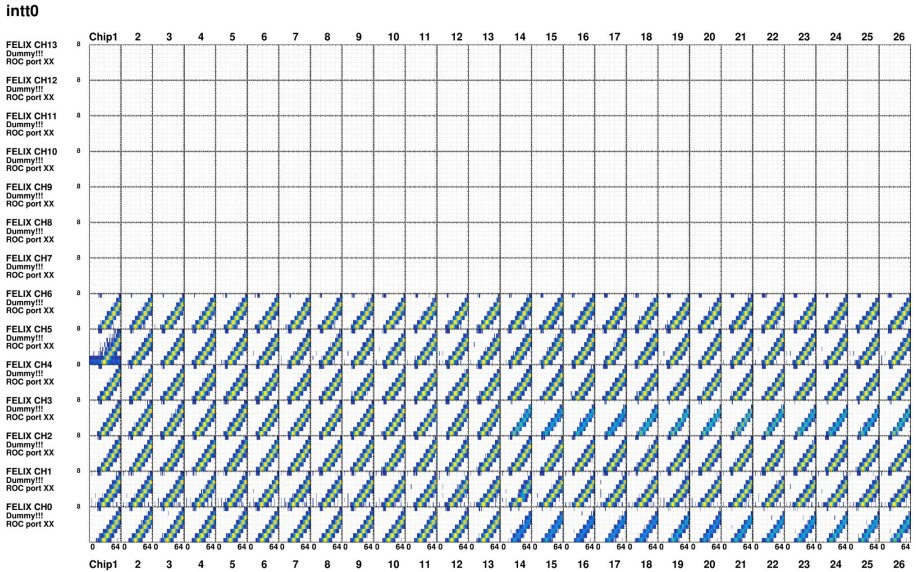
I made a homepage to check plots easily. To access it,

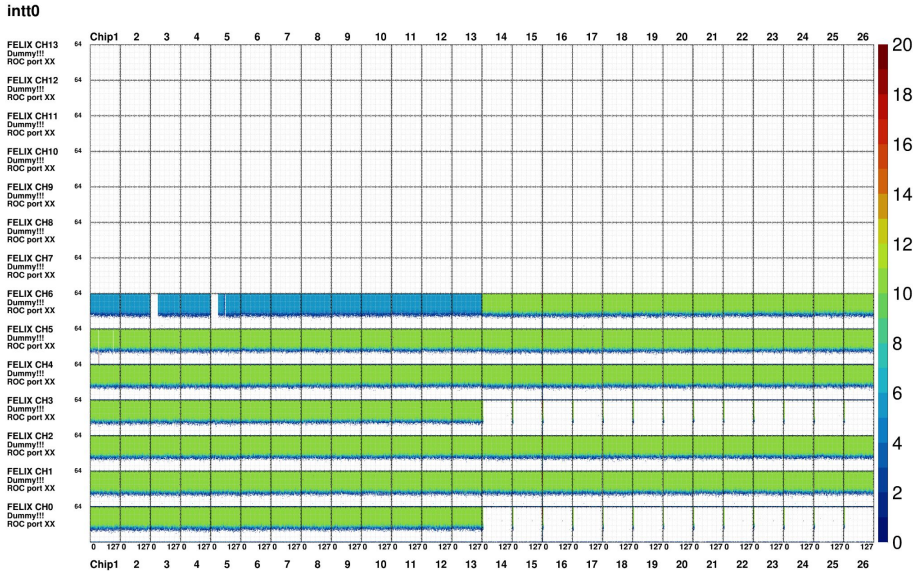
1. Open INTT Hopemage (https://sphenix-intra.sdcc.bnl.gov/WWW/subsystem/intt/)
2. Go to commissioning pots → 2024
3. Select a run



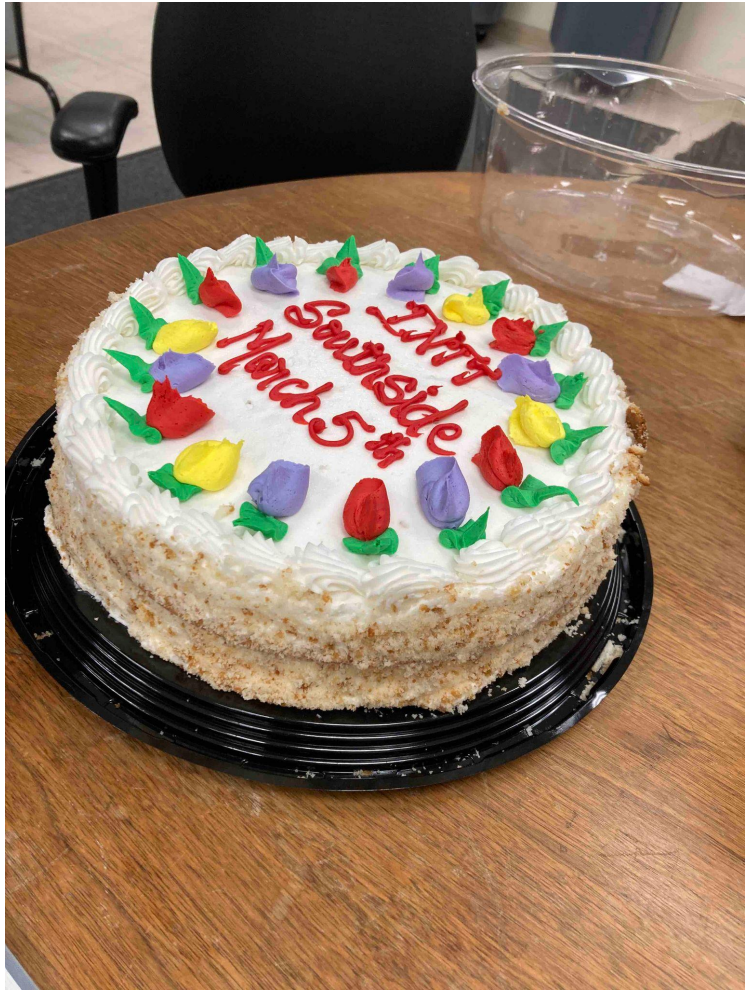
Calibration measurement

Raul could obtain calibration data with RaulDAQ (simple python macro) but not RCDAQ. We also got calibration data by ourself with only intt0. More investigation is needed.





Run 3042036 (different naming schema) taken by INTT team without Raul.



what's next?😇😈