SiPM Biasing in ePIC Fwd (& Bwd tbd) ECAL and STAR FCS

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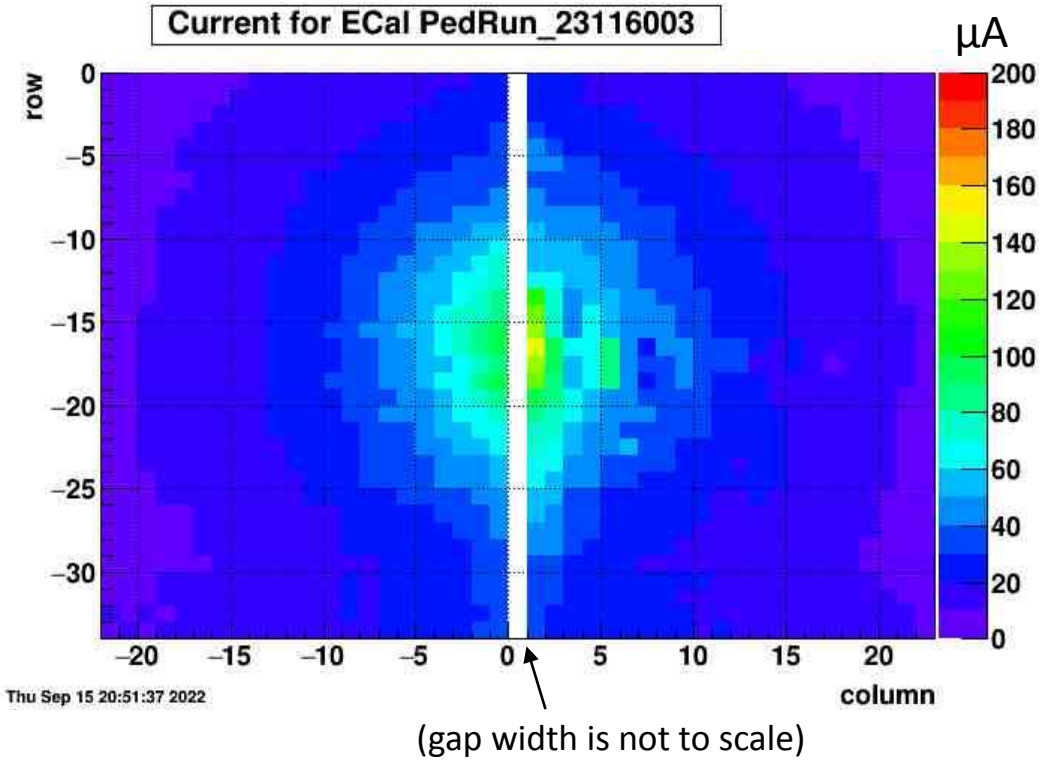
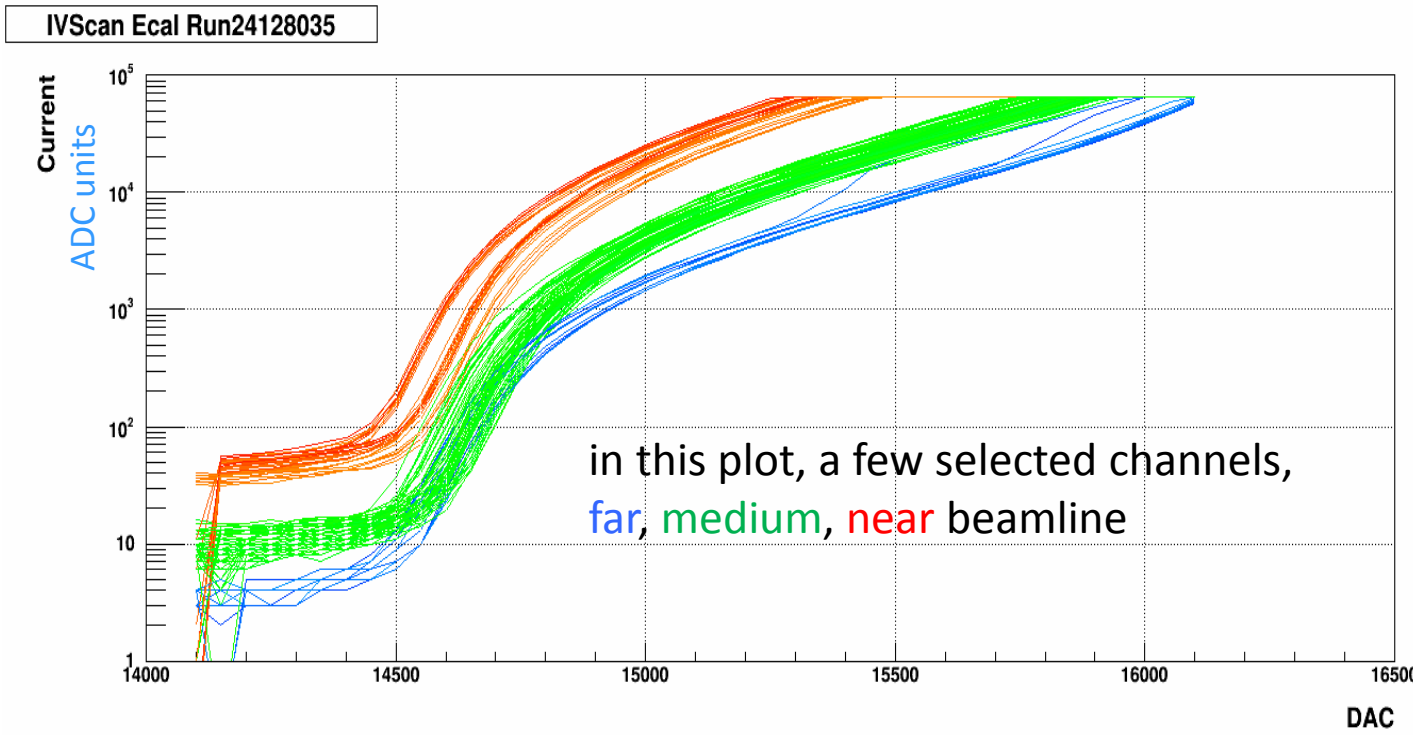
3/14/2024 ePIC DAQ/Electronics meeting

STAR FCS



(gap width is not to scale)



4× 3×3 mm^2 15 µm SiPM's in parallel per channel.

Every channel's bias can be set independently, every channel's SiPM current read independently.

Lots of information at expert's fingertips. This was important at times, for tests/commissioning and diagnosing issues. I think we say it was worth the effort.

A lesson learned:
Choose your voltage reference chips carefully! We had problems due to small shifts of reference voltage after radiation damage. Recovered by periodic bias voltage adjustments based on LED data.

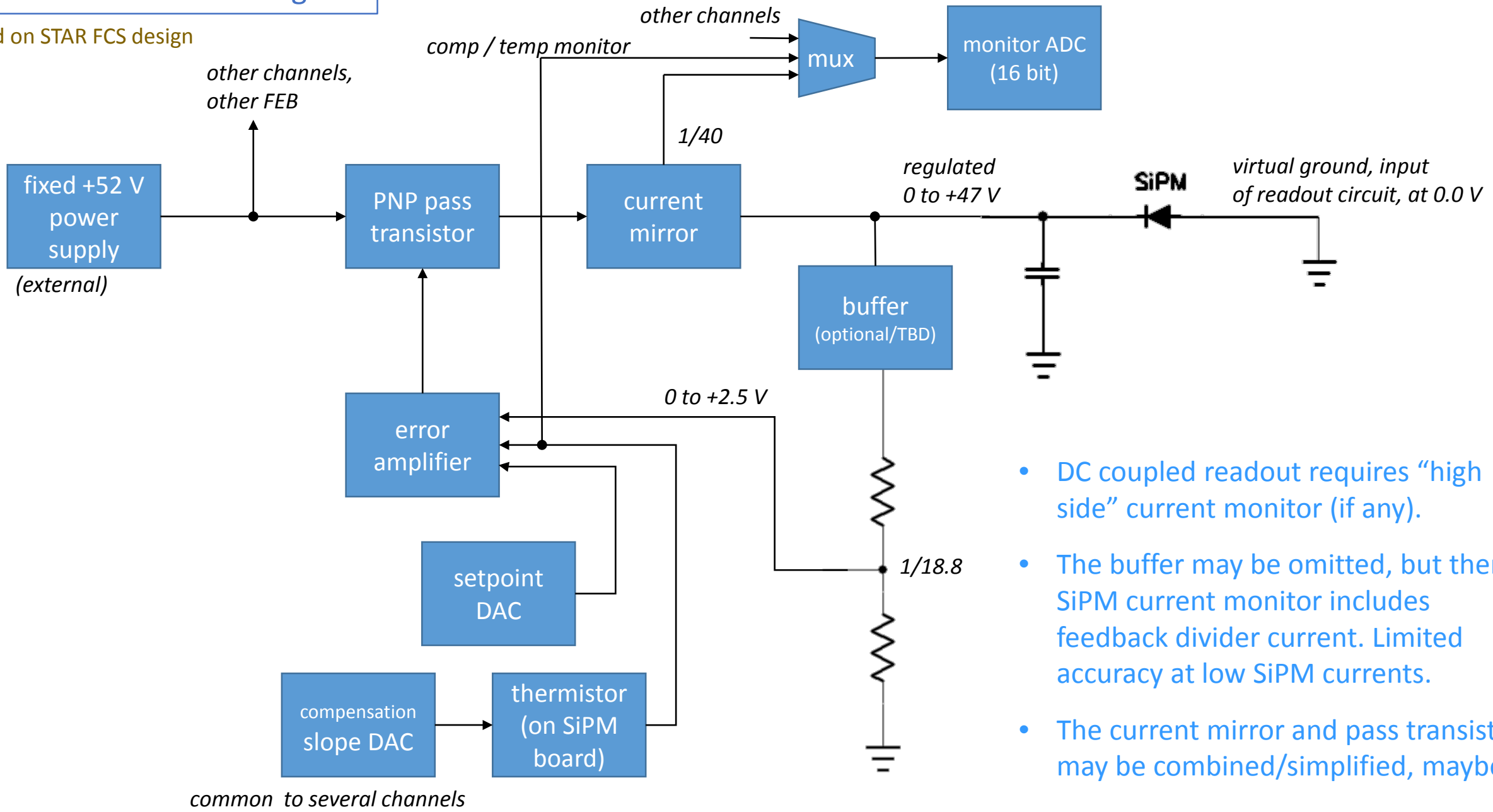
→ *might choose to feed in external V ref in fwd ECAL*

fwd ECAL bias requirements

- operating bias voltage range covering at least 25 V to 47 V
  - this is −10 V to +6 V overvoltage + V_{BR} (38 +/− 3 V spec)
    - −10 V is “standard” for no-gain tests, could be −4 V, but anyway not difficult
    - +6 V is well over recommended overvoltage (4 V), maybe we only need +4 V?
- adjustable slope temperature compensation, *with monitoring*
- overall stability of overvoltage <10 mV (1% gain stability if we used V_{OV} = 1 V), includes:
  - noise (DC to ~ shaping frequency) of bias circuits
  - temperature compensation stability
  - effect of temperature errors between SiPM’s and temperature sensor
  - output impedance of bias regulator + any series resistors added [keep it low!]
- support bias current up to 2.5 mA per tower (4× 6×6 mm^2 SiPM’s) **PERHAPS REDUCE**
- current limiting (to protect SiPM and regulator channel)
- monitor SiPM current over the supported range
  - ideally with enough resolution (~10 nA) to make useful IV curves in situ
  - certainly with enough resolution (~1 uA) to relate dark noise in readout to current
- absolute accuracy (at least initial) of bias voltage 0.5%; after bench calibration 0.05%
  - this enables setting voltages based on Hamamatsu data (which of course would also require a plan to track that data to installed SiPM boards)
- granularity of voltage setting & temperature compensation: at least, every SiPM board (4 readout channels)
- granularity of current monitoring: probably at least every SiPM board

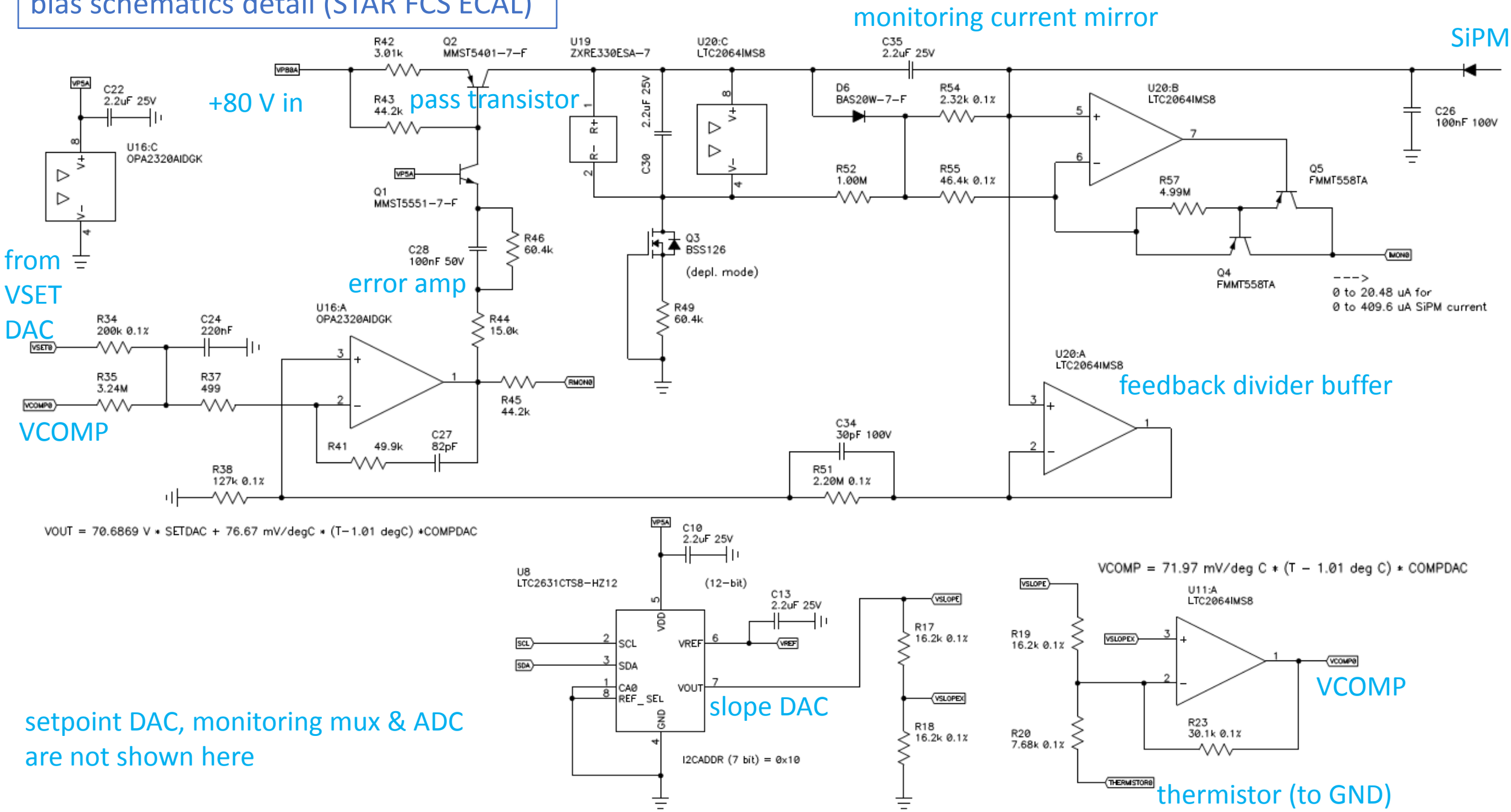
bias schematic block diagram

based on STAR FCS design



- DC coupled readout requires “high side” current monitor (if any).
- The buffer may be omitted, but then SiPM current monitor includes feedback divider current. Limited accuracy at low SiPM currents.
- The current mirror and pass transistor may be combined/simplified, maybe.

bias schematics detail (STAR FCS ECAL)



setpoint DAC, monitoring mux & ADC are not shown here

comments on other bias approaches

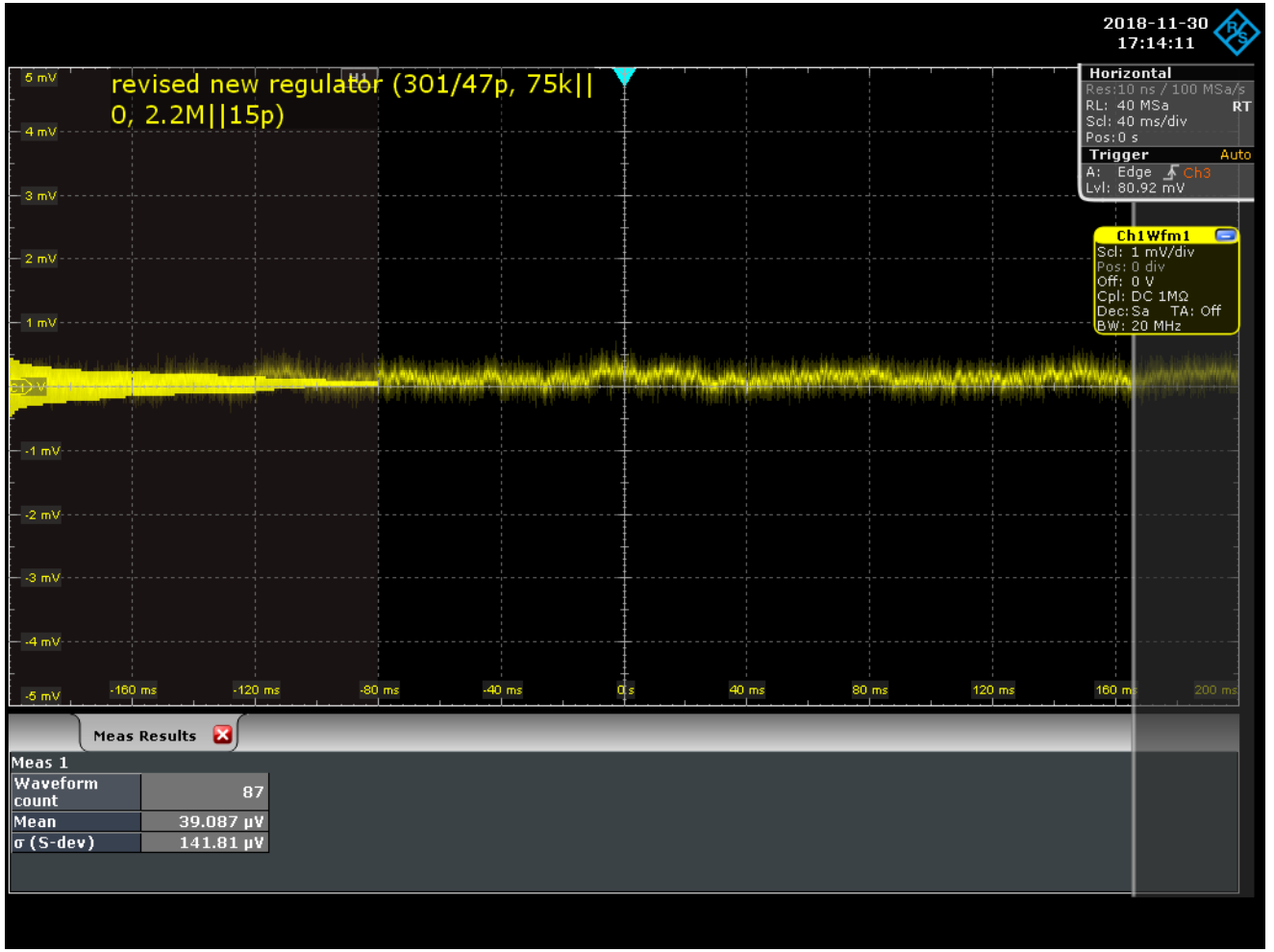
- Instead of a full 0 to 47 V regulator on each bias channel, we could use a ‘trim DAC’ with e.g. 5 V range together with a common 25 to 47 V main regulator feeding all. Why not?
  - It is sometimes useful to be able to set specific channels to voltages more than 5 V different from others. For example in mapping tests, or to deal with a failed channel.
  - Current limiting (without voltage drop) **per channel** is an essential feature and is inherent in this regulator design anyway. It would have to be added as a separate stage if we used a standard DAC IC for ‘trim DAC’ function.
- Instead of DC coupled readout, if we used AC coupled readout we could just monitor the current and/or trim the voltage there (on readout side, near 0 Volts).
  - Time-dependent rates, e.g. due to abort gap, may shift the baseline. Definitely a worry at RHIC, maybe not at EIC? Nevertheless, it is avoidable, DC coupling feasible.

STAR FCS – measured noise

142 µV (DC to ~ 30 MHz)

Meets specs, not much more to say.

Note: Depends on using a good type of feedback resistor…



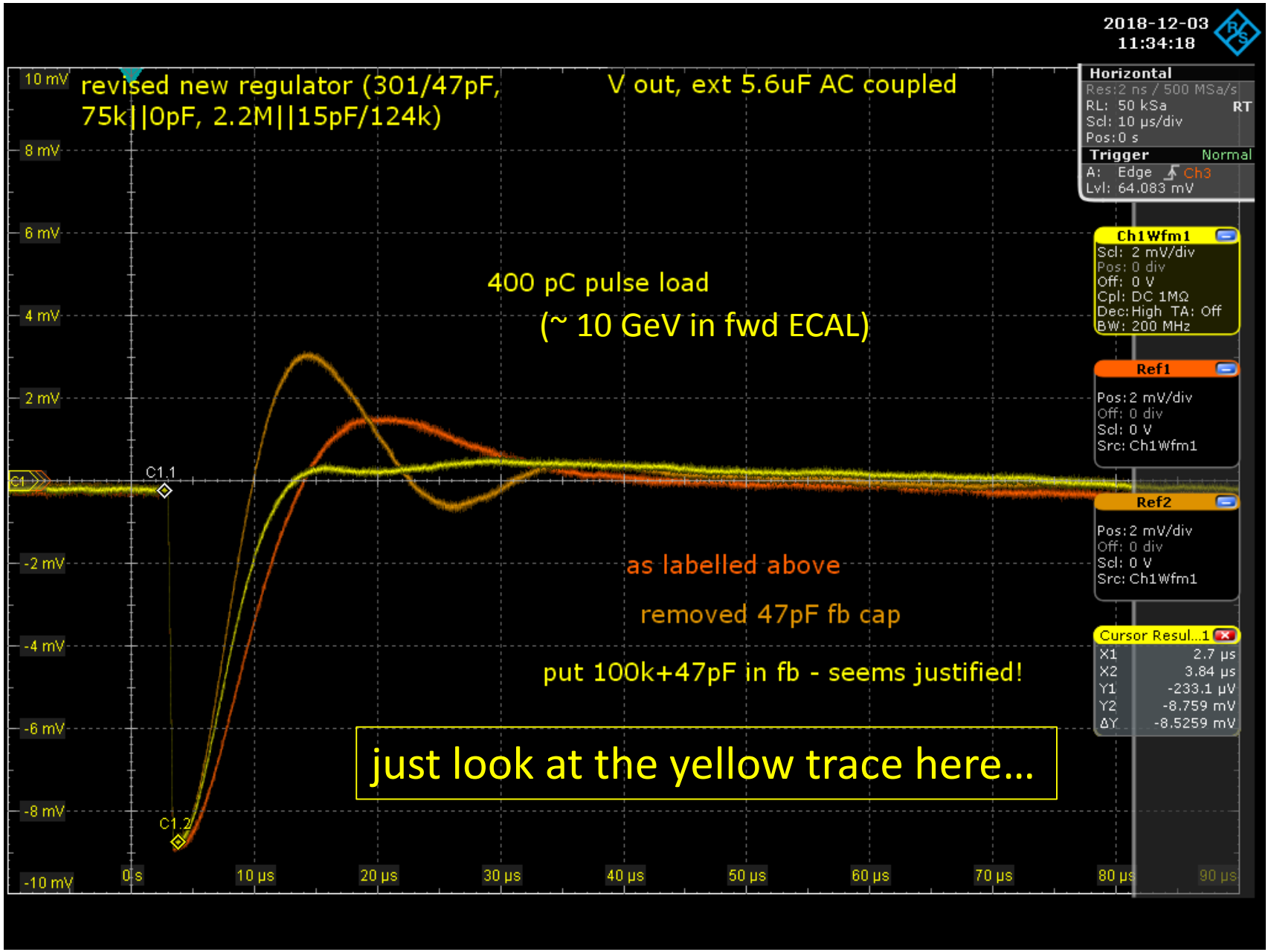
STAR FCS – transient response/recovery and output impedance

Complete recovery from large signal in about 9 µs.

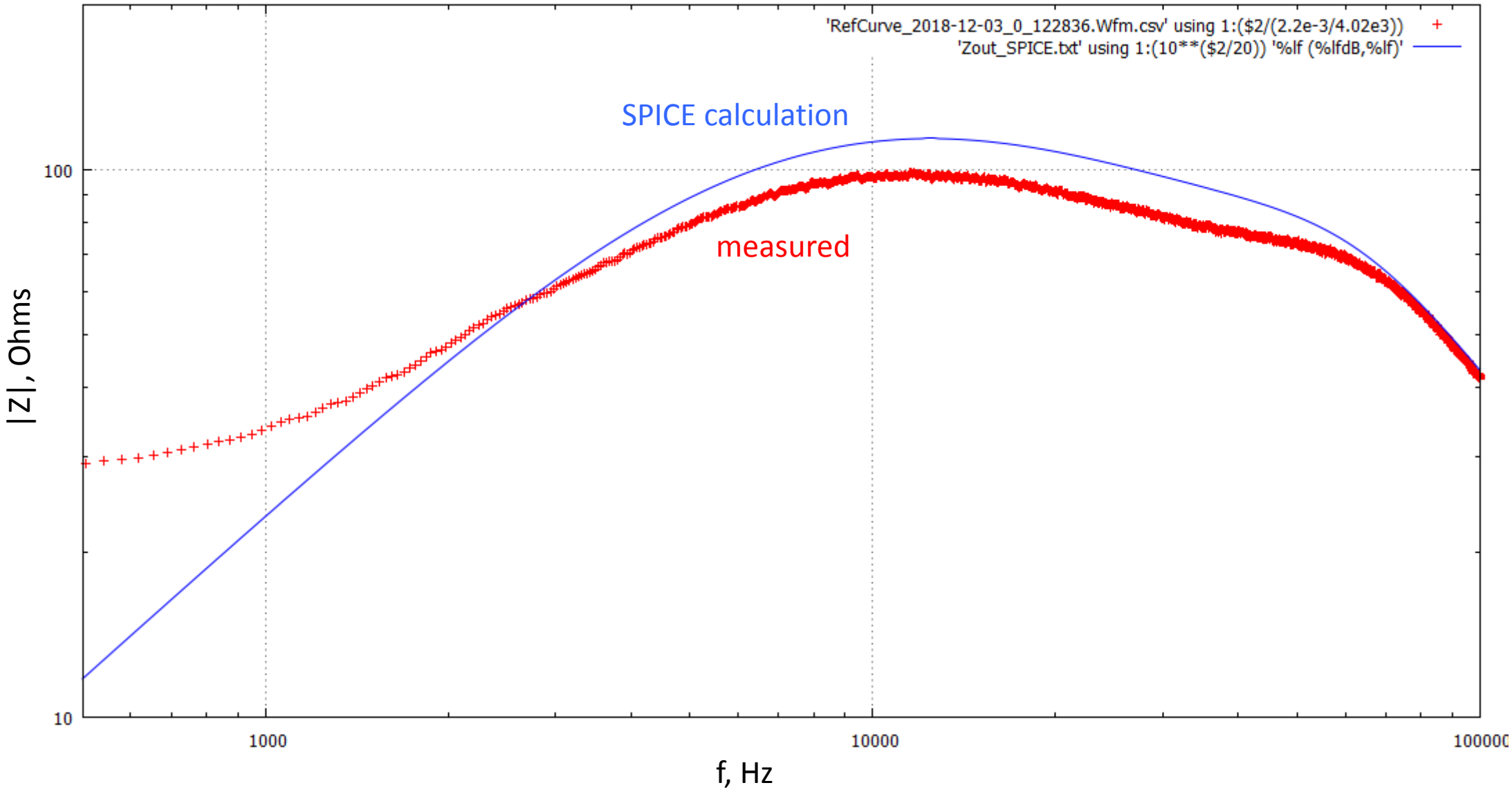
Briefly after a large signal, voltage will be out of spec by more than 10 mV though.

E.g. with 100 nF capacitance for fwd ECAL, peak deviation for full scale 100 GeV signal will be 43 mV.

But, can correct gain by history of large pulses, if necessary.



STAR FCS – transient response/recovery and output impedance



+52 V supply scheme

This is treated as just another LV supply to the FEB, same as the +15 V &c.

- Up to 9 FEB on a local LV cable on the detector, in some locations fewer
- Up to 2 local LV cables connect to external LV cable going to rack(s)
  - connection at a patchpanel mounted at outer perimeter of fwd ECAL detector
  - 16 external LV cables / PS groups per half of the detector (North/South)
  - Up to 17 FEB served by an external LV cable / PS group
  - North and South will connect to separate racks
- +52 V supply from MPOD (MPV8060I, 60 V 1 A 50 W channels)
  - *In same crate as other LV channels, to take advantage of MPOD "group" on/off/trip functions*

see backup slide for (tentative) arrangement of power groups on detector

serialization

The SiPM board will have a DS2411 “silicon serial number” chip

- readable through FEB/DAQ slow controls
- also of course read and used in production test of SiPM boards
- Hamamatsu test info for SiPM’s will be associated to board S/N

The FEB board(s) will also have an electronic serial number(s) of some kind

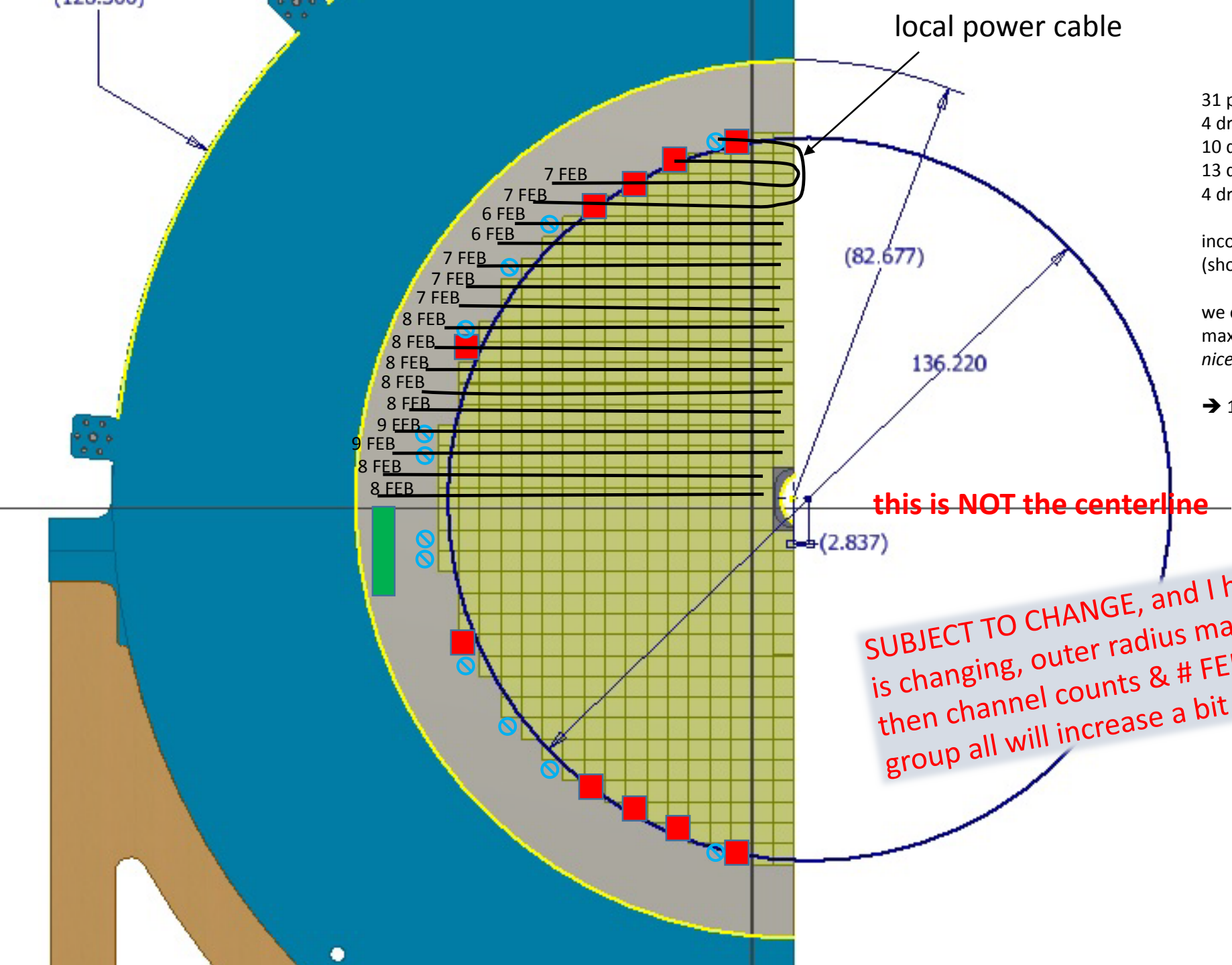
- readable through slow controls
- used in production test
- our voltage calibration of bias regulator channels will be associated to board S/N

Database to implement this stuff is TBD.
But the hardware and test plans definitely will be developed with this idea in mind.

conclusions

- We'll adopt a basically similar scheme as STAR FCS for the SiPM biasing
  - Some simplifications of the circuit details perhaps, to be explored soon, mainly for cost & size reduction
  - STAR FCS bias scheme already meets our requirements as-is
- Raw external voltage to feed the FEB bias regulator channels will be handled as any other LV supply
  - Anticipate using MPOD for this and all LV channels
  - It should be a reasonable low noise supply, but there is no requirement for precision regulation


BACKVP
177104925



31 power drops per N/S half detector
4 drops with 6 FEB
10 drops with 7 FEB
13 drops with 8 FEB
4 drops with 9 FEB

incoming power group connects to 2 power drops at patchpanel (shown as green box here)

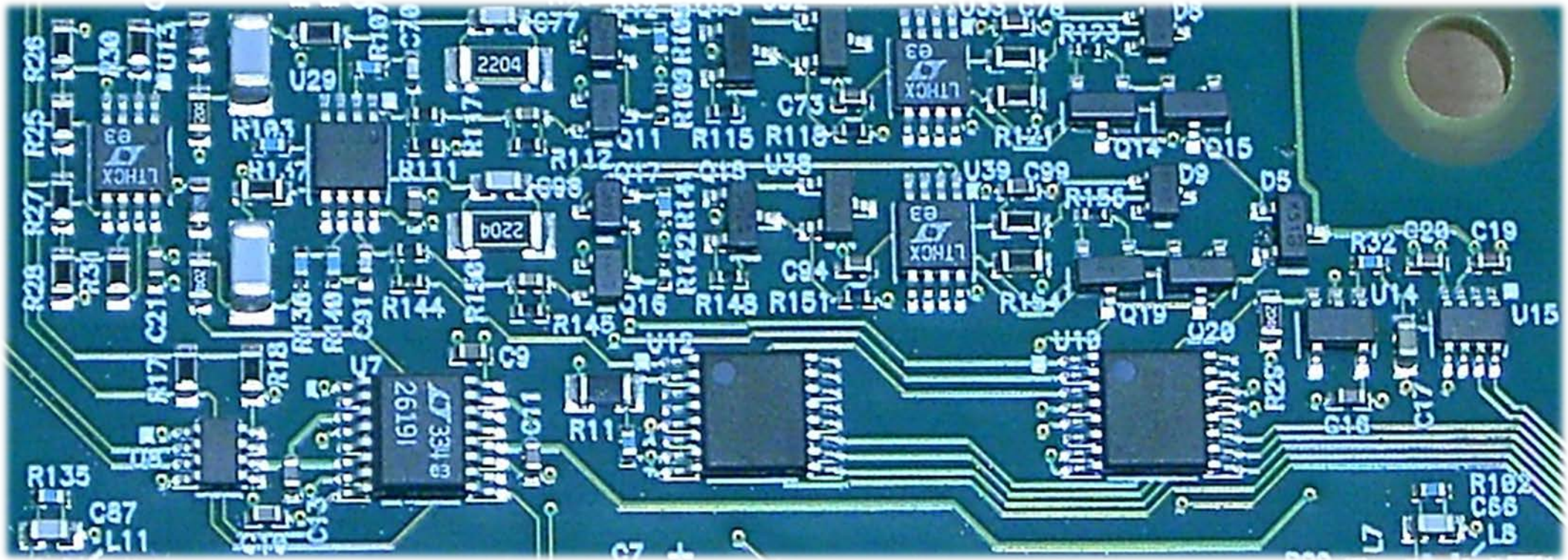
we can say (e.g.) max 17 FEB per group
max PS power (to feed ~15 VDC load) ~48 W
nice fit to 50W MPOD LV modules

➔ 16 power groups per N/S half detector

SUBJECT TO CHANGE, and I heard it probably is changing, outer radius may increase a bit, then channel counts & # FEB per power group all will increase a bit

⊘ indicates overhanging unused half-FEB

2 of 4 bias regulator / current monitor channels on STAR FCS ECAL FEB
with temperature compensation circuits, all DAC's, and monitor mux/ADC



single-sided assembly (for simplicity), could be done smaller if necessary

also, probably will simplify the circuit a little in ePIC version