dRICH SiPM bias distribution

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ePIC Electronics & DAQ WG meeting
14 March 2024

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Bias distribution

Topics of interest

- Topology of the Bias distribution
  - a diagram/schematic illustrating the approach
- Granularity of the Bias supplies
  - how many SiPMs (or groupings of) are to be fed from a single Bias supply channel?
- Bias Channel counts and need for distribution chassis
- Temperature dependencies
  - Bias compensation, measurement and compensation, etc.
- Bias supply/gain stability and noise requirements
- Configuration controls with reference to SiPM serial numbers

dRICH bias voltage distribution

bias voltage to SiPM sensors
we have two bias voltages to distribute to SiPM

dRICH numbers
6 sectors
1248 PDUs
320k SiPMs

- **HIGH VOLTAGE (Vbias)**
  - this is the normal operation mode for Physics
  - reverse bias to SiPM
  - < 55 V
  - < 1 μA / sensor
- **ANNEALING VOLTAGE (Vann)**
  - when doing annealing recovery of radiation damage
  - forward bias to SiPM
  - < 12 V
  - < 150 mA / sensor

Vbias distribution

1 main - 4 PDU

32 channels
100 V
10 mA

for full dRICH
320 channels
10x modules
< 1 main frame

dRICH sector
readout box patch panel

52x

Vbias distribution

1 main - 1 PDU

32 channels
100 V
10 mA

for full dRICH
1248 channels
39x modules
< 3 main frames

dRICH sector
readout box patch panel

208x

Vbias distribution

1 main - 208 ML3 - 1 PDU

60 V
1 A

communication

dRICH sector
readout box patch panel

60 V
3.3 mA

custom linear regulator
MasterLogic v3 (1 channel)

PDU

MICROCHIP
ATMEGA1609

microcontroller
or similar

208x

dRICH has 6 sectors
208 photodetector units (PDU) / sector
256 SiPM channels / PDU

Vbias distribution with

- one main primary channel for each sector (6 main Vbias channels for whole dRICH)
- that feeds 208 channels of custom linear regulators (one channel for each PDU)

Total of 1248 Vbias derived channels
Granularity of 1 PDU (256 sensors)

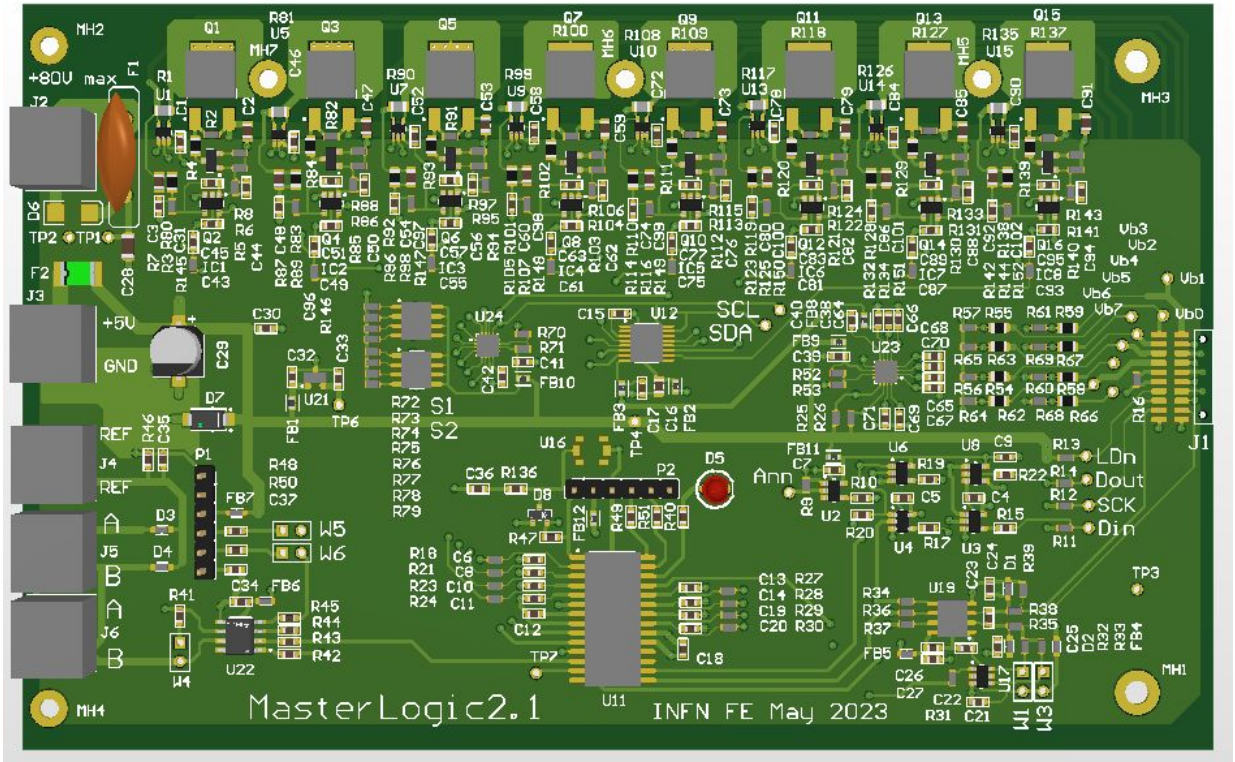
The Masterlogic v2

we developed and operated in the dRICH beam test in October 2023 the MasterLogic v2 card (evolution of the MasterLogic v1 card).

the card hosts

- 8 channels made of identical circuits for linear regulation of Vbias from 0 to Vin (80 V max)
- a microcontroller (PIC) for external communication (RS485)
- voltage & current monitor

the MasterLogic v2 card hosts more features that are needed for beam test operations. Some of them will be delegated to the RDO, other might be included or dropped.



The Masterlogic v3 and the patch panel

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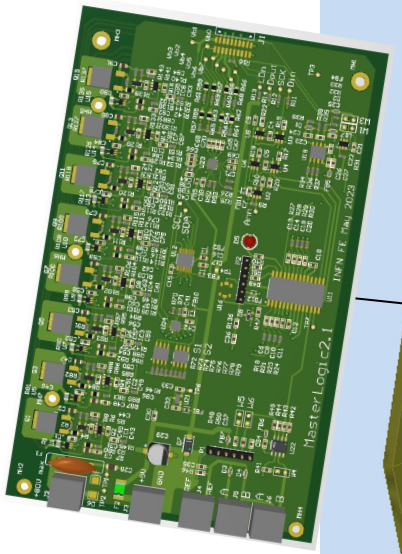
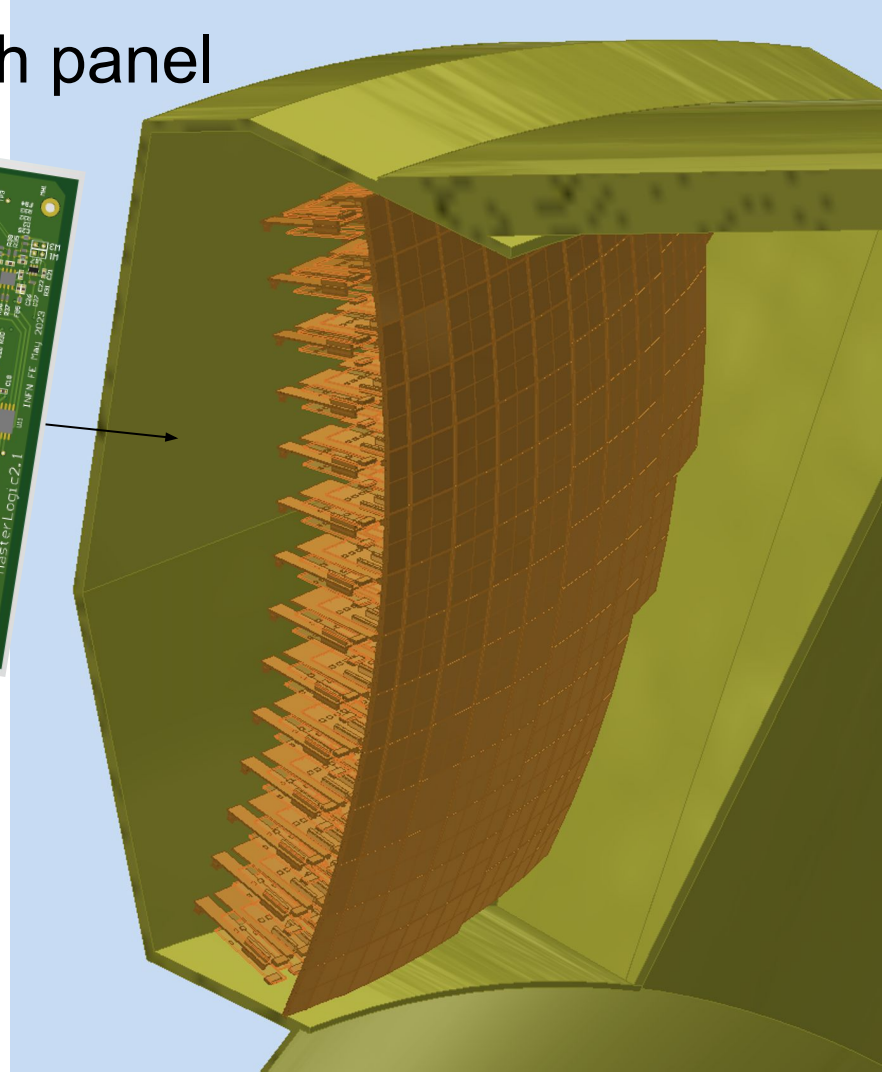
- a microcontroller (PIC) for external communication (RS485)
- current monitor?
- something else?

the MasterLogic v2 card hosts more features that are needed for beam test operations. Some of them will be delegated to the RDO, other might be included or dropped.

a future evolution might be a MasterLogic v3 card to plug onto the dRICH readout box patch panel for Vbias and Vann control and distribution (and perhaps more features).





Vbias distribution

summary table

commercial

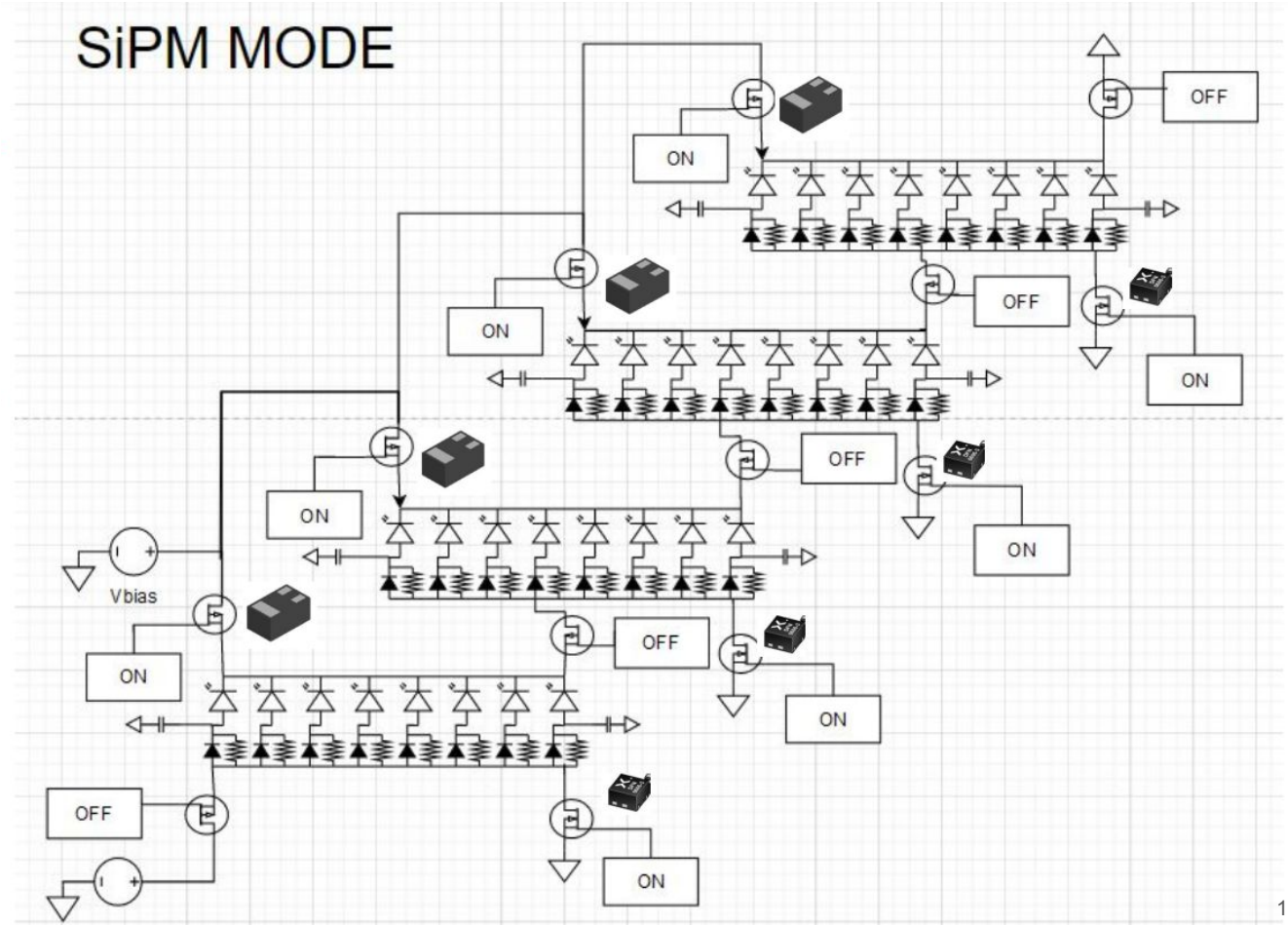
custom

this is cheaper than that

this is likely cheaper, but more complex

	1 main 1 PDU	1 main 4 PDU	1 main 52 ML3 4 PDU	1 main 208 ML3 4 PDU
$N_{primary}$	1248	312	6	6
$N_{primary}$ / sector	208	52	1	1
$V_{primary}$ (V)	60	60	60	60
$I_{primary}$ (A)	< 1 mA	< 1 mA	250 mA	1 A
Granularity	256	1024	1024	256
uControl	no	no	yes	yes

Vbias distribution



the circuit foreseen to allow both normal operation of SiPM (reverse bias) and self-annealing (forward bias) allows to inhibit the Vbias to a granularity of 8 SiPM.

might come at handy in case of troubles with Vbias distribution in a specific SiPM → inhibit Vbias in a string of 8 SiPM sensors while the rest of the PDU can still be operated

digital switches (MOSFET) controlled by RDO

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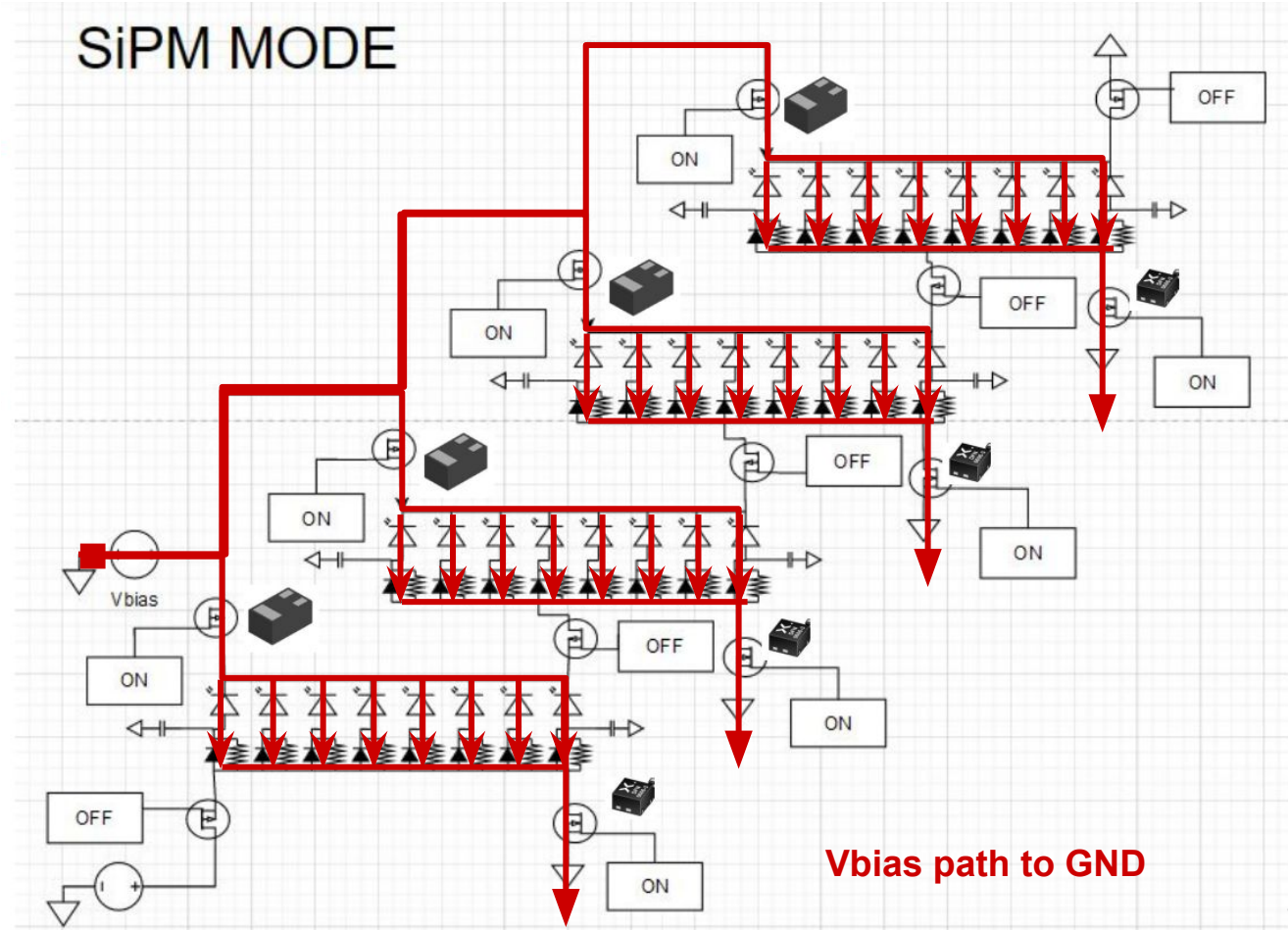

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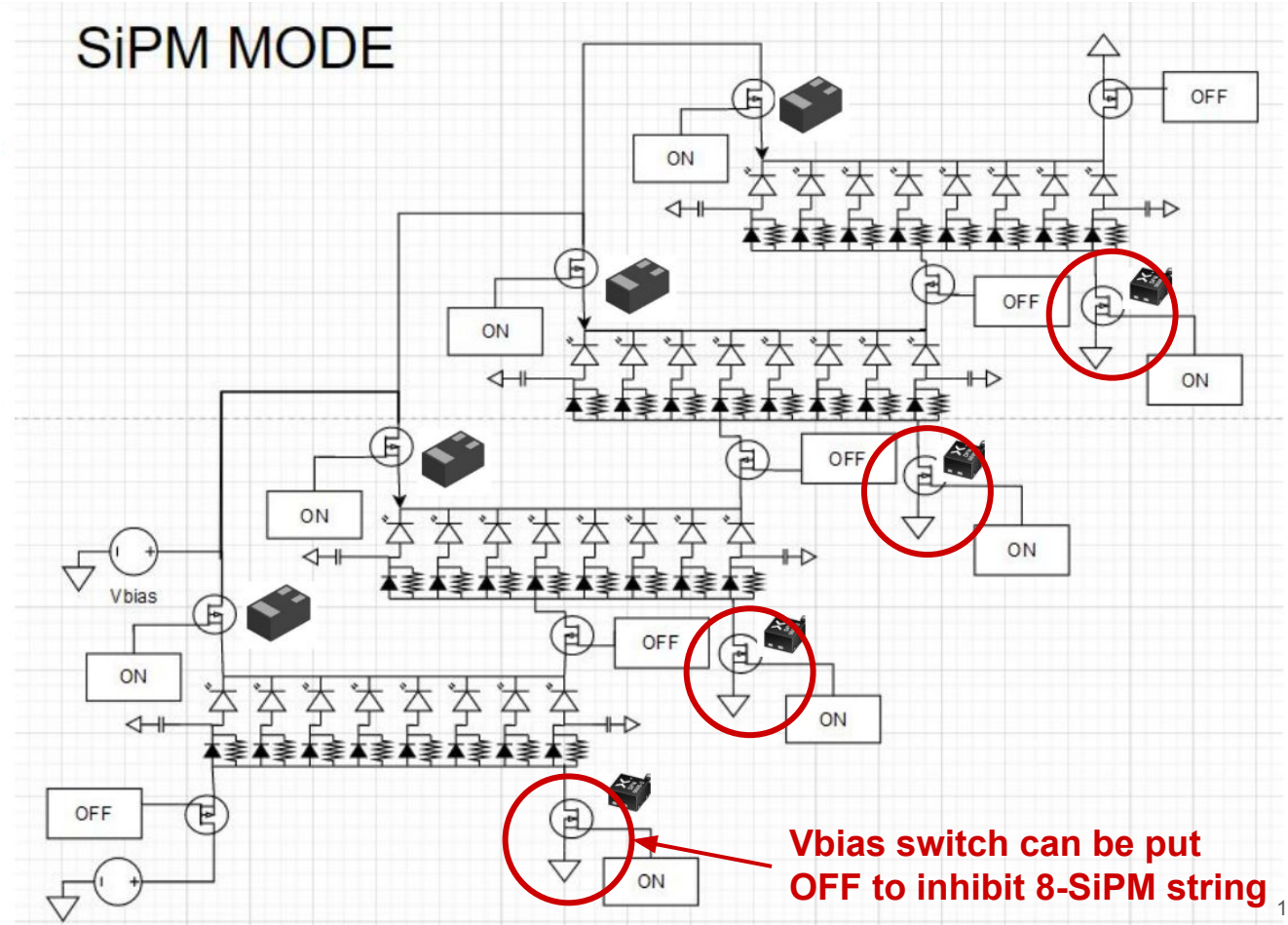

Vann distribution

1 main - 16 drivers - 1 PDU

48 V
8 A

dRICH sector
readout box patch panel

8x channel annealing driver

PDU

microcontroller
or similar

16x

13x

13x

Vann distribution with

- 13 main primary channels for each sector (total 6 sectors)
- each channel feeds 16 octal channel drivers to select which portions of the 16 PDUs will undergo annealing
- typically one full PDU at a time

advantage: less channels
disadvantage: less control / monitor

Vann distribution

8 main - 16 drivers - 1 PDU

8x ch
48 V
1 A

dRICH sector
readout box patch panel

8x channel
annealing driver

IPS8160HQ-1

IPS8160HQ-1

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IPS8160HQ-1

PDU

PDU

16x

MICROCHIP
ATMEGA1609

13x

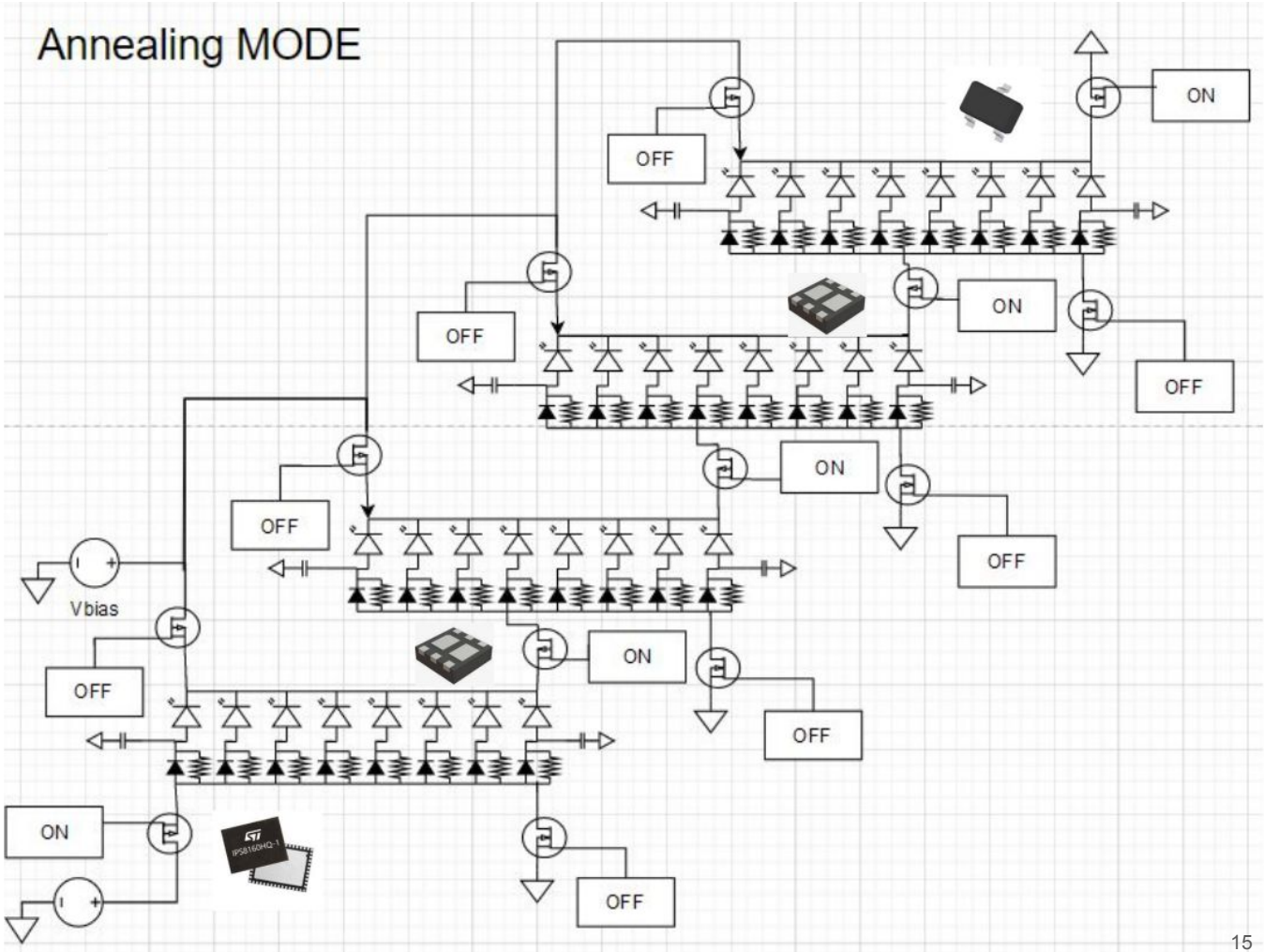
13x

Vann distribution with

- 104 main primary channels for each sector (total 6 sectors)
- each channel feeds the 8 inputs of 16 octal channel drivers to select which portions of the 16 PDUs will undergo annealing
- typically one full PDU at a time

advantage: more control / monitor
disadvantage: more channels

Vann distribution



forward-bias annealing current for each sensor can reach up to 100 mA
to keep annealing current low we foresee to forward-bias the SiPM in series of 4 SiPM strings

note: this approach should work but has to be tested to prove its performance

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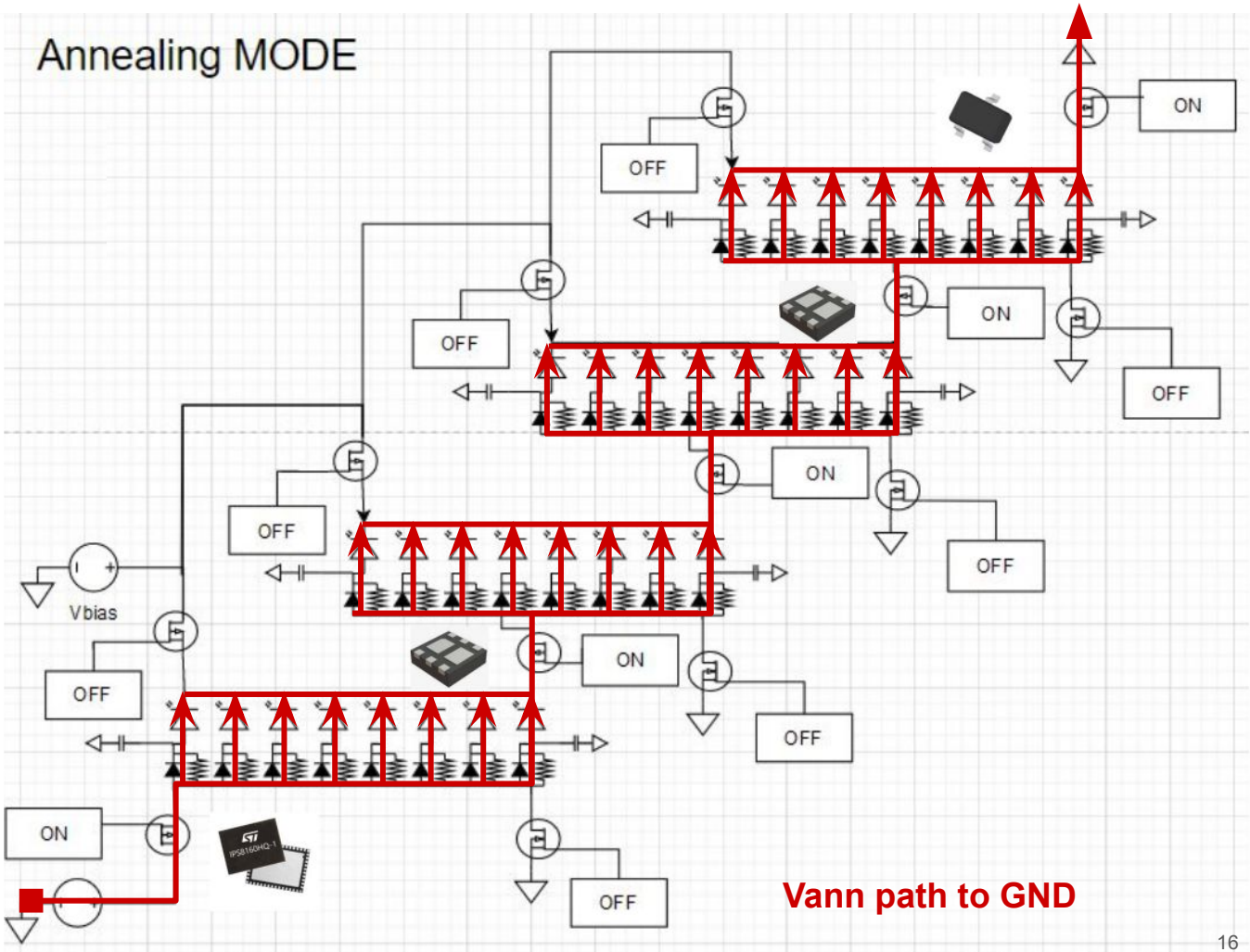


Summary

two potentially good approaches (both for Vbias and Vann)
typically one approach has less primary channels with higher power / current
the other approach has more primary channels and lower power / current

	Vbias (option A)	Vbias (option B)	Vann (option A)	Vann (option B)
$N_{primary}$	6	312	78	624
$N_{primary}$ / sector	1	52	13	104
$V_{primary}$	60 V	60 V	48 V	48 V
$I_{primary}$	1 A	1 mA	8 A	1 A
analog grouping voltage regulation	256	1024	4096	32
digital grouping capability to turn OFF	8	8	32	32
T dependence	yes measured and regulated	yes measured and regulated	no	no
stability	< 20 mV	< 20 mV	< 100 mA	< 100 mA
noise ripple	< 3 mVpp	< 3 mVpp	< 100 mVpp	< 100 mVpp

PDU voltage services

the **SiPM grouping** is composed of 4 strings of 8 SiPM each

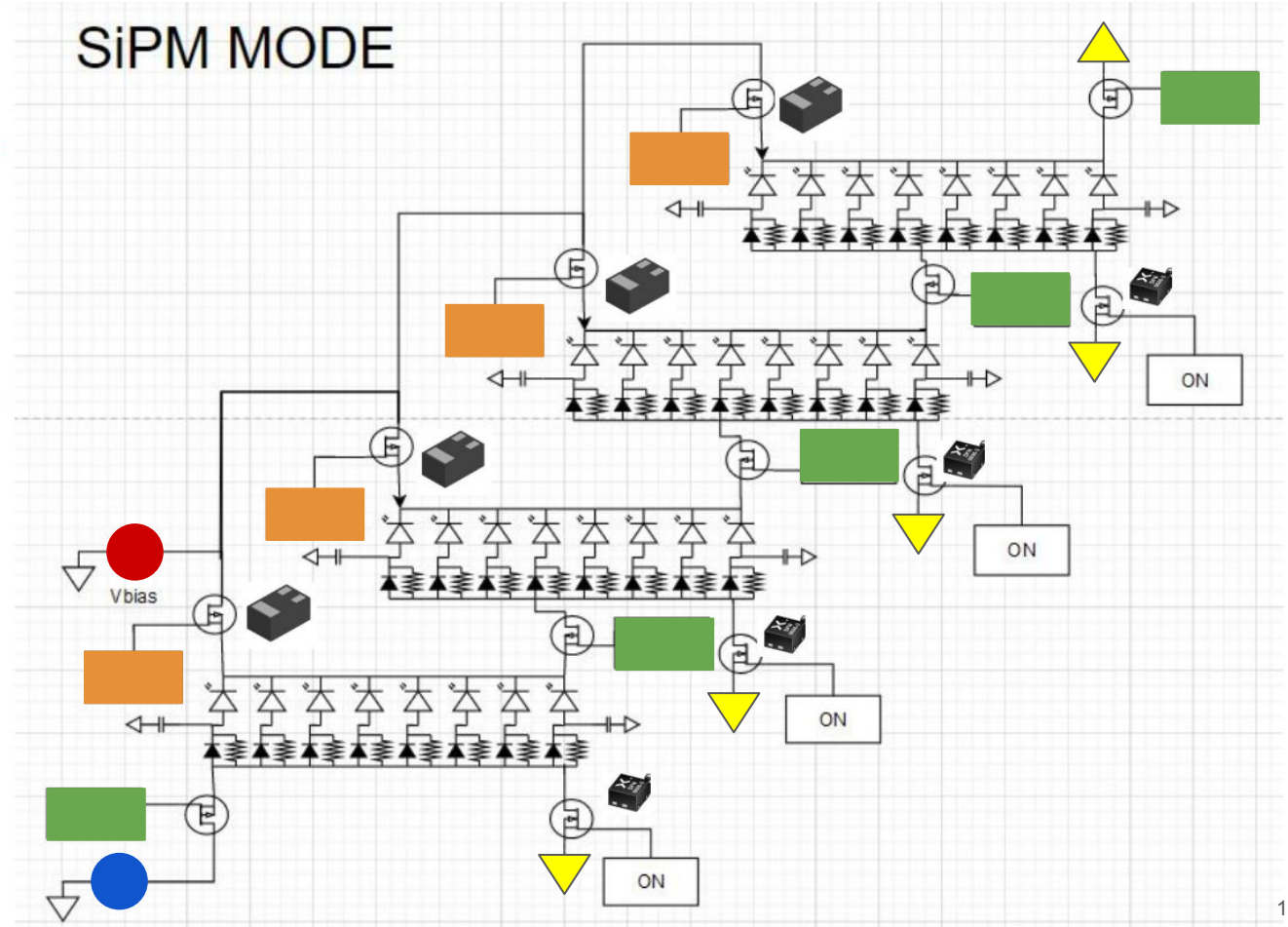
one **SiPM matrix** is composed of two SiPM groupings

the **dRICH PDU** is composed of four SiPM matrices

for each SiPM grouping we foresee the following external services (via RDO)

- **1 V-bias**
- **1 CTRL-bias**
- **1 V-ann**
- **1 CTRL-ann**
- **1 GND**

This is a total of 5 wires for each SiPM grouping, namely a total of **40 wires for one PDU**. The 40 wires enter on the RDO from the readout box patch-panel.



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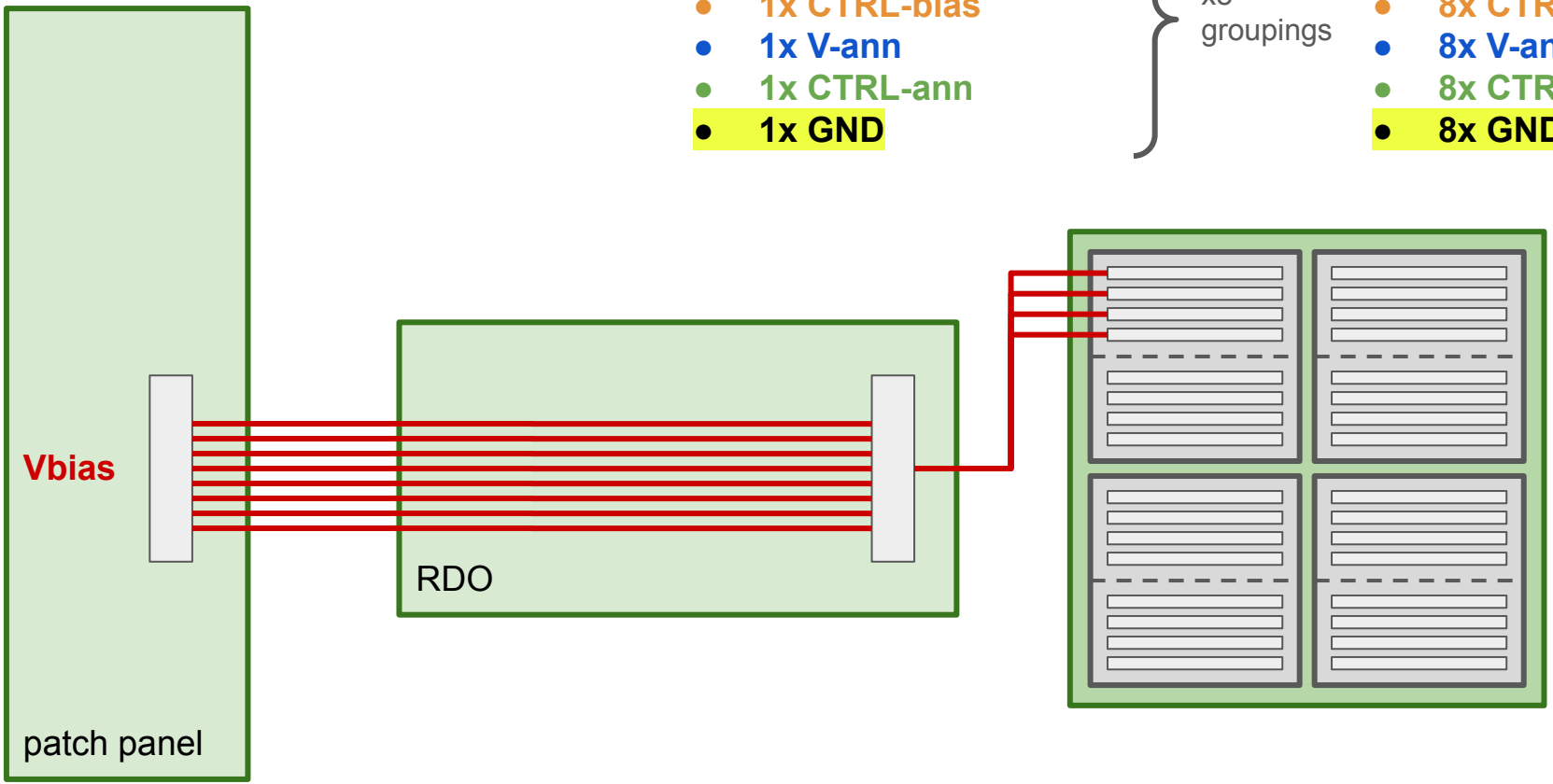
- **1x GND**

x8 groupings

for each PDU we foreseel services (via RDO)

- **8x V-bias**
- **8x CTRL-bias**
- **8x V-ann**
- **8x CTRL-ann**
- **8x GND**



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