ePIC SVT BNL efforts

- now and in the future

March 14, 2024

Contribution:

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ePIC SVT efforts -1

- **Baseline (resulting from LDRD22-078, eRD113 R&D and PED)**

Sensors (ITS3 and EIC-LAS):

- design of data transmission links from RepeatedSensorUnit (RSU) to LeftEndCap for congregation on HighSpeed,
- on-MAPS data sparsification and congregation for reduction of HighSpeed links (ITS3 database needed),
- additional functionalities such as VitalFunctionsMonitoring_ADC, hopefully to be included in ER2.

Ancillary ASIC (AncASIC):

- Implications of adoption of serial powering on ePIC-SVT (some early ideas may not be greatest):
  - negative voltage generation (NVG) for biasing of charge collection volume of MAPS,
  - Slow control and operational command distribution to EIC-LAS,
  - conceptualization of shunt-regulator-based power supply for improved ratio $P_{MAPS}/P_{AncASIC}$.

Testing and assembly:

- Test, assembly, and calibration laboratory for the ePIC components arriving at BNL before installation in the EIC.

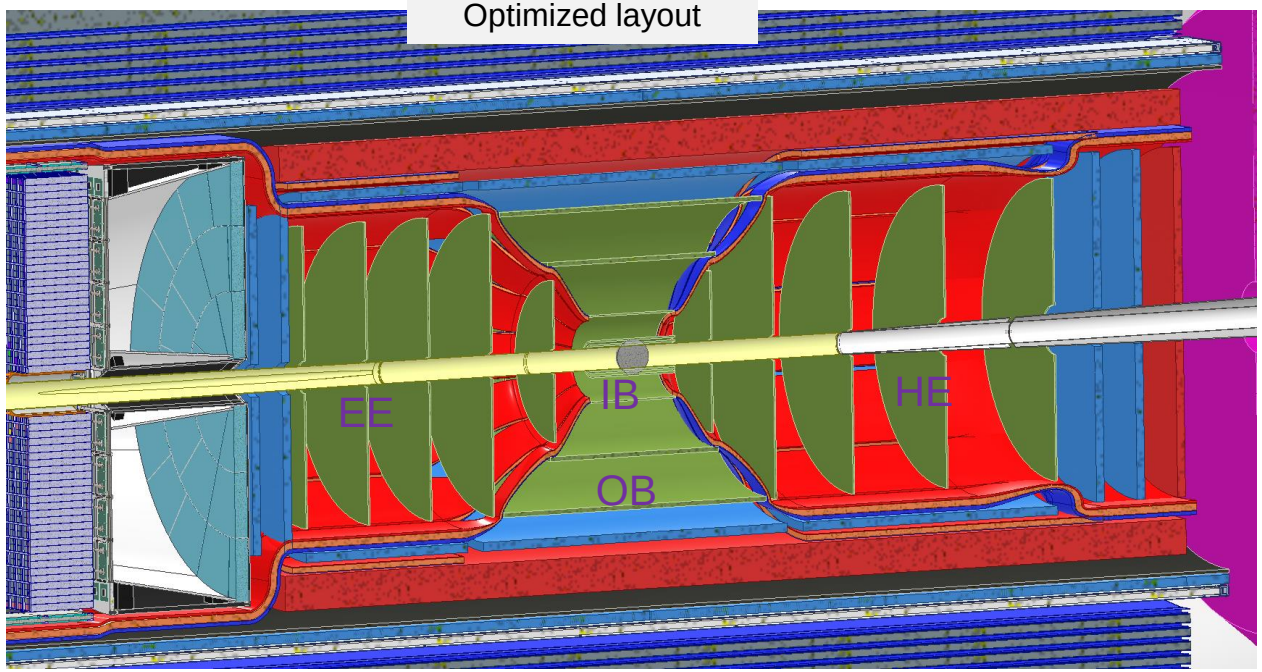
ePIC SVT efforts -2

- **Upgrades (based on EIC gen. R&D, LDRD24-054)**

  - RepeatedSensorUnit (RSU) with Event-Driven, binary (no priority encoding) readout and LowPower (LP) Front-End for O(100 ns) timing resolution;
  - Power-over-Fiber (PoF) for simplified, direct and low material load supply (power delivered by light and converted to electrical with PV cells);
  - Integrated photonics for, small number of components (no laser in fiducial volume) and ultra-large bandwidth data transmission with WavelengthDivisionModulation (WDM);
  - Self-supporting, larger-radius (OB) layers with pre-bent, large-area MAPS sensors for X_0 reduction.

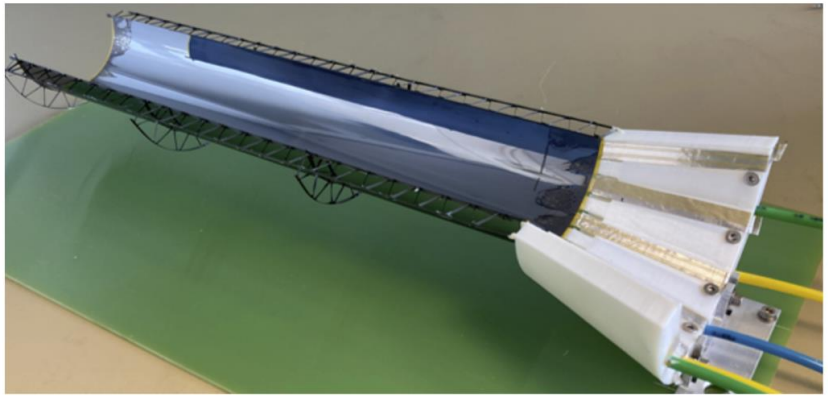
Glance of ePIC SVT -1

Optimized layout



- cables & services for μvertex & OuterBarrel layers + first 2 disks exite on a cone along 45° line and cables run in-front of MM
- 3 equal sized MM modules
- MM cables can run on front or back face of MM
- fewer sharp bends

MAPS Barrel + Disks
MPGD Barrels + Disks
AC-LGAD based ToF



ePIC SVT detector layout configuration
(in total almost 100B pixels, on ~ 10 m^2 of Si)

Silicon Barrel Layers			
	Radius [mm] (min, max)	Length [mm]	X/X0 [%]
VX 1 (L0)	36	270	0.05
VX2 (L1) IB	48	270	0.05
VX3 (L2)	120	270	0.05
Sagitta1 (L3)	270	540	0.25
Sagitta2 (L4) OB	420	840	0.55
Silicon Hadron Endcap (wheels)			
	Distance [cm]	Radius [mm] (min, max)	X/X0 [%]
HD1	25	(36.76, 230)	0.24
HD2 H-End	45	(36.76, 430)	0.24
HD3 Cap	70	(38.42, 430)	0.24
HD4 Disks	100	(54.43, 430)	0.24
HD5	135	(70.14, 430)	0.24
Silicon Electron Endcap (wheels)			
ED1	-25	(36.76, 230)	0.24
ED2 E-End	-45	(36.76, 430)	0.24
ED3 Cap	-65	(36.76, 430)	0.24
ED4 Disks	-90	(40.0614, 430)	0.24
ED5	-115	(46.3529, 430)	0.24

Technology of choice: MAPS in TPSCo 65 nm process, following CERN's ALICE ITS3 upgrade development of bent silicon

Disclaimer: some numbers, mainly X/X0, are evolving due to stave approach and cooling.

G. Feofilov et al.,
ITS3 WP4 10 October 2023.

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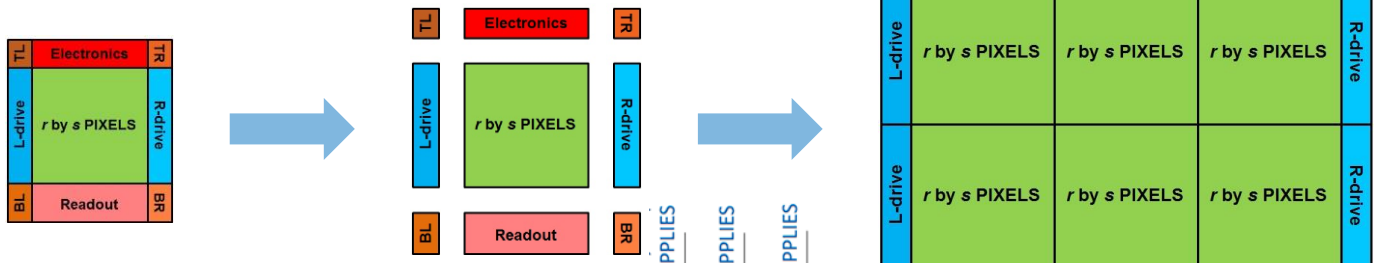
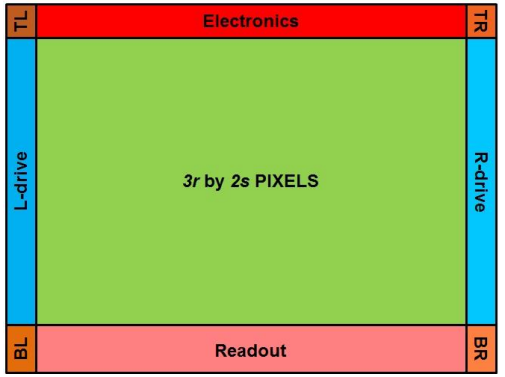
Glance of ePIC SVT -2

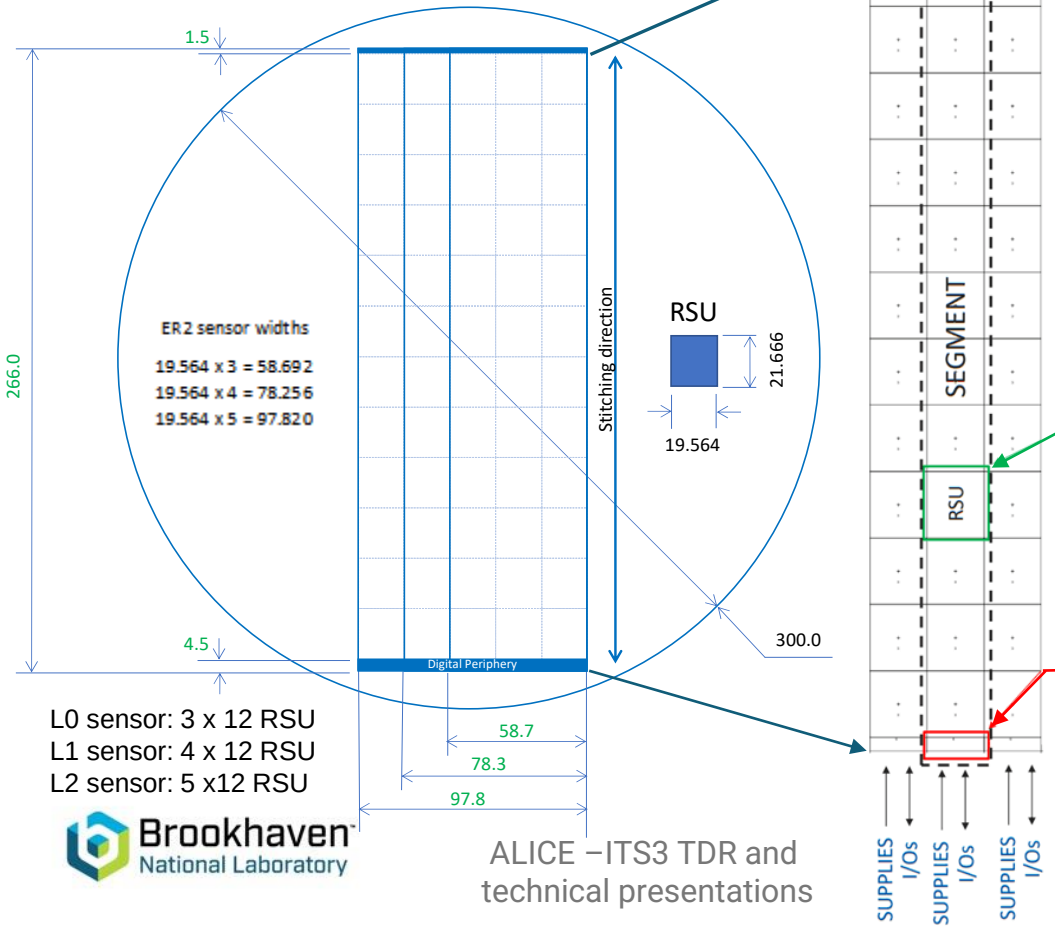
MAPS sensors are large (single ASIC) …

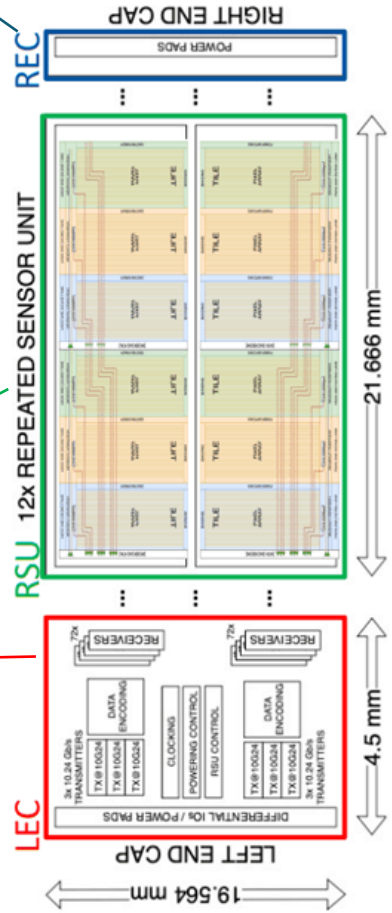




by Iain Sedgwick

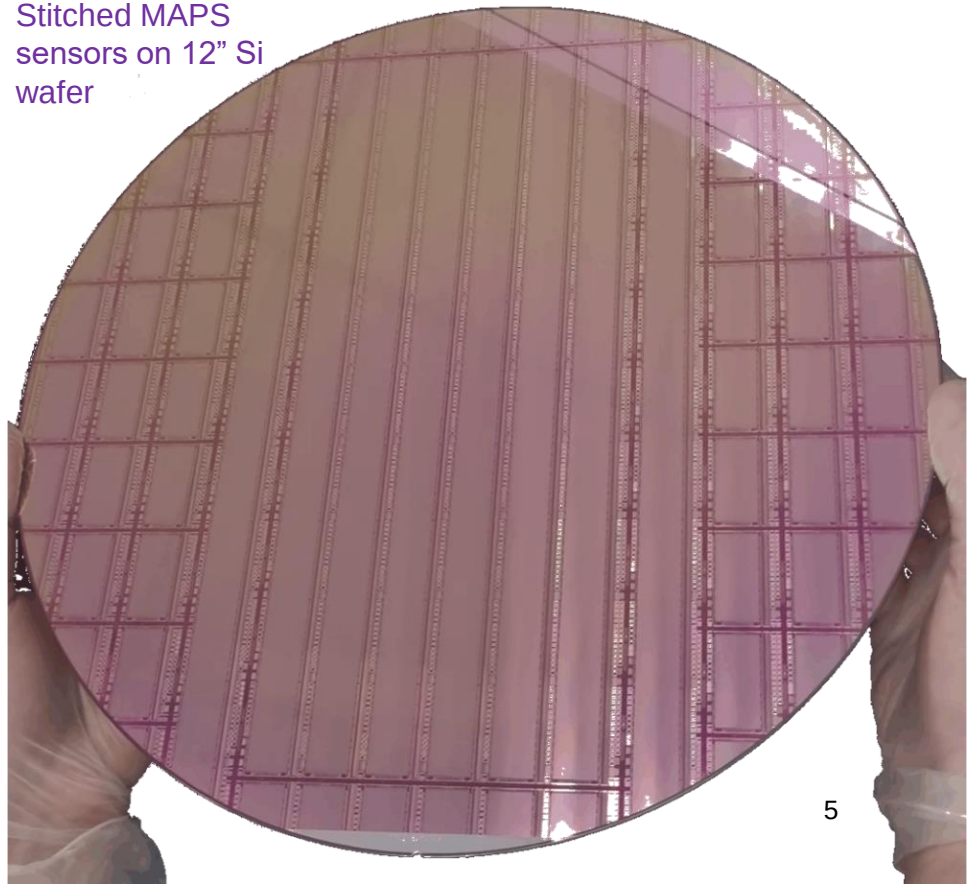
…thanks to reticle stitching





L0 sensor: 3 x 12 RSU
L1 sensor: 4 x 12 RSU
L2 sensor: 5 x12 RSU

Stitched MAPS sensors on 12” Si wafer



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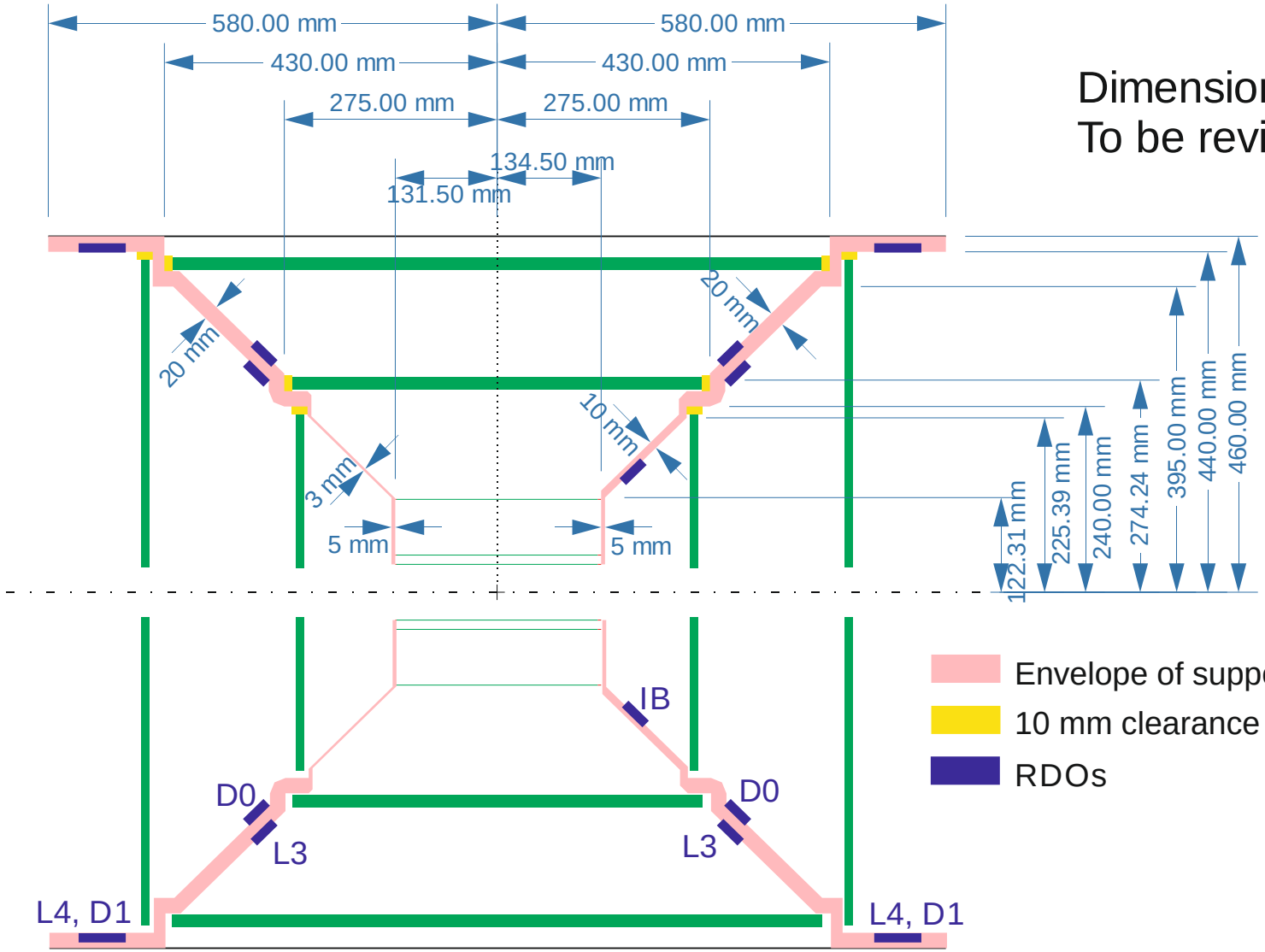
ALICE –ITS3 TDR and technical presentations

Glance of ePIC SVT



Dimensions indicative only!
To be revised after proper design

Envelope of support cones and services (electrical, optical and air)

10 mm clearance at end of local supports

RDOs

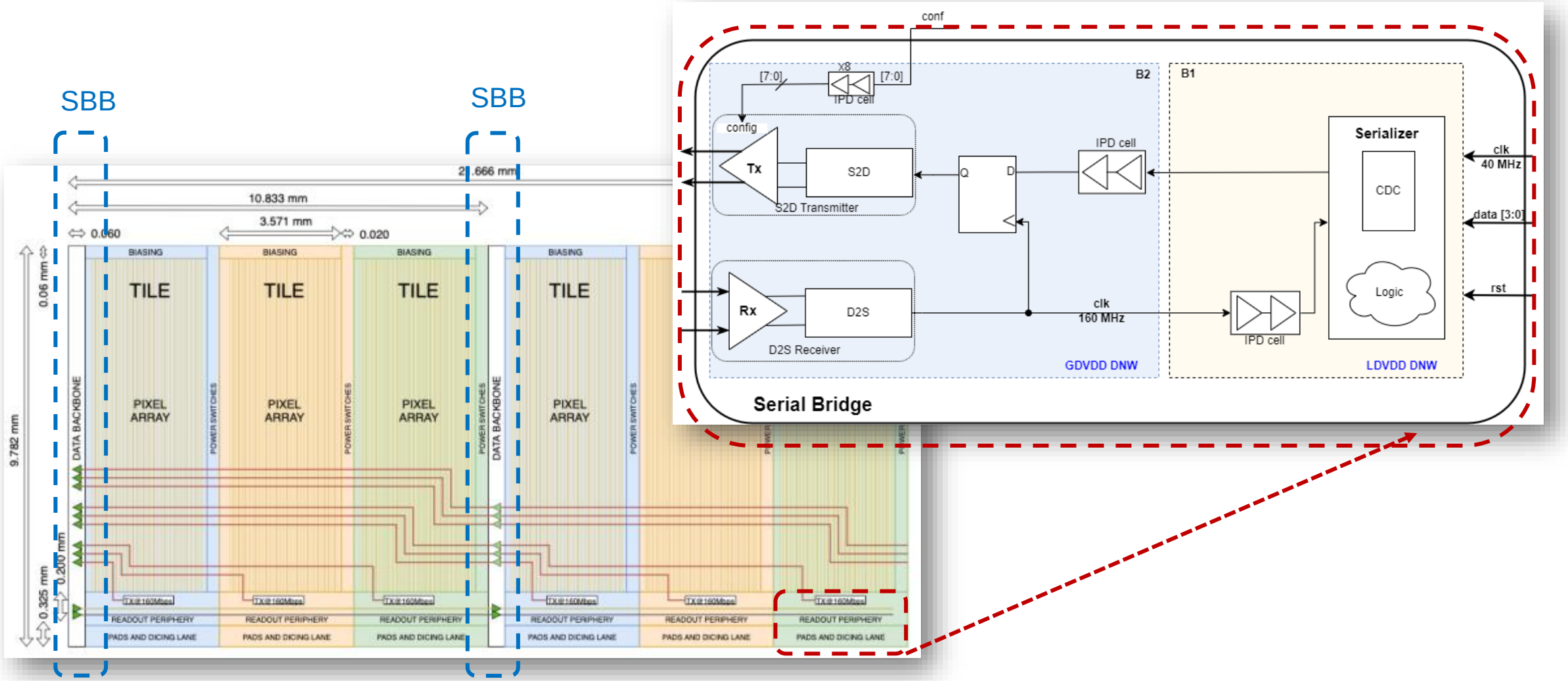
Brookhaven National Laboratory

by Georg Viehhauser

MOSAIX

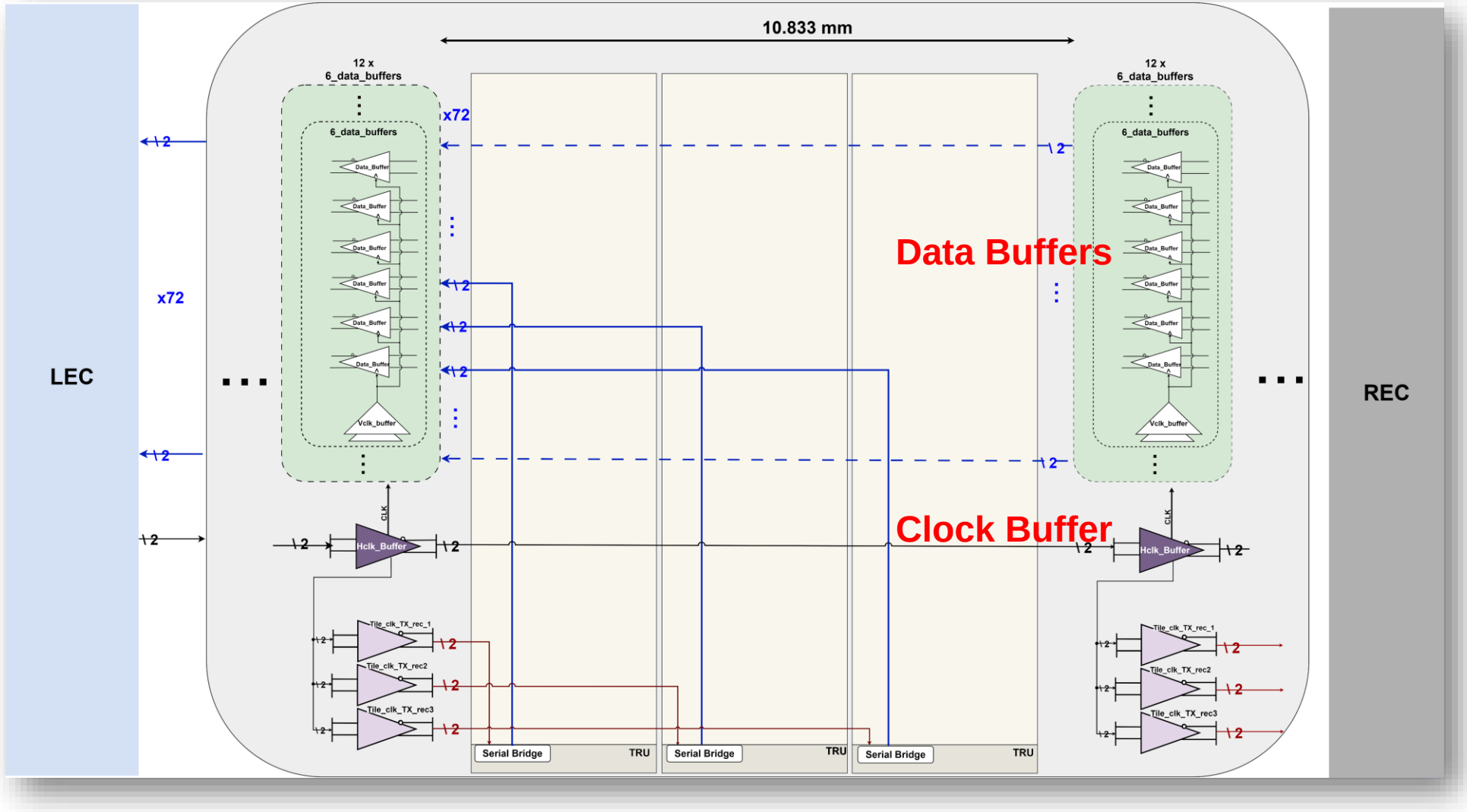
12-Reticle-long MAPS stitched sensors in TPSCo 65 nm process

Transmission Links from RSUs -1

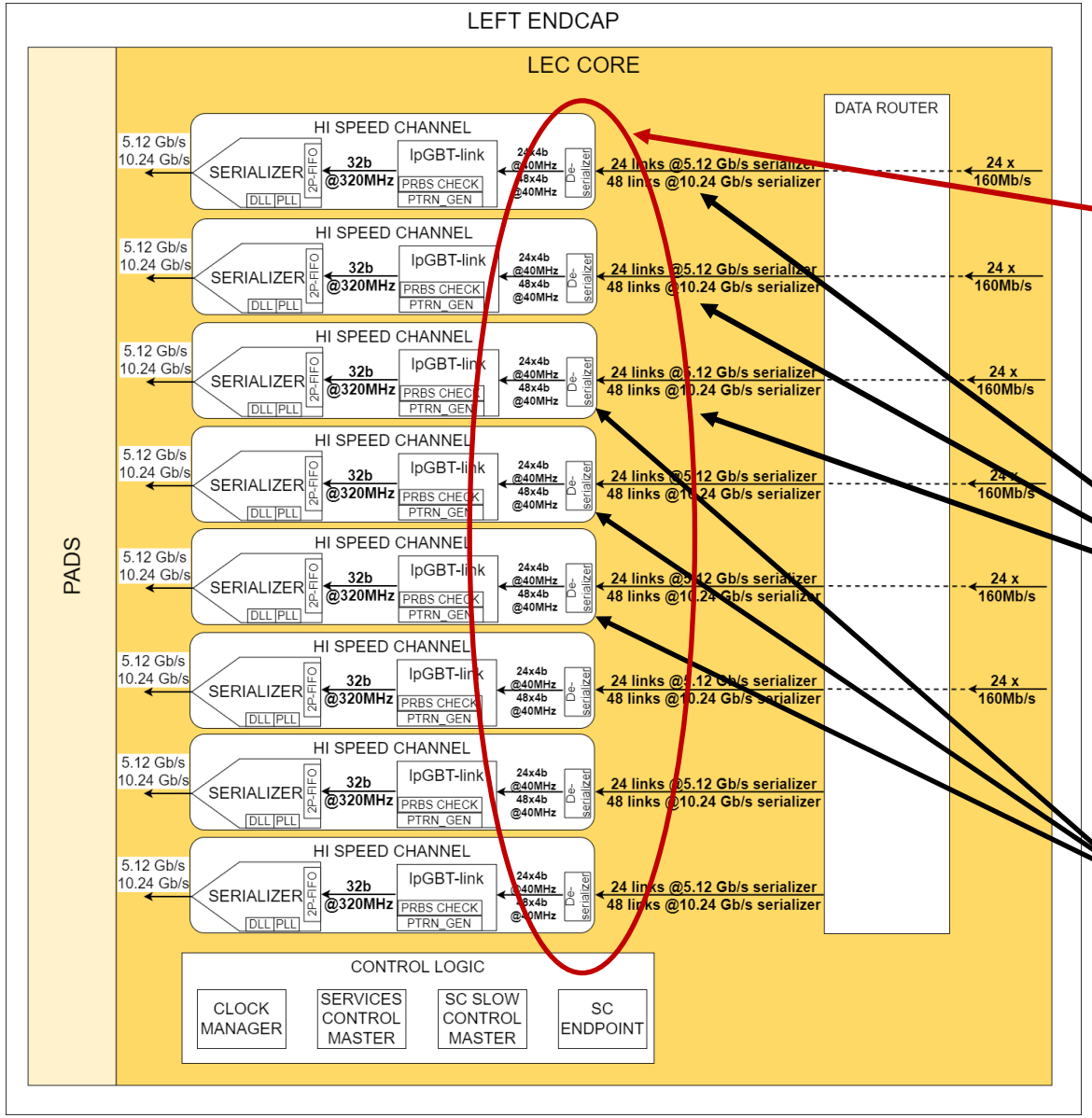


Stitched Backbone

Transmission Links from RSUs -2



Transmission Links from RSUs -3

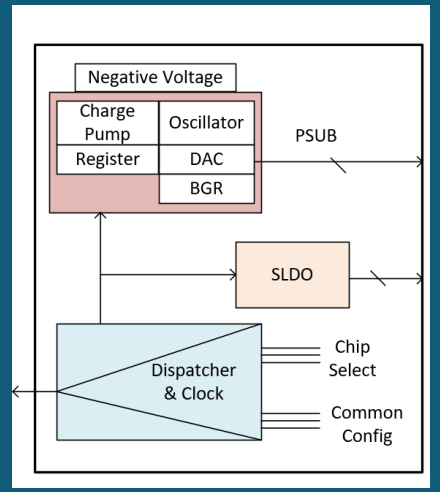


All these links convey effectively "zeros" – therefore we consider addition of "data interpreter" for sparsification and sending data off EIC-LAS on smaller number of links in OB

tile serial streams
@ 160/80 Mbps

de-serializers

Ancillary ASIC



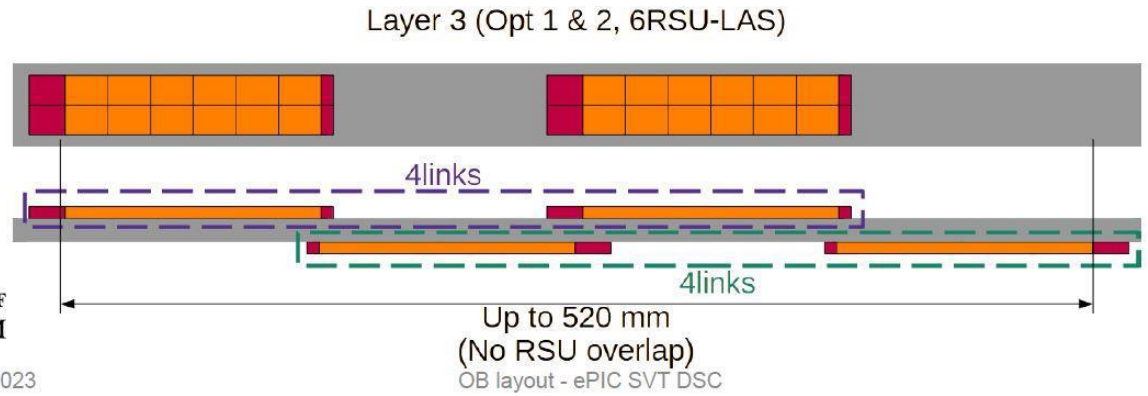
3 functions:

- Intermediating between lpGBT and MAPS Sensors for Slow Control and commands transmission
- Power supply delivery to MAPS sensors
- Biasing (negatively) of charge collecting volume of MAPS sensors

Ancillary ASIC – Power Management

- **MAPS sensors (EIC LAS) will be organized in stave layouts in OB**

Ideas still under construction



UNIVERSITY OF BIRMINGHAM

28 November 2023

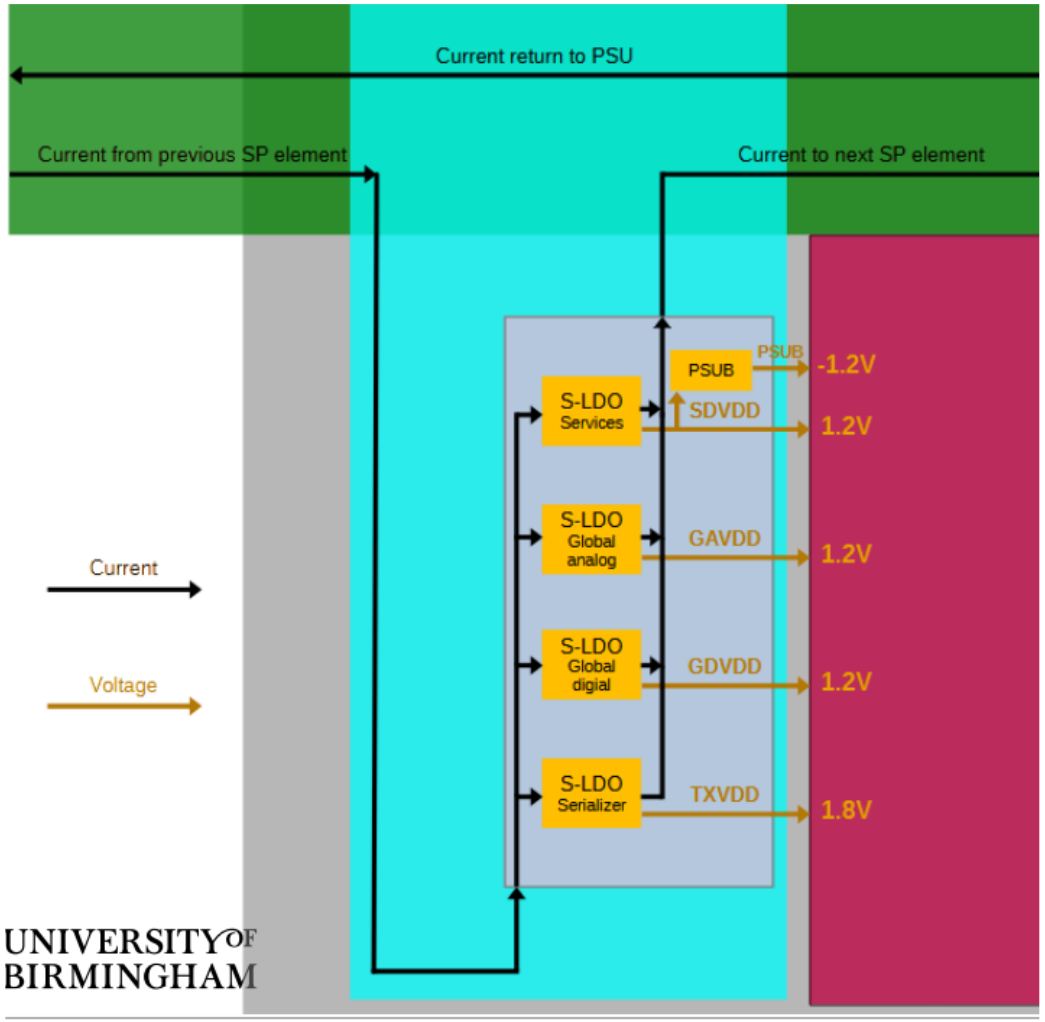
Assumptions:

- Sensor mounted on front and back sides of cold plate;
- LEC overlaps REC;
- Services to stave from the left and right sides;
- FPC will overlap the active area of sensors;
- FPC will impact material budget of active area of Si tracker

AncillaryASIC (AncASIC) will be mounted next to sensors:

- most likely bump bonded on FPC;
- its power consumption will be dominated by SLDOs

Ancillary ASIC on FPC



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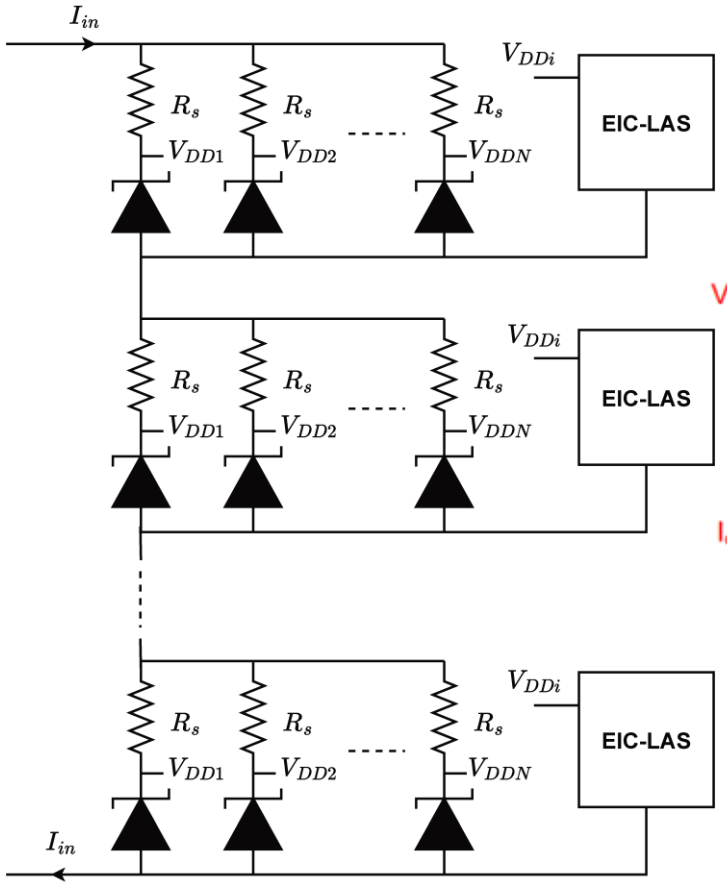
Ancillary ASIC – Power Management

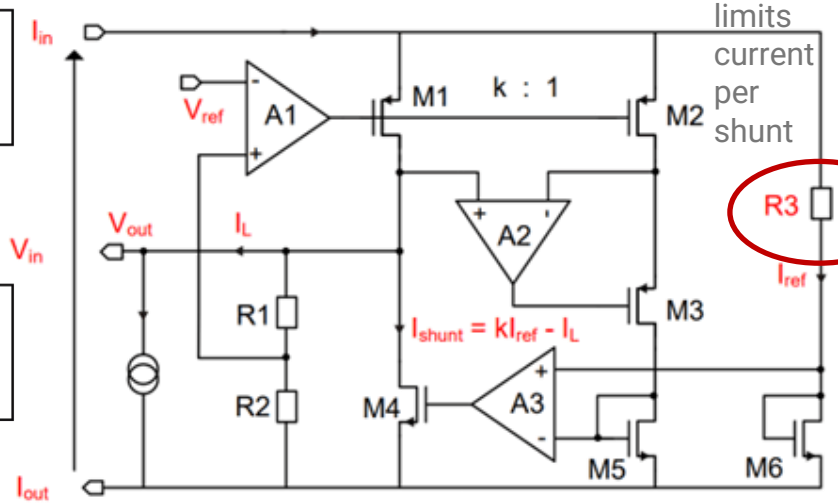
- **Is reduction of SLDO power consumption possible?**

- current design features multiple Shunt - LDOs to generate supply voltages for each EIC-LAS;
- series resistor in each shunt consumes a significant amount of power;

- Idea: use single shunt LDO for each MAPS sensor (EIC-LAS) and set of series LDOs to generate required supply voltages;
- Dropout voltage of each series LDO can be designed to be small (< 100 mV), thus improving power efficiency.



SLDO concept borrowed from ATLAS pixels; there SLDOs are distributed in parallel



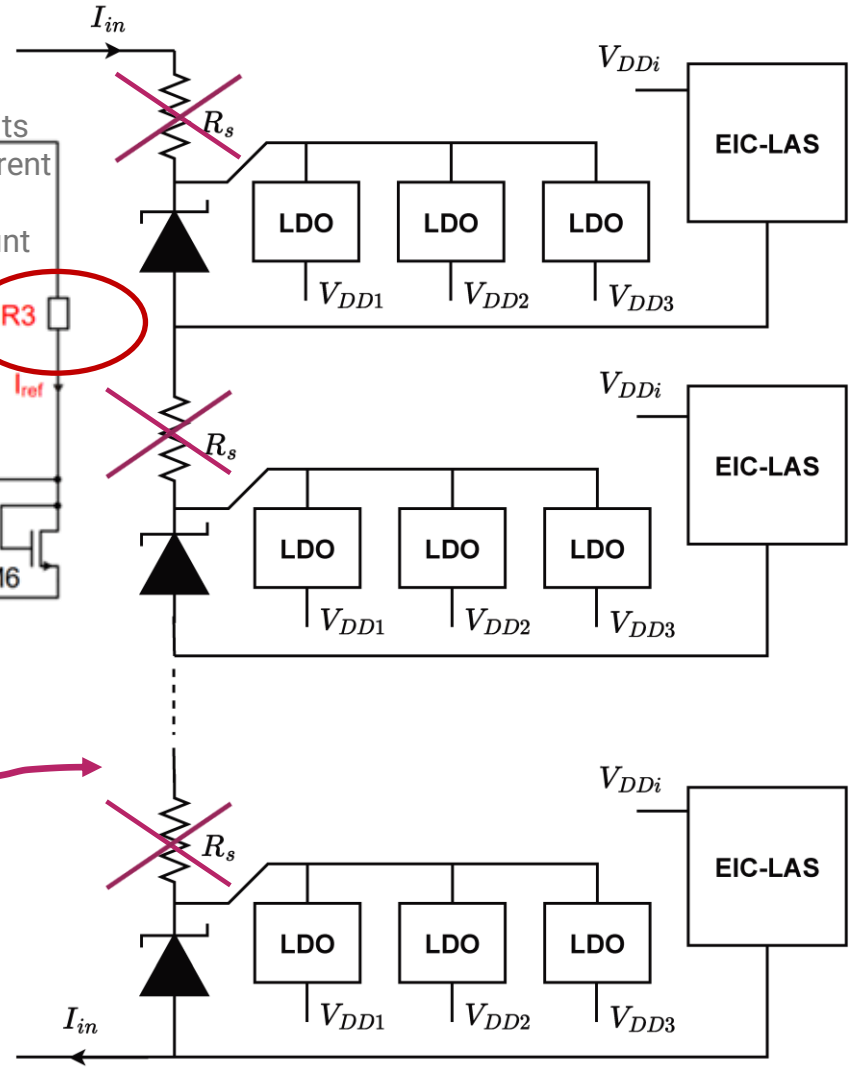
R3 limits current per shunt

Current estimate:

$P_{MAPS}/P_{AncASIC} \approx 2$

This means that 50% of power is wasted not accounting for I^2R in cables

therefore



+10% shunt overhead based on https://cds.cern.ch/record/2292628/files/CR2017_385.pdf

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Ancillary ASIC – slow control

- **There is justified reason why industrially standardized slow control interfaces are DC-coupled**

Interfaces:

- mother of all interfaces: RS-232 is DC-coupled although it uses voltage levels that would give modern people a headache!
- CANBUS (it works in very harsh environment), I^2C, JTAG all, even Centronics are DC-coupled standards;
- RS-485/422 is current-mode interface, and familiarity with it may make considerations simpler.

AC-coupled interface always requires to know how to start and makes more difficult regaining transmission after it is stopped or interrupted;

❖

Slow-control interfaces may remain muted for most of the operation time (why to burn unnecessary power?);

❖

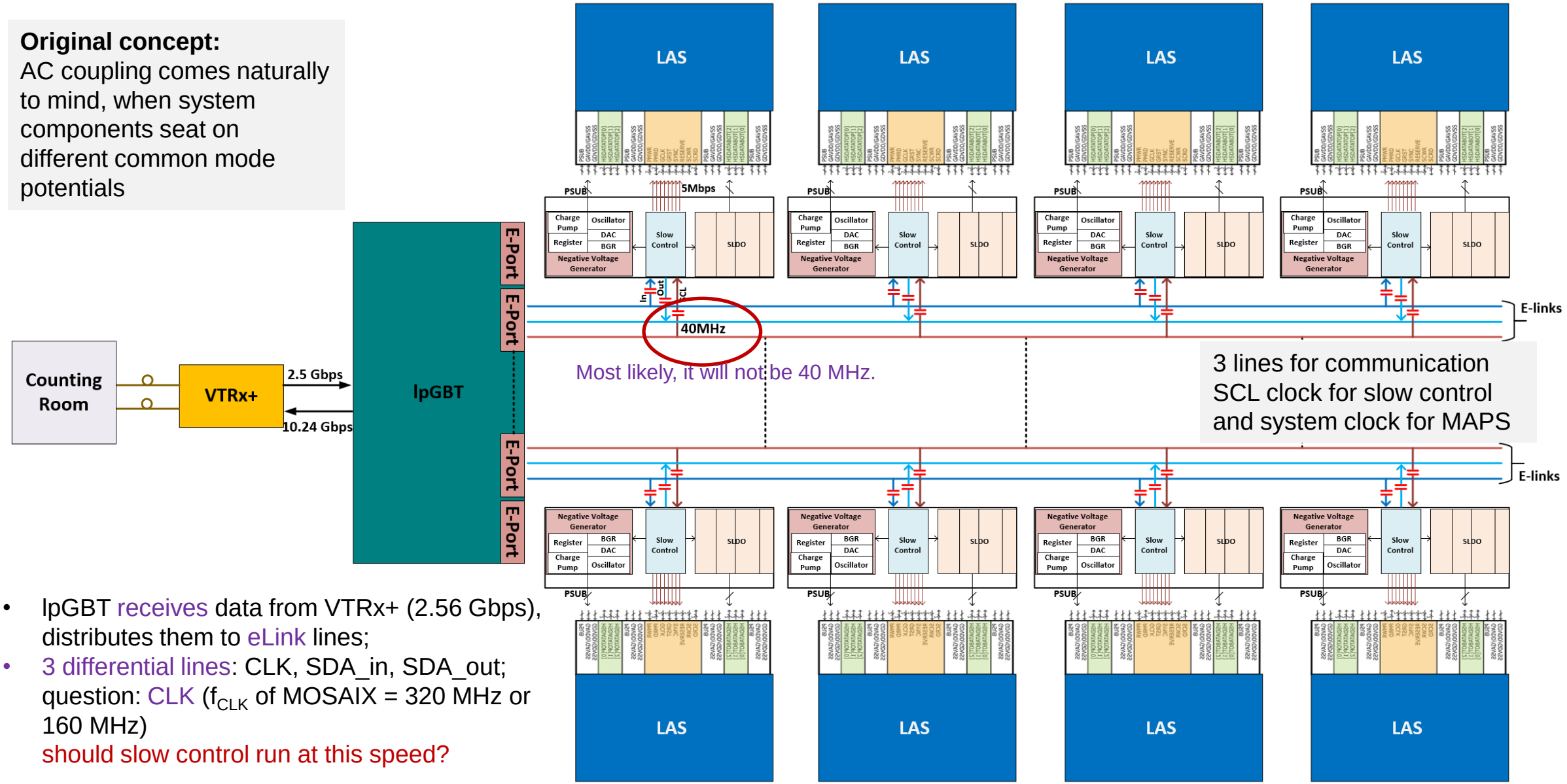
Decision on AC/DC - coupling is neither domain of ASIC nor power and electrical interfaces: it is fully cross domain

wrong choices in power/grounding shielding and slow control

may kill entire detector

Slow control, Block Diagram (AC Coupling)

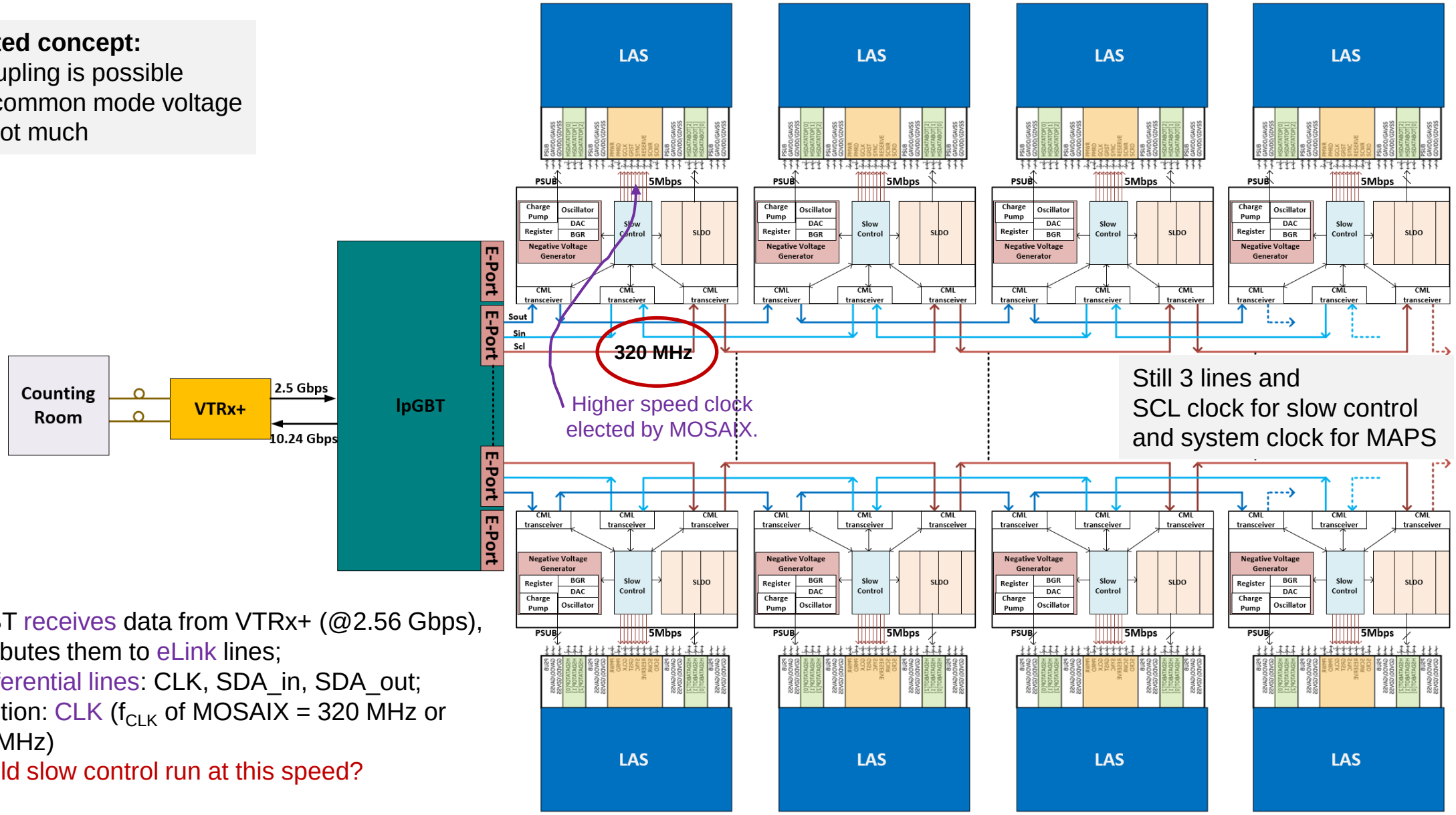
Original concept:
AC coupling comes naturally to mind, when system components seat on different common mode potentials



- lpGBT receives data from VTRx+ (2.56 Gbps), distributes them to eLink lines;
- 3 differential lines: CLK, SDA_in, SDA_out; question: CLK (f_{CLK} of MOSAIX = 320 MHz or 160 MHz)
  should slow control run at this speed?

Slow Control, How about DC Coupling? Better choice!

Adjusted concept:
DC coupling is possible when common mode voltage differ not much

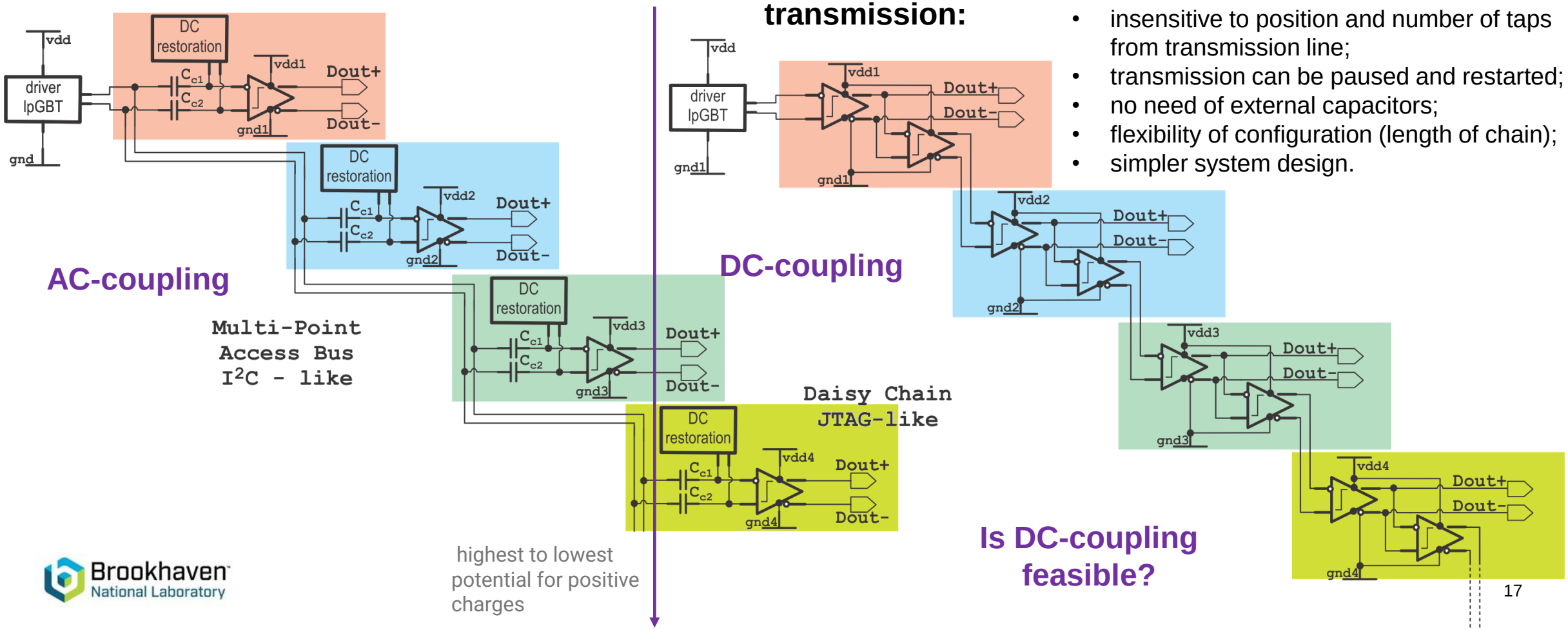


- lpGBT receives data from VTRx+ (@2.56 Gbps), distributes them to eLink lines;
- 3 differential lines: CLK, SDA_in, SDA_out; question: CLK (f_{CLK} of MOSAIX = 320 MHz or 160 MHz)
  should slow control run at this speed?

Slow Control, Interfacing lpGBT downlink -1

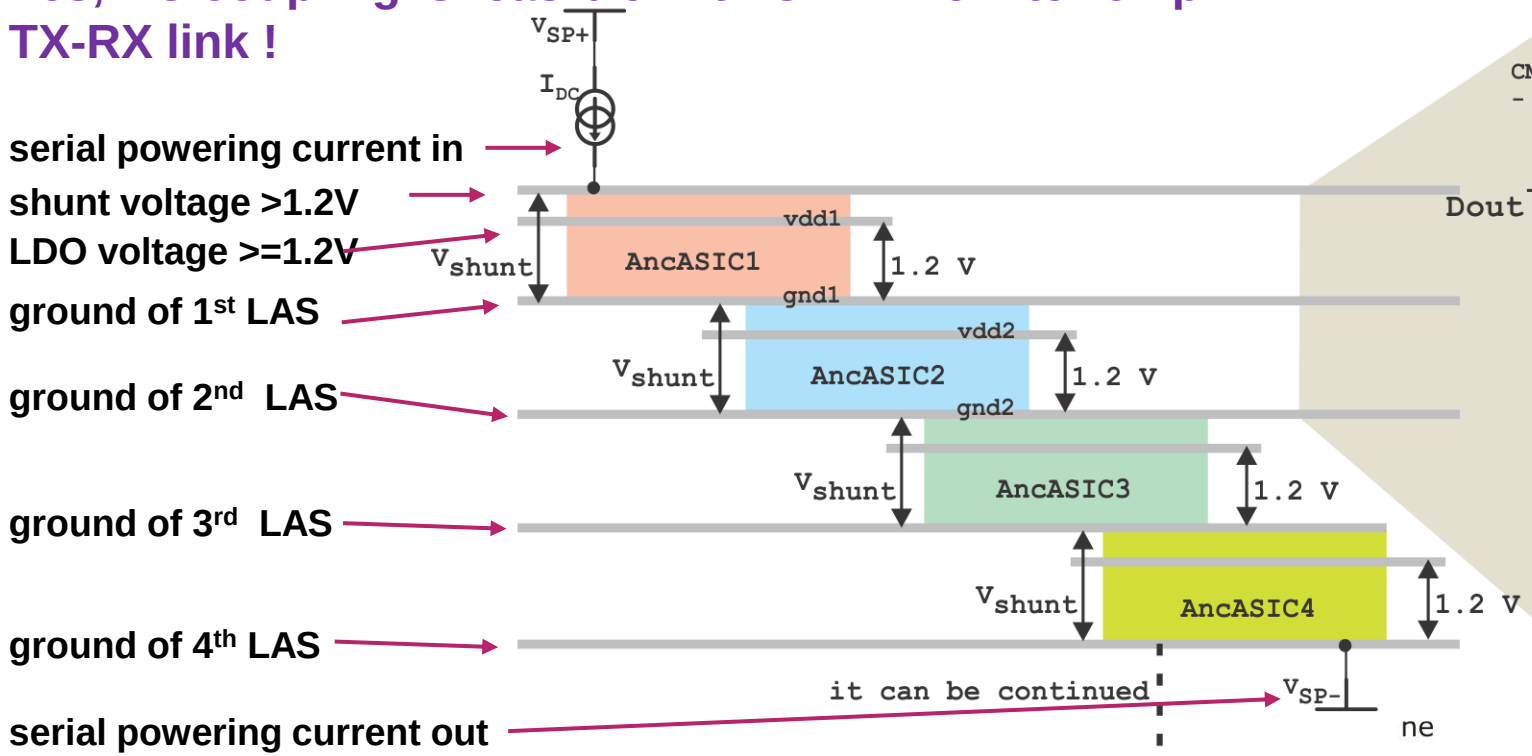
- **Ancillary ASIC seats between lpGBT and EIC LAS on OB staves and disks**
- **Serial Powering makes each EIC LAS seat on local ground (gnd1, gnd2, gnd3 …)**

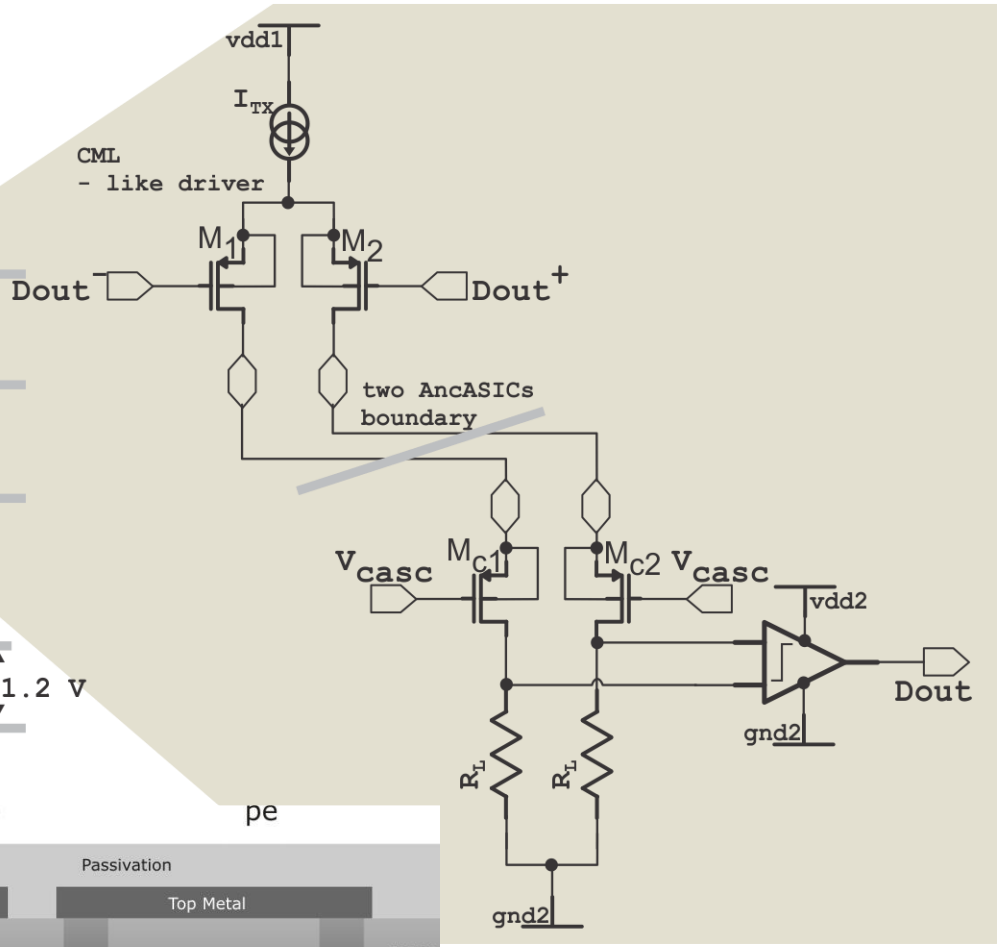
- **Communication to and from lpGBT must take into account gnd1…4 potential differences into account**
- **Natural seems to use AC-coupling, but DC-coupling offers advantages for transmission:**
  - insensitive to position and number of taps from transmission line;
  - transmission can be paused and restarted;
  - no need of external capacitors;
  - flexibility of configuration (length of chain);
  - simpler system design.



Slow Control, Interfacing lpGBT downlink -2

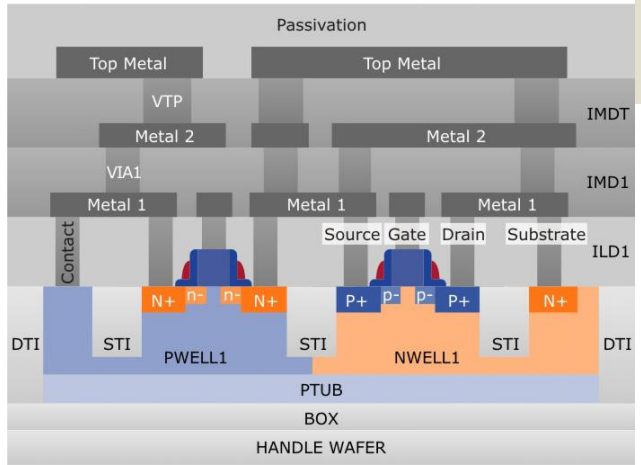
Yes, DC coupling is feasible with CML-like inter-chip TX-RX link !





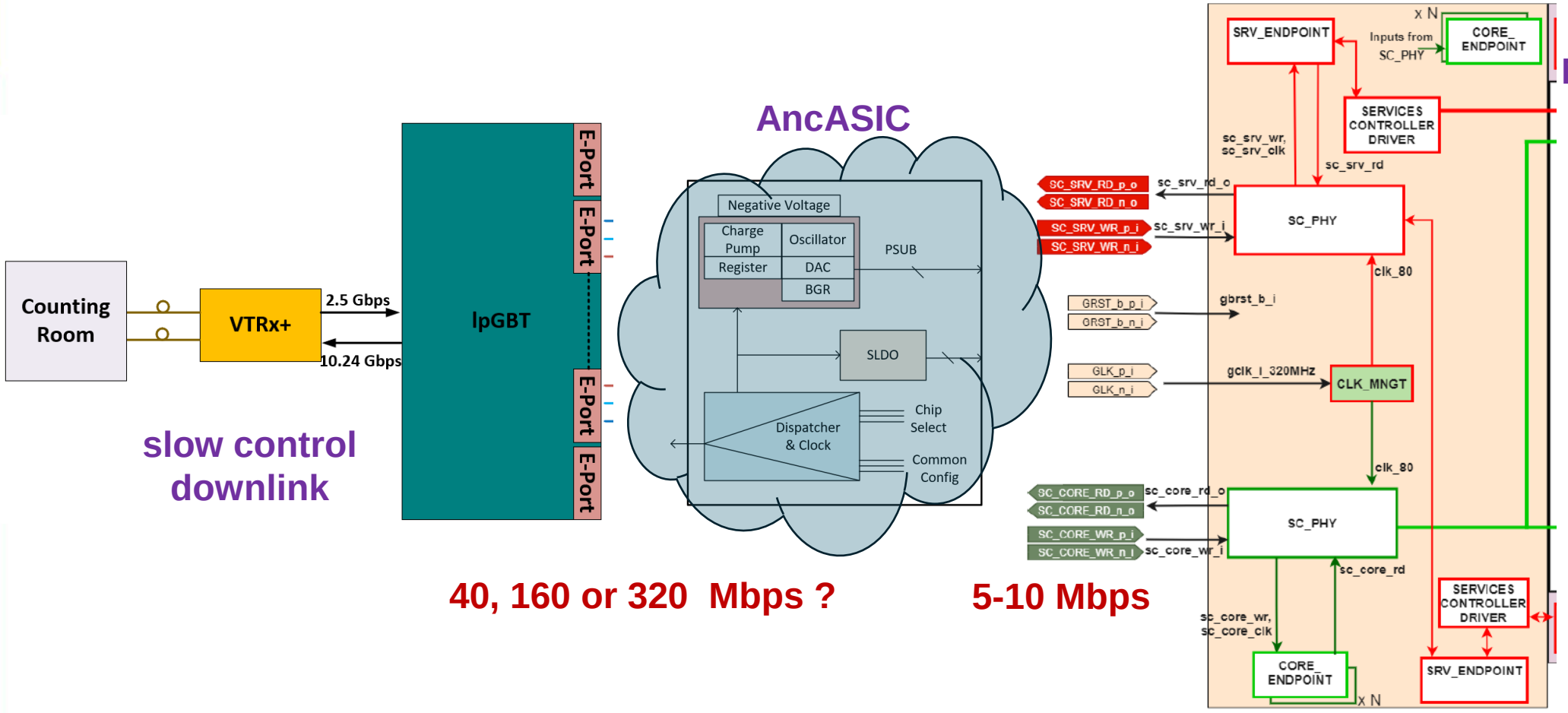
enabling elements for the design:

- small potential differences (X00 mV) between **vdd** and **gnd** of two neighboring AncASICs;
- selection of Partially Depleted SOI CMOS process comes with all transistors isolated and having their terminals *hanging slightly below or protruding slightly above* ground and power potential of predecessor and successor.



cross-section of XT018 process
with selected metal stack option and
featuring deep trench isolation DTI

Slow Control, Interfacing lpGBT downlink -3



slow control downlink

40, 160 or 320 Mbps ?

5-10 Mbps

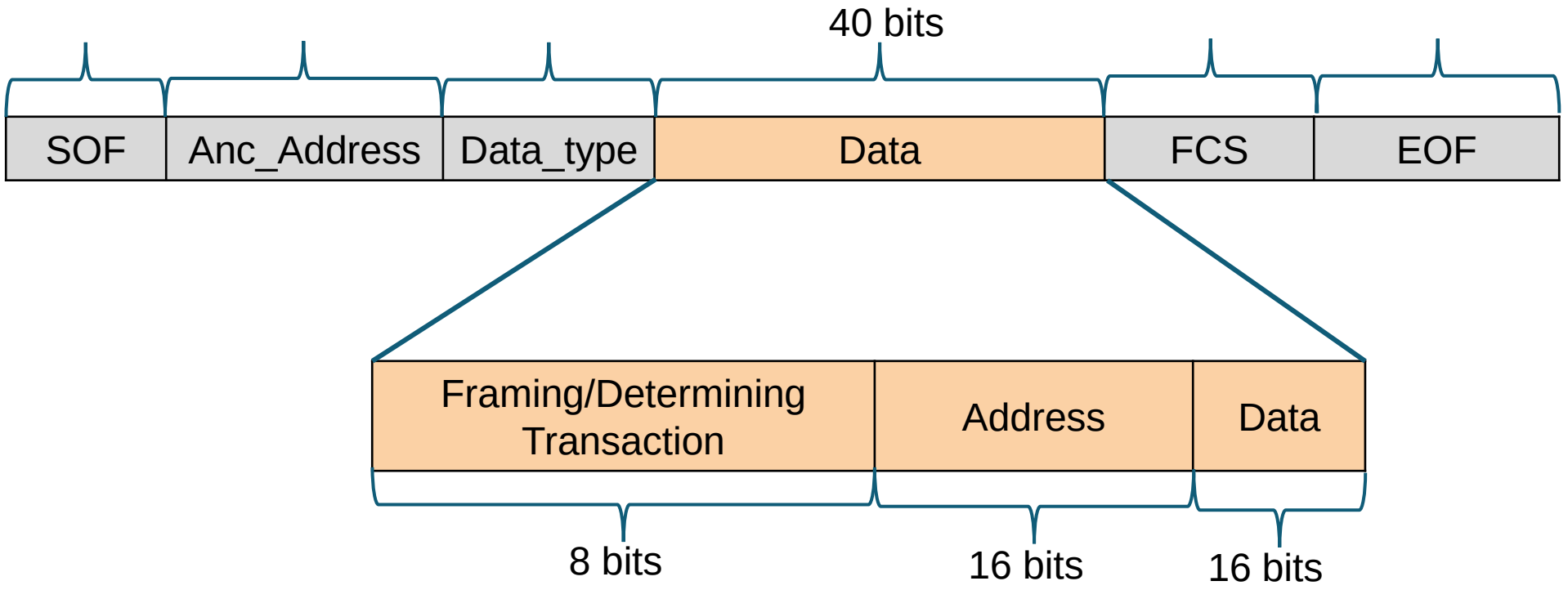
MOSAIX / EIC-LAS interface

MOSAIX (all diff. CLPS):
Clock - input
Reset - input
Sync - input
2× slow control – input/output
Services management
Core management
1× reserved

– +HS Data (all differential):
8× high-speed channels (4 top, 4 bottom)

Slow Control, Interfacing lpGBT downlink -5

proposal of slow control data framing, including AncASIC intermediate features



- **SOF:** Start of Frame
- **Anc_Address:** Address of Ancillary Chip
- **Data_Type:** Read/Write
- **Data:** To MOSAIX / EIC-LAS
- **FCS:** Frame Checksum Field
- **EOF:** End of Frame

MOSAIX/EIC-LAS SC interface:

- controls power, configuration and monitoring;
- is serial, half-duplex bidirectional;
- differential, with independent signal pair up and down stream;
- DC-balanced data, Manchester enc.
- line rate 5-10Mbps;
- immune to errors and wrong transmissions

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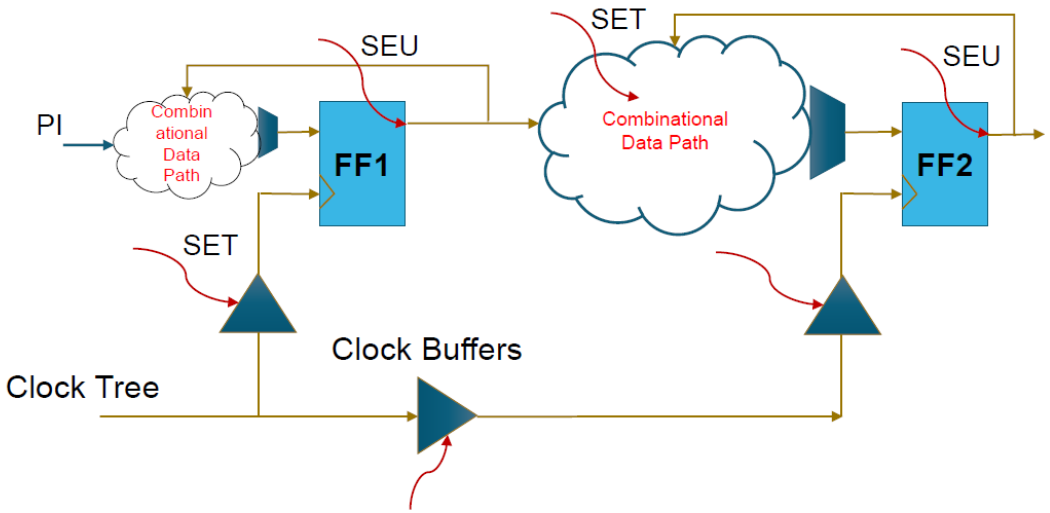
Slow Control, Interfacing lpGBT downlink -4

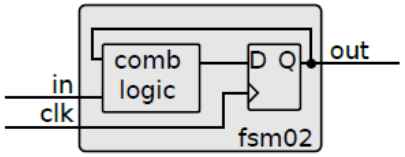
Current work focused on writing down protocol, specification and define development timelines:

- matching of clock speeds of eLinks and MOSAIX/EIC-LAS interface requires buffering of data inside AncASIC;
- data sent from lpGBT must be formatted to contain:
  - addresses of AncASIC (eFuse-burned), and
  - addresses / data following MOSAIX/EIC-LAS data structure (address-data);
- internal configuration of AncASIC built consistently with MOSAIX (for uniformity of data exchange protocol);
- data integrity methodology (checksums, correction, triplication, read back) tbd.;
- addition of built in fast commands (reset, synchronize MOSAIX readout, status readout, etc.);
- MOSAIX debate: 320 / 160 MHz system clock – should it be slow control transmission clock or 4th line is needed for system clock?

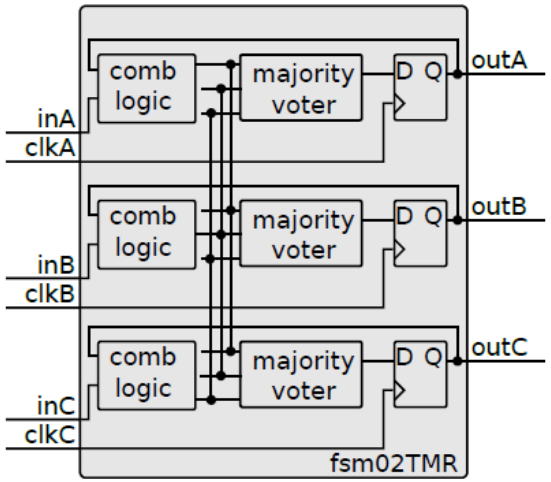
Information on MOSAIX interface available from ITS3-WP6;



mitigation of soft errors:
Transient & Static
SET in combinational logic
SEU in memory cells / flip-flops



Simple FSM



Triplicated FSM

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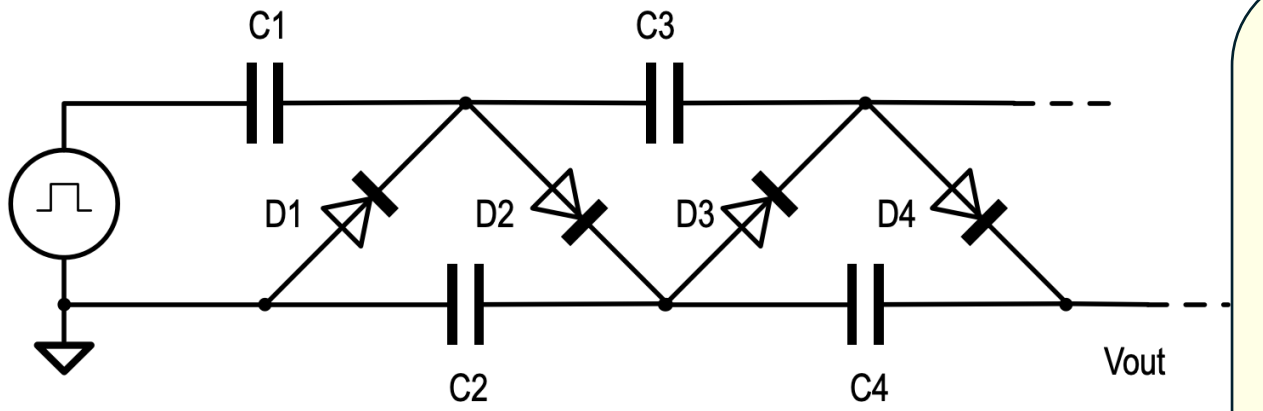
Negative Voltage Generator / Regulator

NegVReg creates negative bias for charge collecting volume from positive regulated power supply 1.2 V

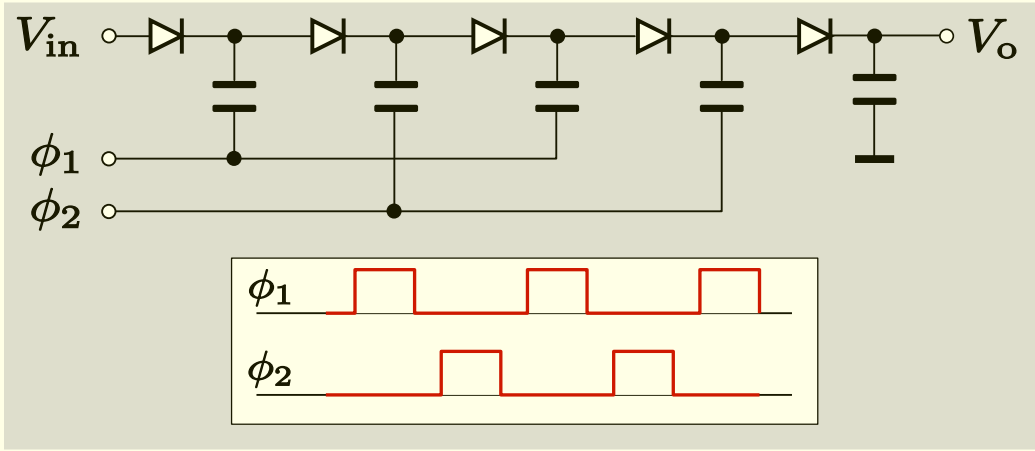
- settable range ∈(~0 V, -6 V) and current drive up to 1 mA;

⇨ diode-based charge-pump circuit

- Two main topologies: Cockcroft-Walton and Dickson (hybrids are also possible).
- Cockcroft-Walton: RF signal is fed in series.
  - The DC voltage across each capacitor is limited to ~V_{RF}, so very high output voltages are possible.
  - The output impedance increases rapidly with number of stages since all the capacitors are in series.
- Dickson: RF signal is fed in parallel
  - The DC voltage across each capacitor equals V_{OUT}, limiting the maximum output voltage.
  - The output impedance increases less rapidly since the capacitors are in parallel.
- The current design requires a modest output voltage, so the Dickson topology is preferred.



Cockcroft-Walton multiplier



Dickson charge pump

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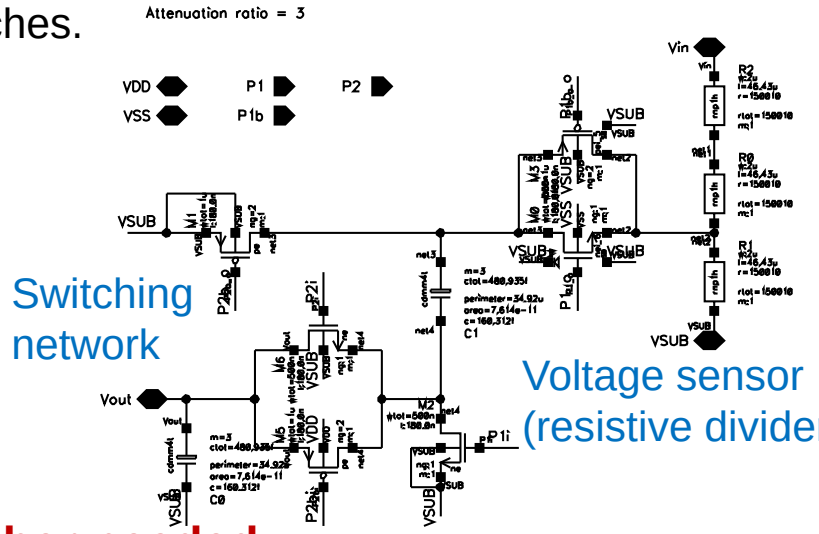
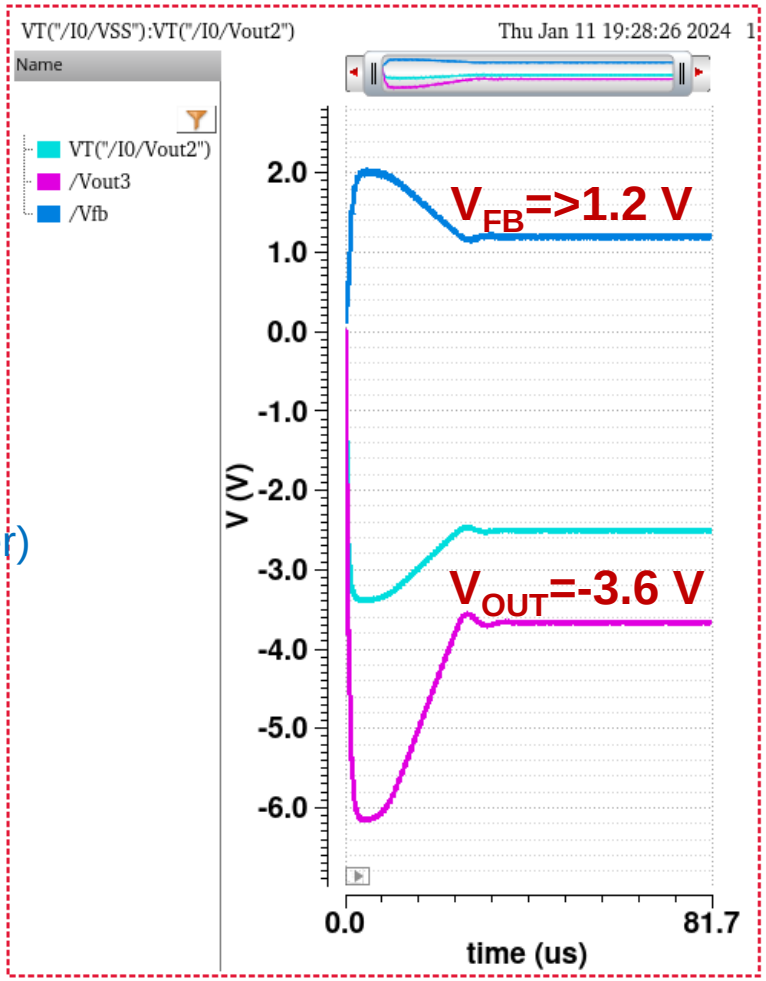
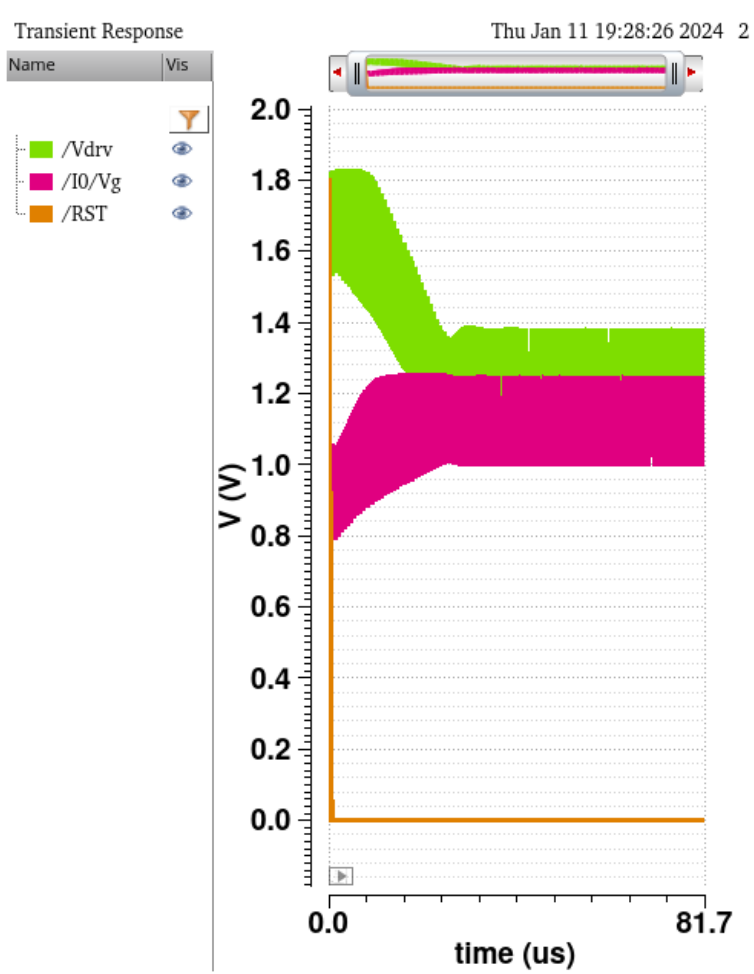
Negative Voltage Generator / Regulator

Circuit Design progressed to demonstration of feasibility

Basic circuit charges capacitor to αV_{IN} (where α = 1/3 in this case), then flips its polarity using switches.







Closed-loop simulations V_{REF}=1.2 V

- $V_{OUT} = -V_{REF}/\alpha = -3 \times V_{REF} = -3.6V$.
- C_L = 10 pF (small value w.r.t. real to reduce $T_{simulation}$).

Further needed:

- more realistic model of output load MOSAIX/EIC-LAS) including I_{leak}, to optimize design;
- corner and Monte Carlo simulations;
- implement spread spectrum modulation;
- design voltage DAC to generate V_{REF} for digital programming of output voltage of NegVReg;
- complete trial layout and evaluate impact of layout parasitics;
- use enclosed layout transistors (ELTs) if needed to improve radiation hardness;

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Specifications and design

- component functional blocks are being identified;
- full specification of AncASIC is underway;
- targeted project completion by end of CY2024;
- testing with MOSAIX sensors in ER2 in future;

ePIC SVT - Specification for EIC-LAS and Ancillary Chip

March 14, 2024

1 Introduction

This document contains specifications for the chips needed for construction of the ePIC SVT - the EIC-LAS and the ancillary chip.

2 Negative Bias Generator

This block provides a negative voltage to back-bias the EIC-LAS. This is necessary because the level of the back-bias voltage is sufficiently low, and requried to be sufficiently precise, that it is needed to generate the negative voltage relative to the local ground in the serial powering chain.

2.1 Specifications

Negative Bias Generator Specification				
Specification	Unit	Value	Comment	Status
Voltage Range	V	0 to -6	Relative to local ground	
Current Capacity	A	10^{-3}		
Voltage Ripple	mV	< 0.1		
Power	W	$< 10^{-2}$		
Supply Voltage	V	1.8		
Area	μm^2	4×10^5		

2.2 Outstanding Questions

1. Level of radiation hardness required?

3 SLDO

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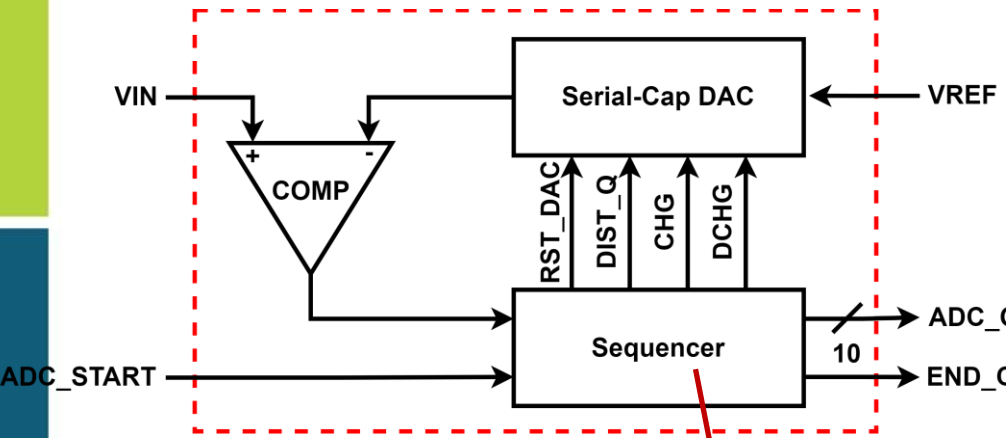
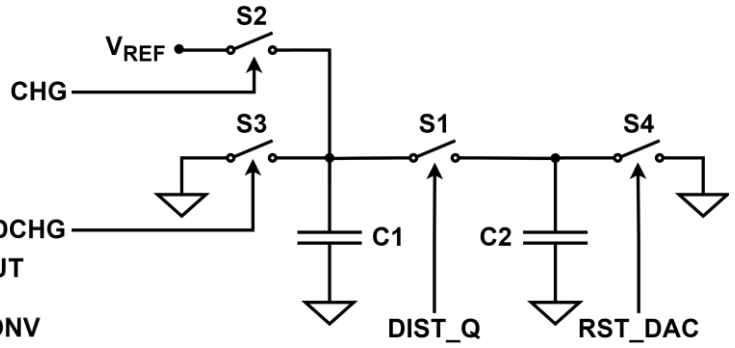
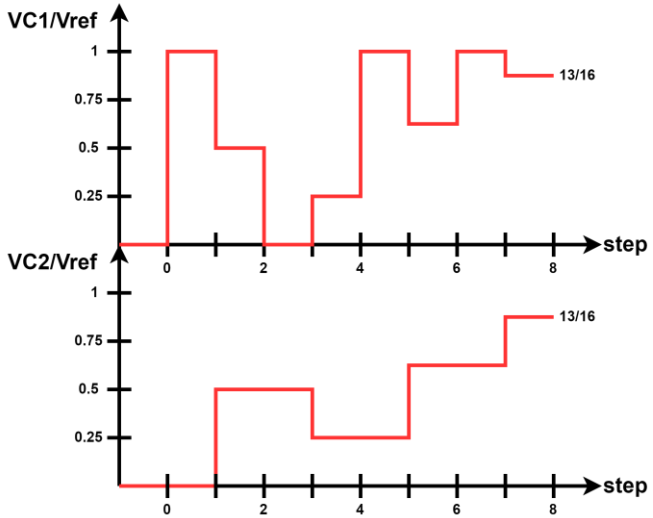
VFM_ADC

Small footprint ADC for collecting information on health of MAPS sensors:

VFM_ADC, self clocked, <5,000 μm²,10 b ADC

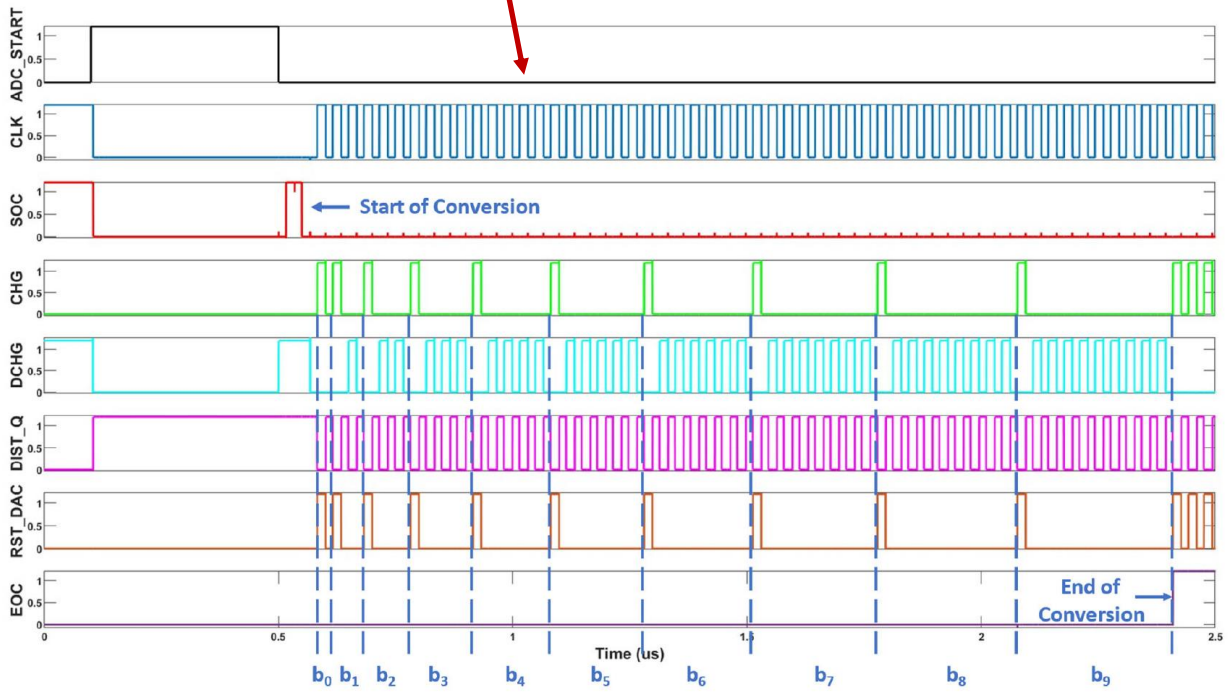


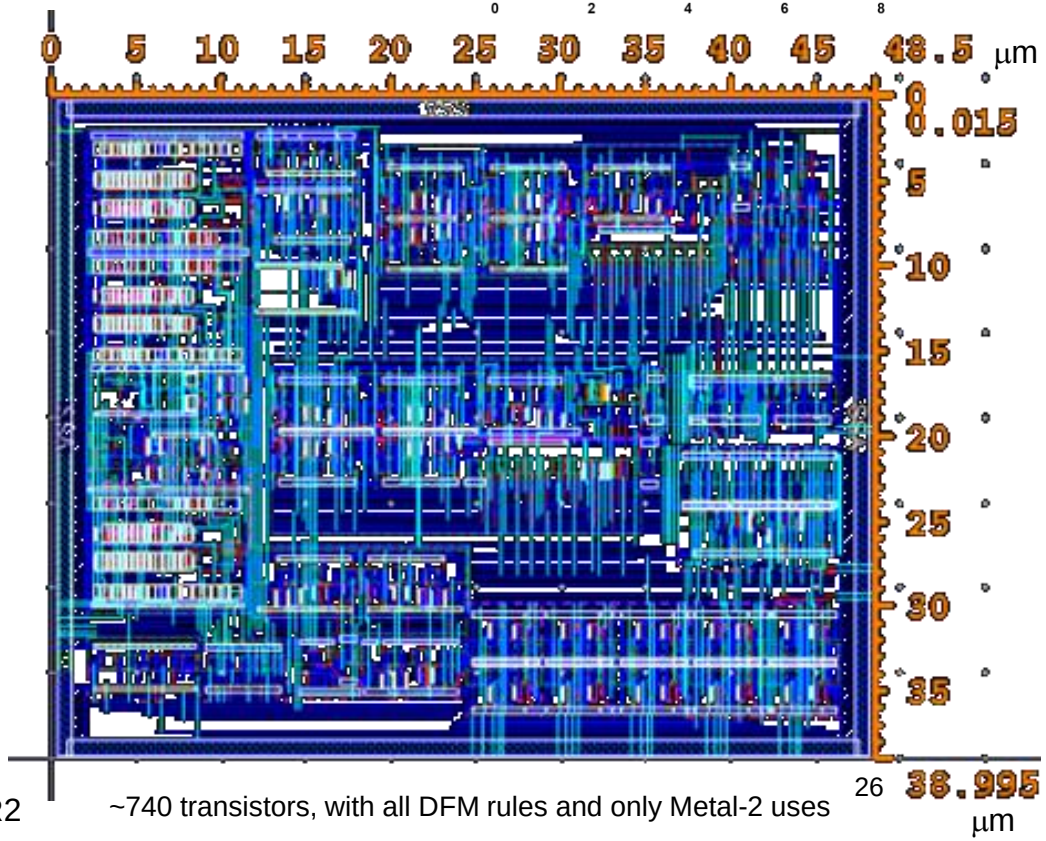




doi: 10.1109/JSSC.1975.1050630.

sequencer and its operation





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gained familiarity with TPSCo 65nm process and planning to include in ER2

~740 transistors, with all DFM rules and only Metal-2 uses

Testing and Assembly

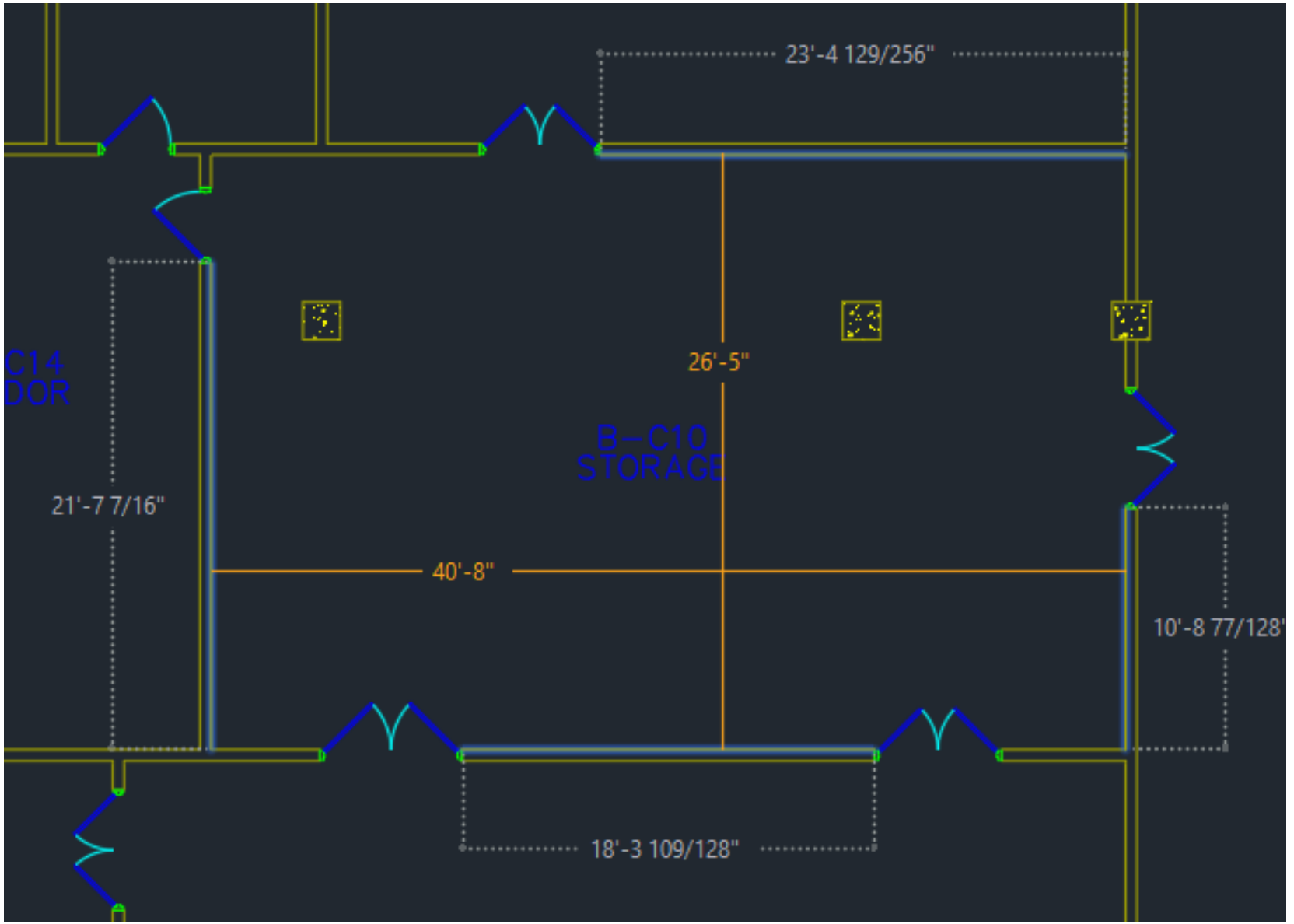
Organize equipped laboratory space

Testing and Assembly

Test, assembly & calibration laboratory for ePIC components arriving at BNL before installation

deeded space in IO 535B basement

- space for each ePIC SVT participating institution;
- 2 large optical tables;
- ESD proof test benches and storage cabinets;
- 12-inch probe station with temperature control;
- environment controlled chamber;
- coordinate metrology and calibration;
- semiconductor characterization instruments;
- data acquisition resources;
- services: vacuum, dry air compressed air, nitrogen;
- high-density interconnect, plasma cleaning, rework;



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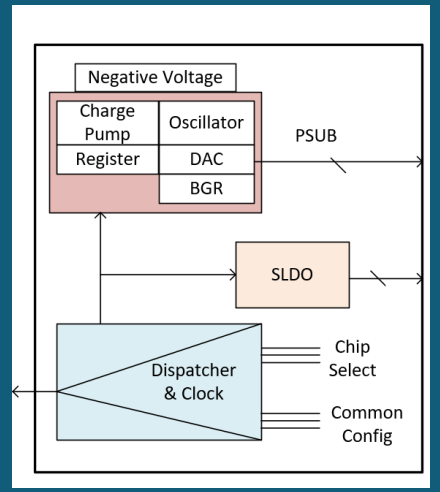
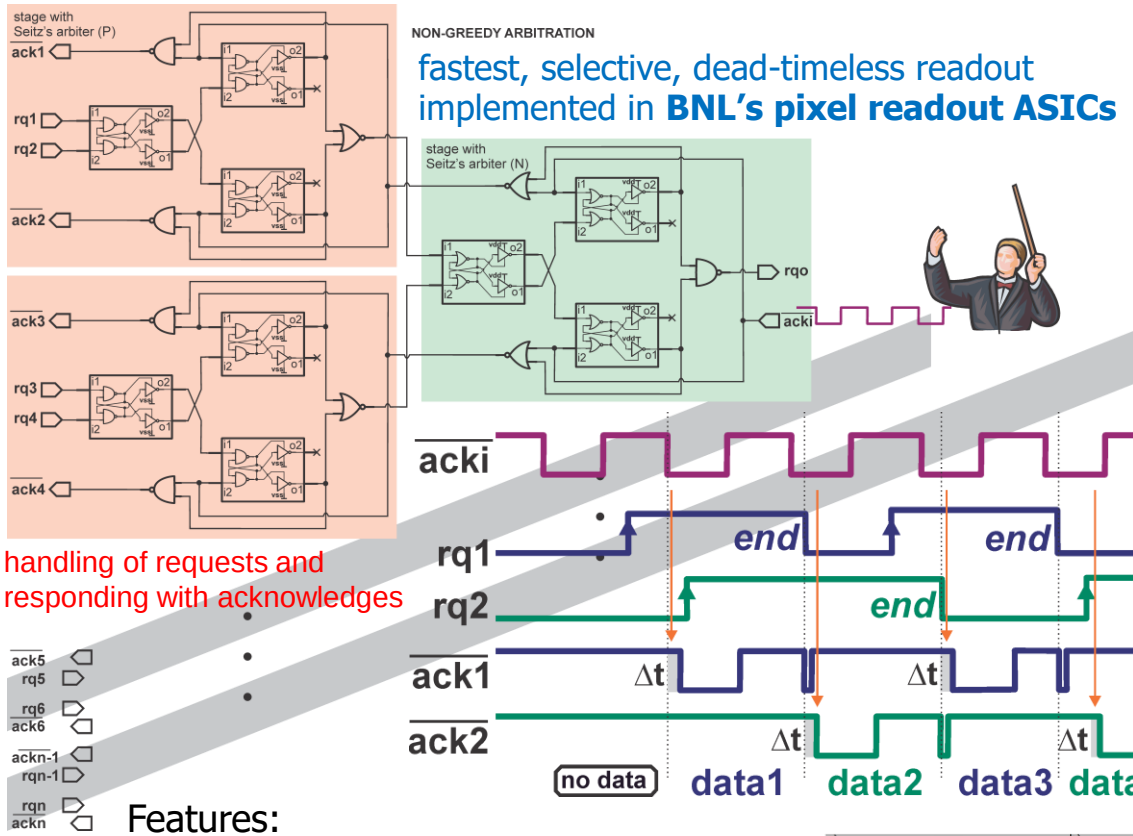
Ancillary ASIC



3 functions:

- Intermediating between lpGBT and MAPS Sensors for Slow Control and commands transmission
- Power supply delivery to MAPS sensors
- Biasing (negatively) of charge collecting volume of MAPS sensors

Upgrades R&D -1



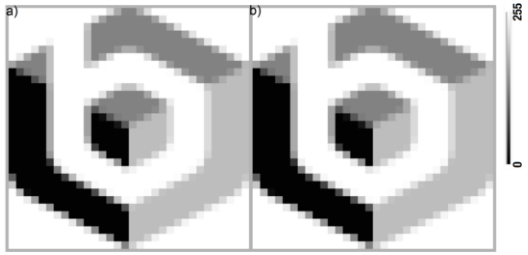
handling of requests and responding with acknowledges

fastest, selective, dead-timeless readout implemented in **BNL's pixel readout ASICs**

Features:

- **Event-driven** ➡ hits extracted from matrix of pixels on the fly, without snapshotting in readout frames;
- Energy-efficient ⬅ no clock, no strobes distributed to other but being read out pixel;
- Silicon-proven and patent pending;

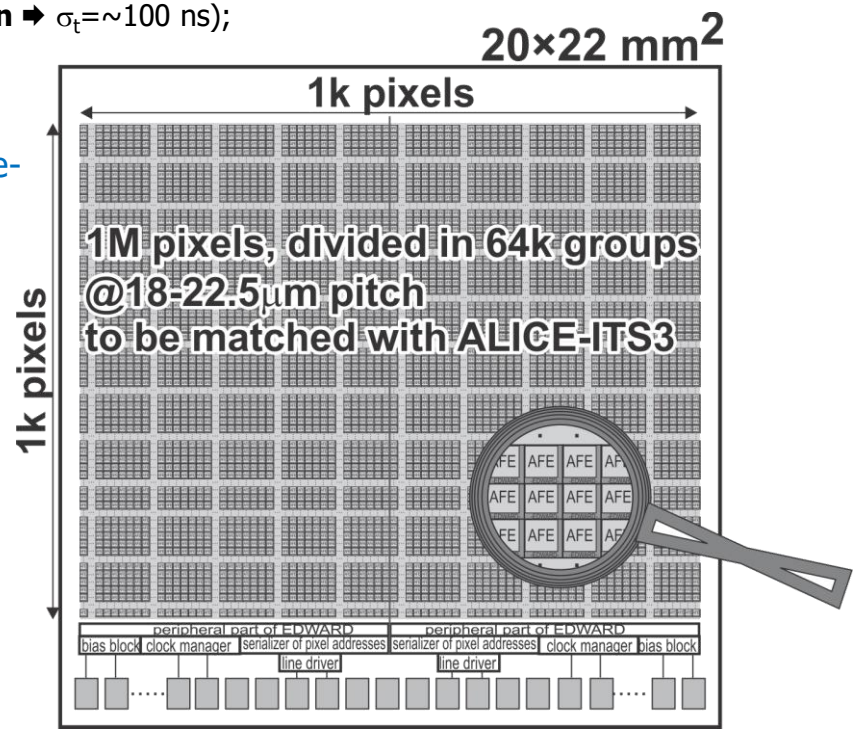
WO/2022/221068: Event-Driven Readout System with non-priority arbitration for multichannel data sources

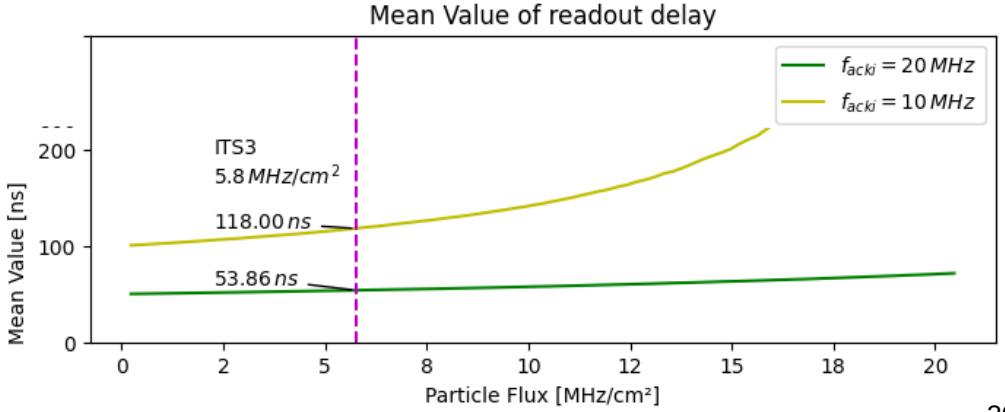


number of readouts as intensity maps:	as programmed using I2C-SPB interface	as actually read out from all pixels

- ALICE-ITS3 is **priority-encoder** based with **framed readout** ➡ poor σ_t=5 μs);
- **Event-driven** ➡ σ_t=~100 ns);

Binary, event-driven mode operated large-area MAPS **(LDRD-A)**

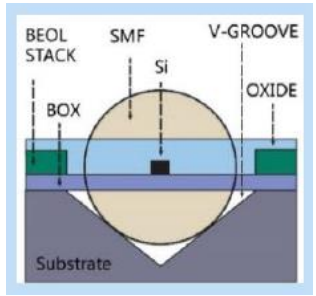


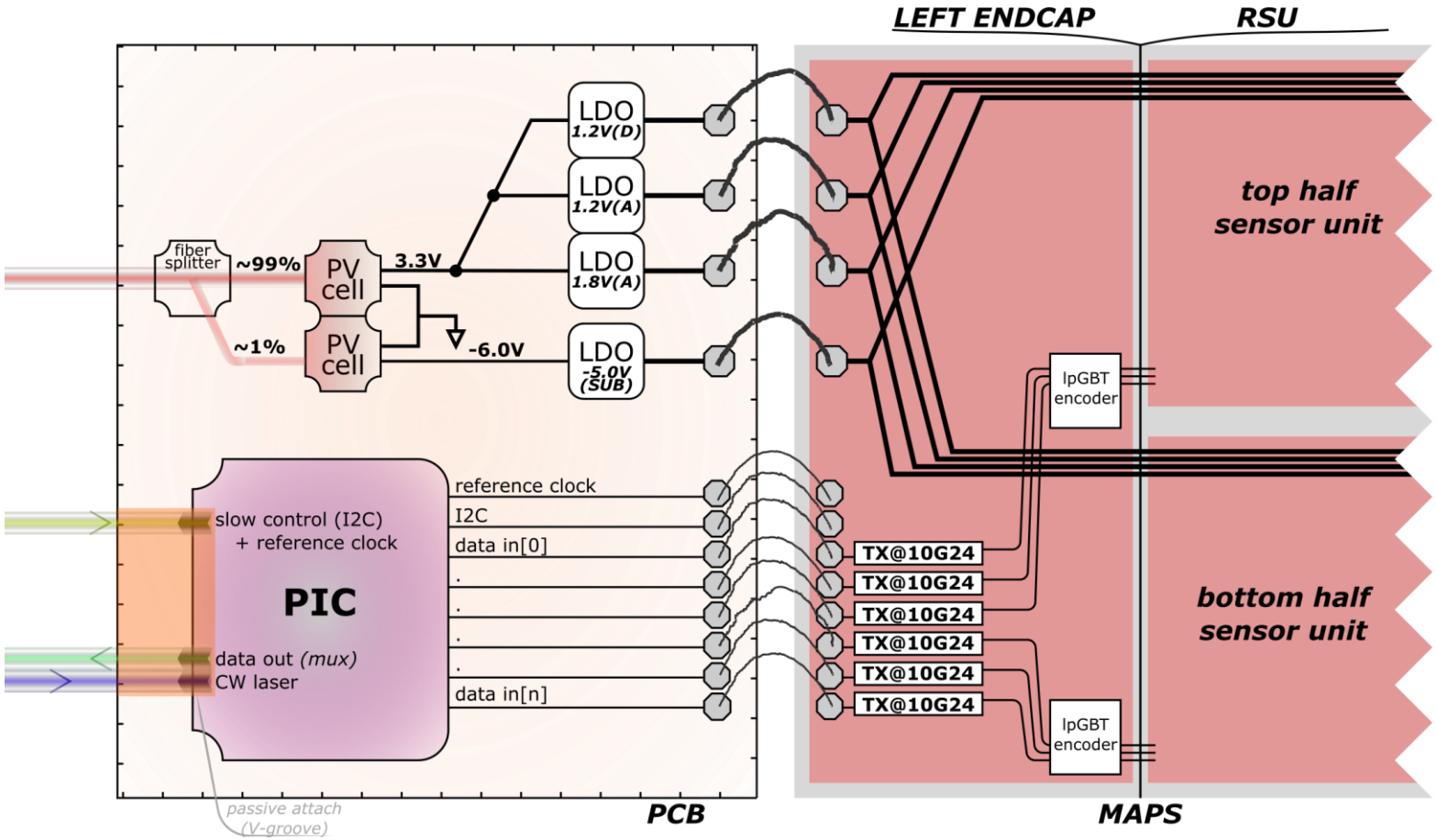


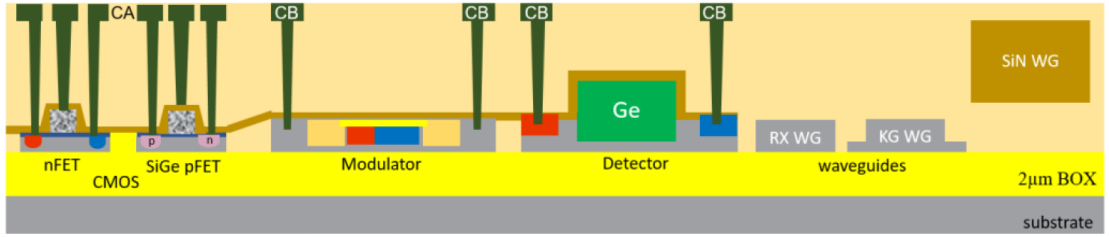
Upgrades R&D -2

Entirely galvanically isolated detector **(generic R&D)**

- **Power ➡** by light on fiber and PV cells;
- **Slow Control and Reference Clock ➡** delivered on fiber
- **High-Speed data ⬅** on fiber, wavelength multiplexed, EOM = Photonic IC (PIC)







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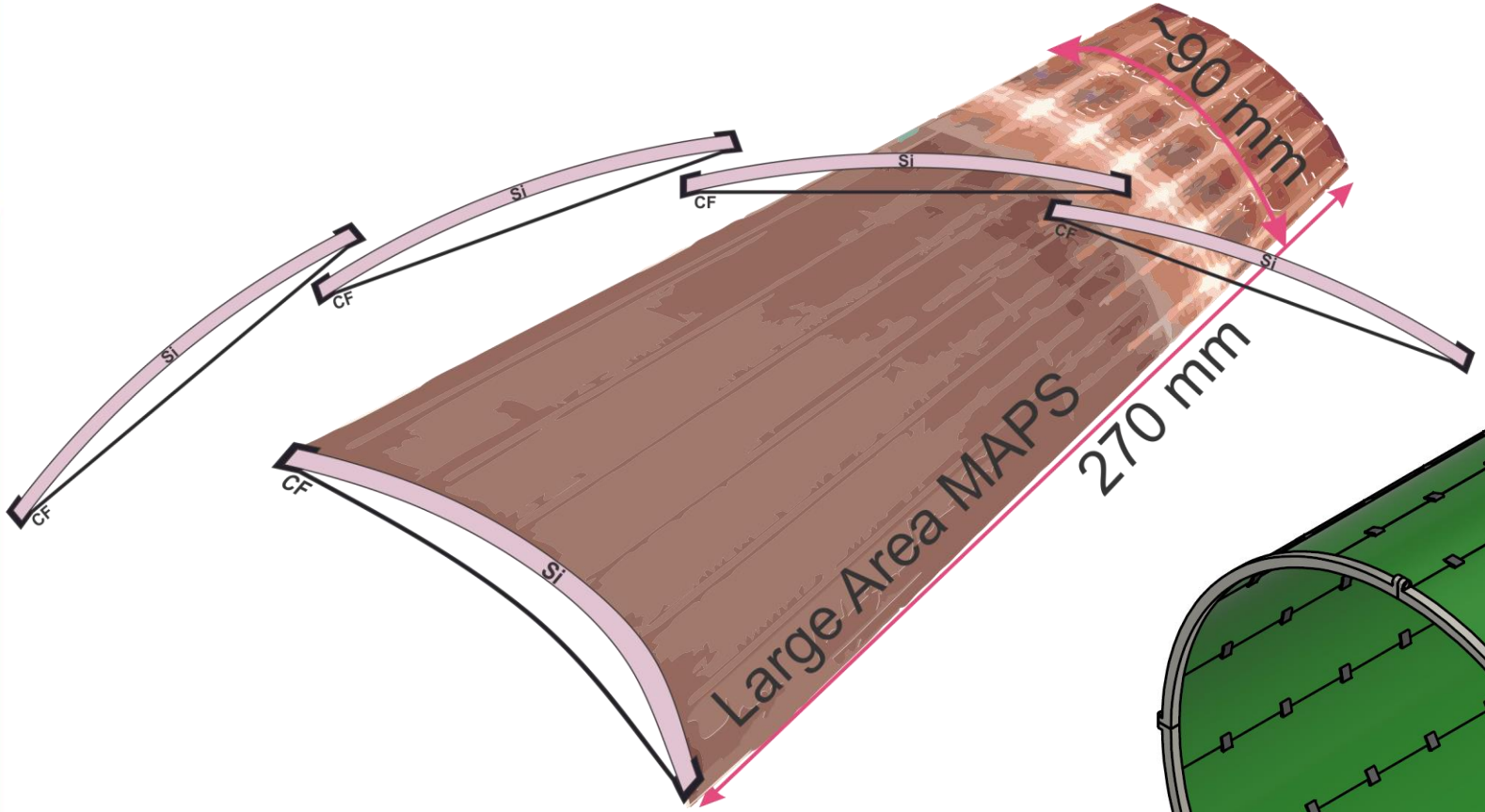
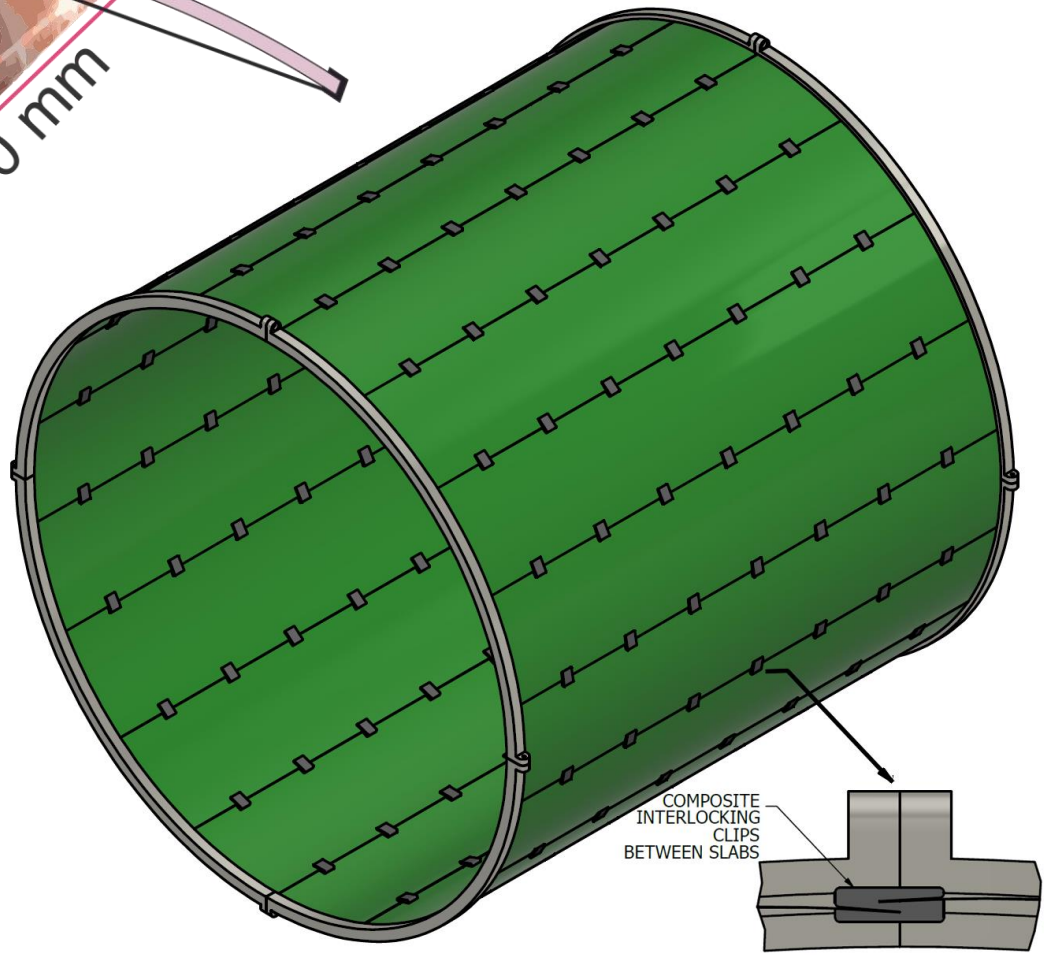
Upgrades R&D -3





R&D on self-supporting, larger-radius cylindrical layers achieved with pre-bent MAPS

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Summary

- **Multiple activities:**
  - emphasis is placed on the baseline ePIC SVT;
  - R&D visible being shifted to PED (specifications under constructions);
  - R&D for the upgrades is ongoing both on sensors and services/readout infrastructure