The FMC Connector Pinout of the RDO Prototype (ppRDO)

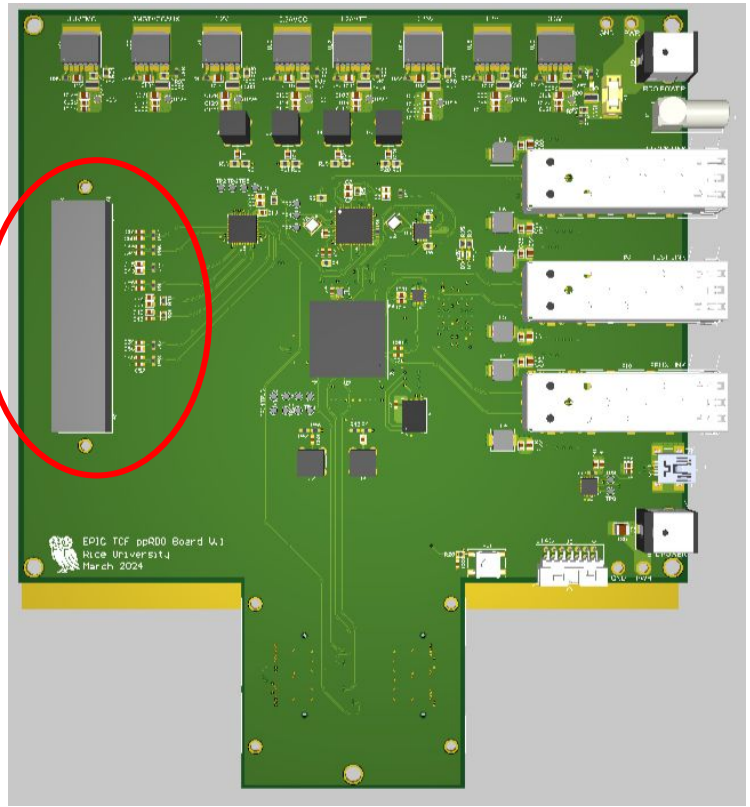
Tonko Ljubicic, Rice University
21 Mar, 2024

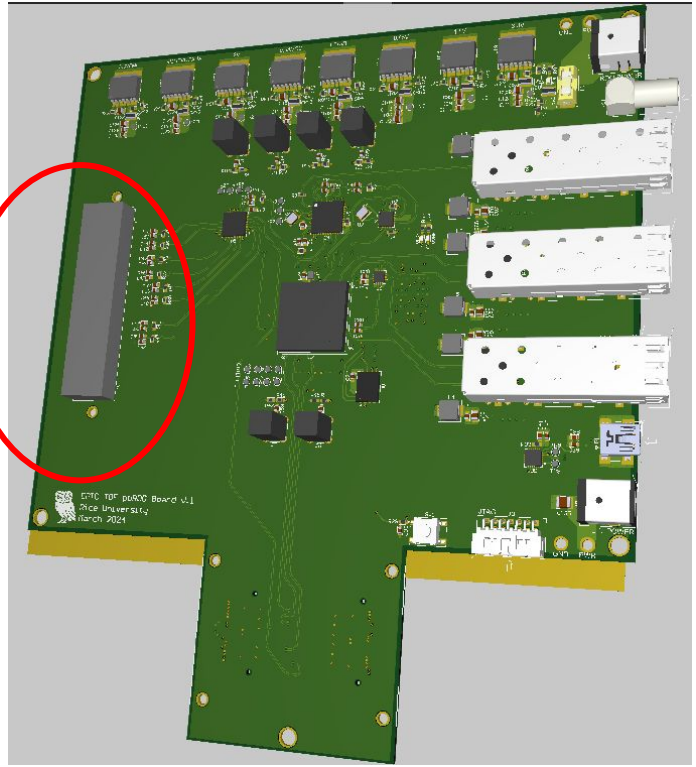
Recap: what's the ppRDO?

- Prototype RDO Project via eRD109
  - produce a generalized RDO using the Xilinx Artix Ultrascale+ FPGA
  - use it to finalize
    - the timing distribution schemes
      - via the reconstructed clock ala CERN's TClink
      - via the direct clock on the fiber
    - power needs of the various components and the myriad of FPGA's voltages
    - connect to various EPIC ASIC test boards for continued prototyping using FMC
    - develop EPIC DAQ fiber primitives
    - final radiation tests of the components (FPGA, PLLs, PROM, SFP, etc)
- ppRDO is in the production stage

ppRDO

FMC

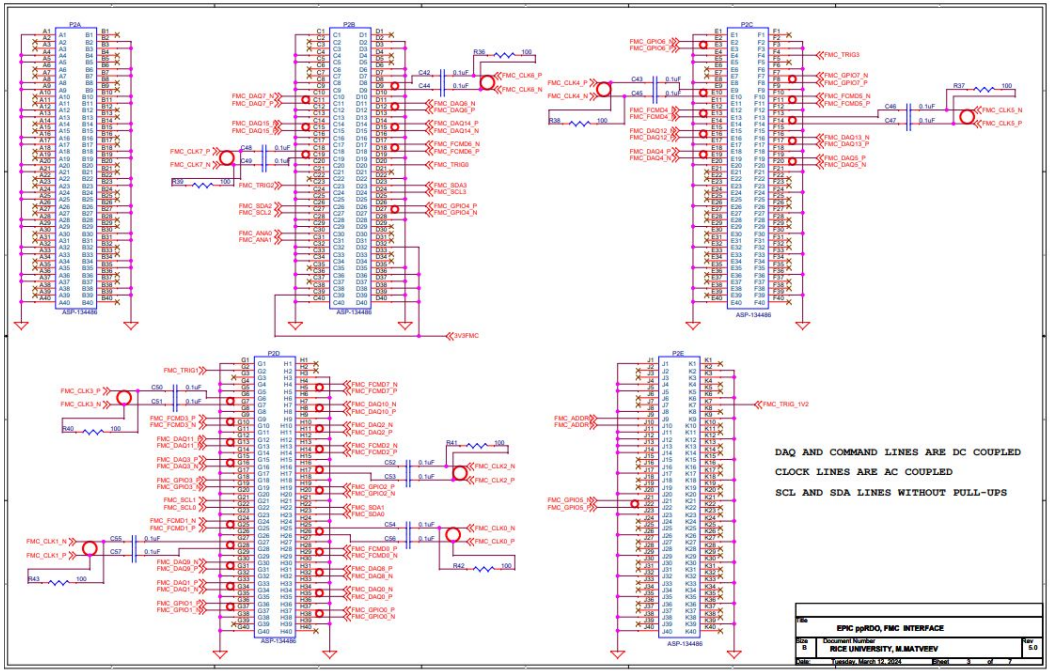

EPIC TOF ppRDO Board V.1
Rice University
March 2024


EPIC TOF ppRDO Board V.1
Rice University
March 2024

FMC Connector

- FMC HPC flavor
  - 8 differential clock lanes directly from a low jitter fanout PLL (“ASIC Clock”)
  - 8 differential data lanes from the FMC to the FPGA (“Data In”)
  - 8 differential data lanes from the FPGA to the FMC (“Fast Command”)
  - 8 differential general purpose lanes to/from the FPGA
  - 4 I2C busses (SDA & SCL) to/from the FPGA
  - few single ended general purpose signals to/from the FPGA
  - 3.3V, 2A power on the standard FMC “3V3” pins
- all single signals are LVCMOS12 at the FPGA
- all (apart from clock) differential lines are DIFF_SSTL12_DIV at the FPGA
- same pinout as Miklos et al for the HGCROC ASIC test board

ppRDO & FMC schematics



⇐ screenshot for illustration only

Full ppRDO schematics:

https://twiki.cern.ch/twiki/pub/Main/EpicSH/RDO_schem_031324.pdf

Conclusion

- The idea is that this standardized FMC signal pinout will be used for future EPIC ASIC test boards thus enabling:
  - a common standard even when connecting to various group-specific FPGA Evaluation Kits
  - connection of the ASIC test boards to the generalized EPIC ppRDO prototype
    - enables common logic for prototyping and later, for production
- My personal request (hope?) is that the new EICROC1 prototype board adheres to this FMC pinout standard so that we (FTOF, Far Forward etc) can quickly develop firmware and evaluate timing performance