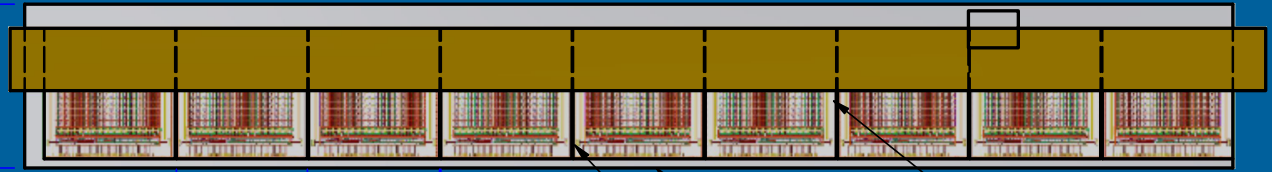


BIC - Astropix Module



Manoj Jadhav
Argonne National Laboratory

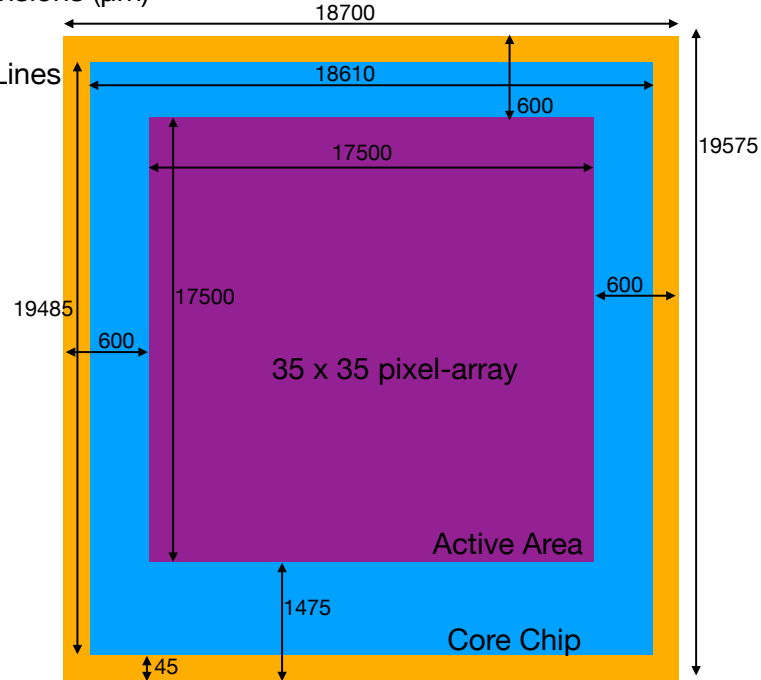
March 29, 2024

AstroPix

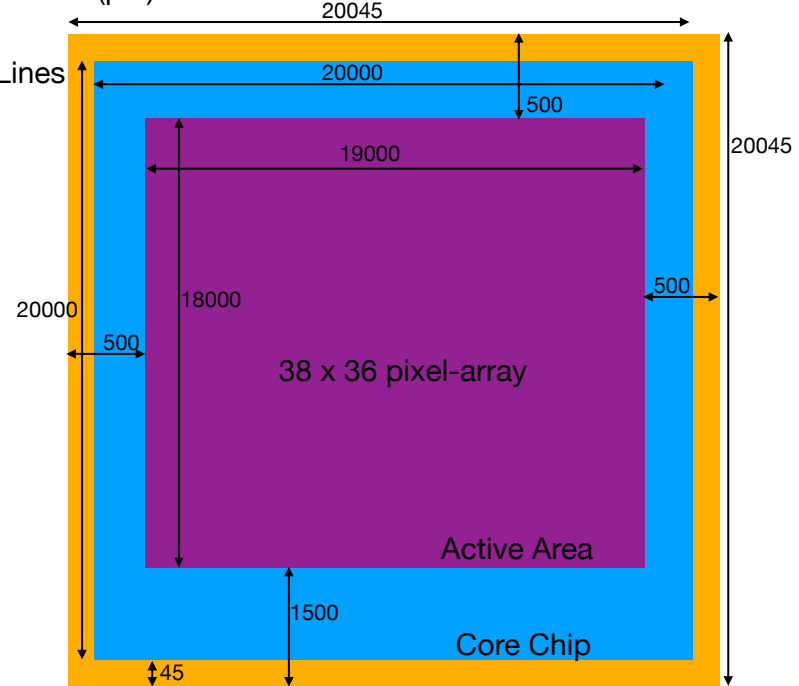
- Modules contain 9 AstroPix chips (2 cm x 2 cm)
- A total of 12 Modules per Stave → 108 chips → length of Stave is 218.16 cm
 - Provides full coverage
- The current AstroPix v3 size is (1.87 cm x 1.9575 cm)
 - AstroPix v5 to be a full-size chip (~2 cm x 2 cm)
- Ongoing discussion topics for the AstroPix Module
 - AstroPix chip
 - Total chip area, active area (2 cm x 2 cm)
 - Pixel to chip edge dead region (minimizing it to < 200um)
 - Power consumption (2 mW/cm²)
 - Bus bar design options (flex bus vs. Cable Harness)
 - Type of LDOs and Connector (right angle vs. vertical)

AstroPix

V3 Dimensions (μm)



V5 Dimensions (μm)



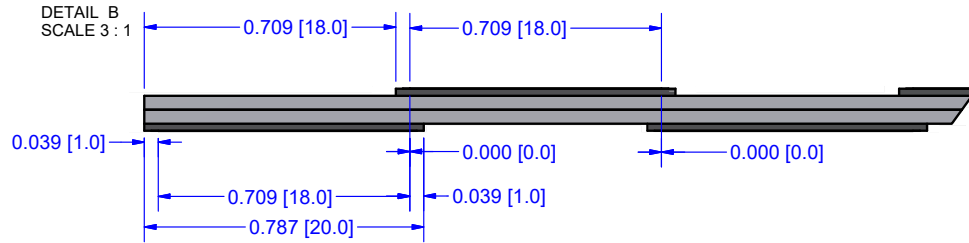
Nicolas said he is keeping 550 μm from pixel to chip edge for V5

AstroPix Power

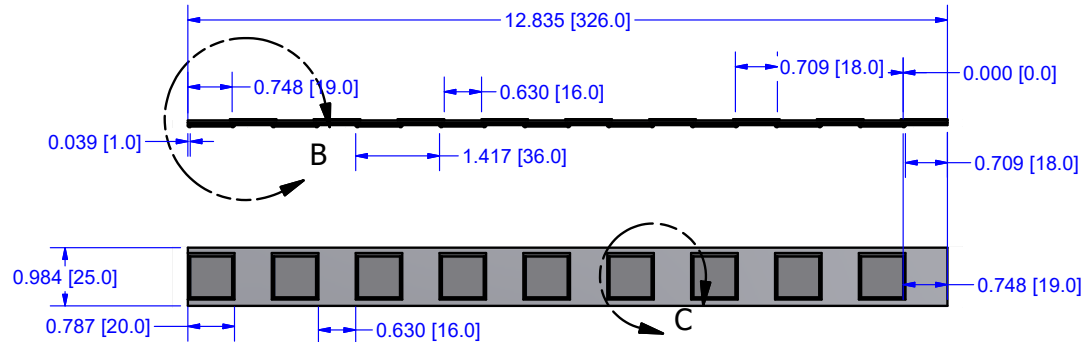
AstroPix v3	1.87cm x 1.95cm	3.66	cm ²			
	Per Chip			Per cm ²	Per Module	Per Stave
Supply	Voltage (V)	Current (mA)	Power (mW)	Power (mW/cm ²)	Power (mW)	Power (mW)
VDDA Analog	1.8	1.47	2.65	0.72	23.85	286.2
VSSA Analog	1.2	1.33	1.6	0.44	14.4	172.8
VDDD Digital	1.8	6.88	12.24	3.34	110.16	1321.92
		Total	16.49	4.5	148.41	1780.92
AstroPix v5	2cm x 2cm	4	cm ²			
(expected)	Per Chip				Per Module	Per Stave
Supply	Voltage (V)	Current (mA)	Power (mW)	Power (mW/cm ²)	Power (mW)	Power (mW)
VDDA Analog	1.8	2.4	4.32	1.08	38.88	466.56
VSSA Analog	1.2	0	0	0	0	0
VDDD Digital	1.8	1.67	3	0.75	27	324
		Total	7.32	1.83	65.88	790.56

*Analog power should be lower by $\sim 0.2\text{mW/cm}^2$ from the ampout buffer. Ways to optimize digital power too.

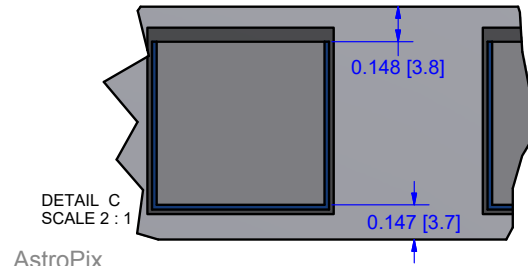
AstroPix Module Designs



We are going back to the initial Module design by reducing the dead area around the pixel array!



Kevin Bailey
Medium Energy Group
Physics Division
Bldg 203 F-126
Argonne National Laboratory
9700 S Cass Ave
Argonne, IL 60439
630-252-4036
Telecommuting - Cell 630-776-5737

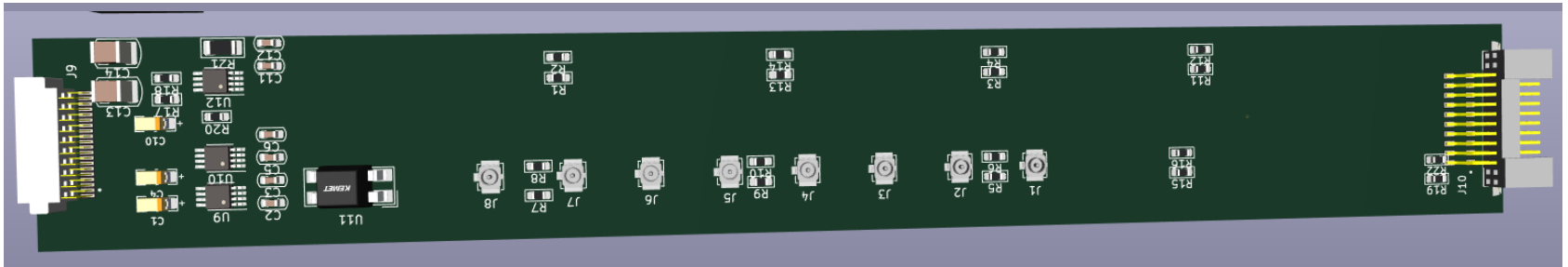
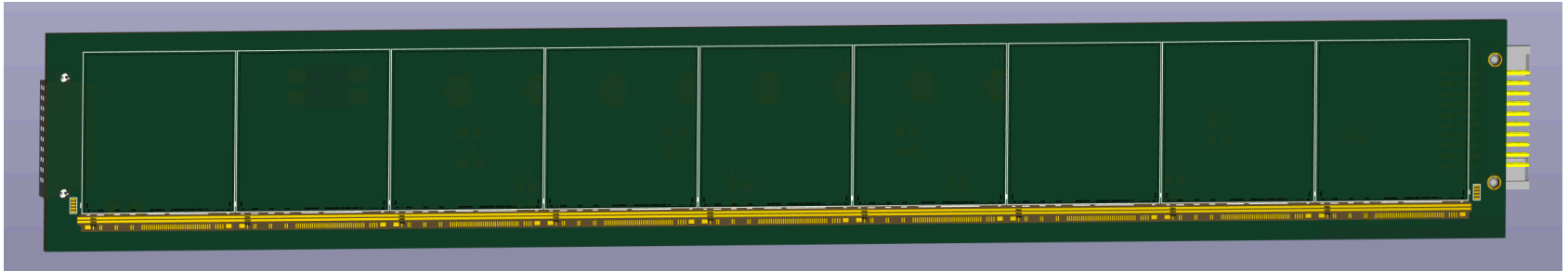


AstroPix Module Connector & LDO options

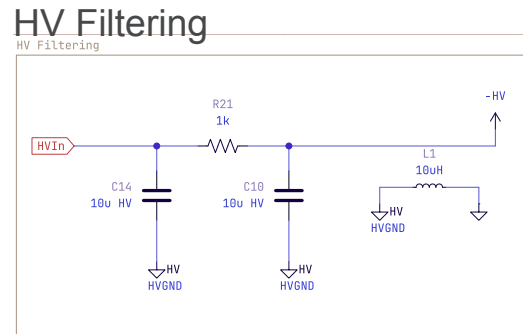
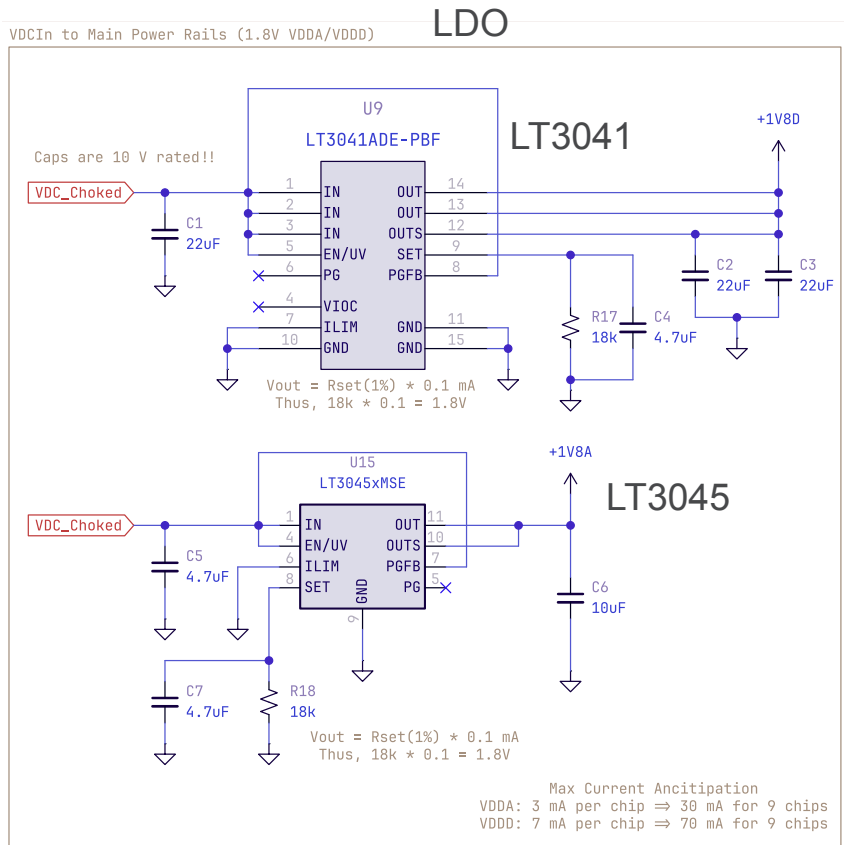
- Connector for Flex bus to Carrier PCB
 - Vertical vs. Horizontal Connectors
 - Flexible connector with cable harness instead of flex bus
- The connector between two Modules
 - Right angle connector
- Connector Suggestions
 - BTH, ERM8, ERM8_RA, LSHM_DA, LSHM_DV (Steven)
 - SFMH-110-02-L-D-LC, FSH-110-04-L-DH-SL (Taylor)
- Options for LDO
 - LT3041, LT3097, LT3045 (Steven)
 - LT3080 (Taylor)

AstroPix Module PCB test design

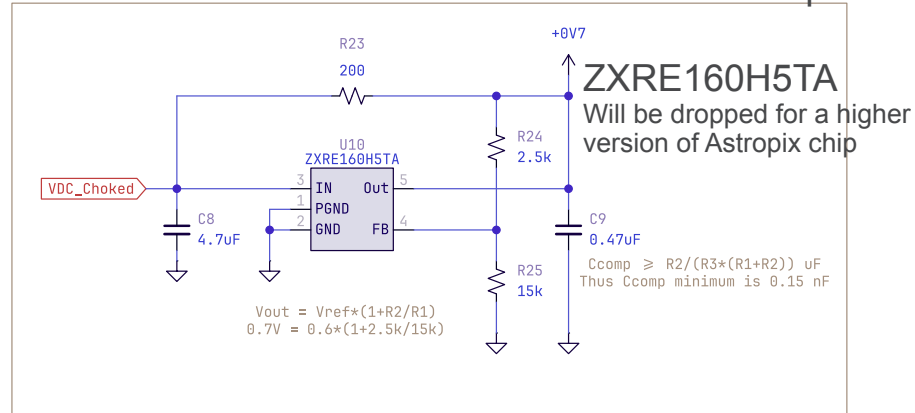
- PCB test Module
 - Similar to the AstroPix Module to test working
 - Additional space for wire bonds, connectors, more I/O lines



AstroPix Module PCB test design



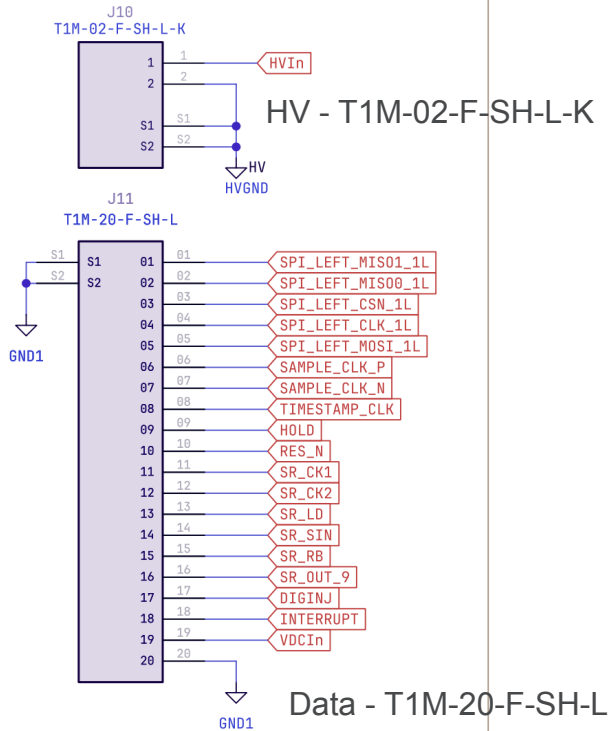
Shunt Regulator for Vssminpix (0.7V) Input (Astropix V3 Only) LDO - vminuspix



AstroPix Module PCB test design

Samtec 20pin Connector Left

Connectors



SR_* lines, DigInj, Interrupt, will be removed later.

List of I/O		
	V3	V5 (Not Final - need in)
Power	HVIn	HVIn
	HV GND	HV GND
	VDCIN	VDCIN
SPI	MISO0	MISO0
	MISO1	MISO1
	CSN	CSN
	CLK	CLK
Sample Clk	MOSI	MOSI
	SAMPLE_CLK_P	SAMPLE_CLK_P
	SAMPLE_CLK_N	SAMPLE_CLK_N
Shift Register	SR_Ck1	
	SR_Ck2	
	SR_LD	
	SR_SIN	
	SR_RB	
	SR_OUT	
Other	DIGINJ	
	INTERRUPT	
	TIMESTAMP_CLK	TIMESTAMP_CLK
	Hold	
	RES_N	

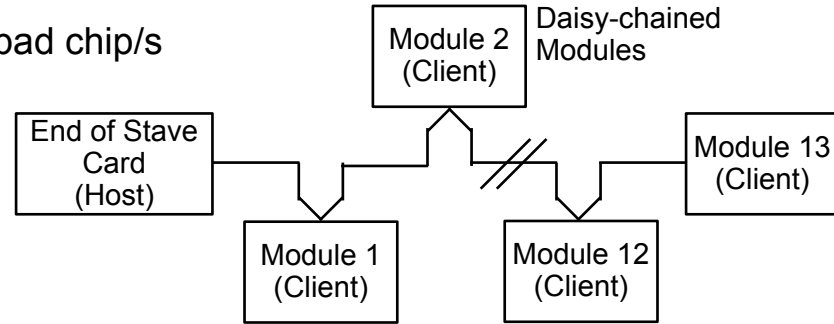
Summary

- Module Design
 - Two main options - Option 2 (vertical connector) & Option 3 (flex attach for Module to Module)
 - Differential SPI, Multi-drop data transmission
 - Check risk factors for SPI failure
 - First test version - PCB test Module
- Connectors
 - Different options are available
 - Can we select a few options for each type - right angle and vertical?
- LDOs
 - Few options available - [LT3041](#), [LT3045](#) for first iteration of Module PCB
- Sector Integrations
 - Check for available space
 - Stave integration on the Tray

Thank you

AstroPix Module Data Transmission

- Are we daisy-chaining the entire stave?
 - Not preferred option
 - Risk of losing an entire row due to a single/few bad chip/s
 - Flex bus alignment might be an issue
- What are our options?
 - Differential SPI (KIT confirmed - ePIC meeting)
 - Multi-drop data transmission using flex bus
 - Daisy-chained chips on the module will be parallel to chips on other modules.
 - Master End-of-Stave will connect to slave Modules through daisy-chain (LVDS on Modules)
- Module enable control
 - Allows to control Module operation individually
 - This will allow to save stave by switching off bad Module



AstroPix Module Block Diagram

