

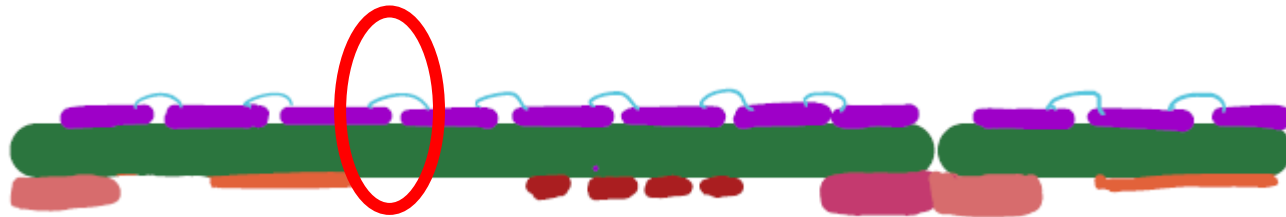
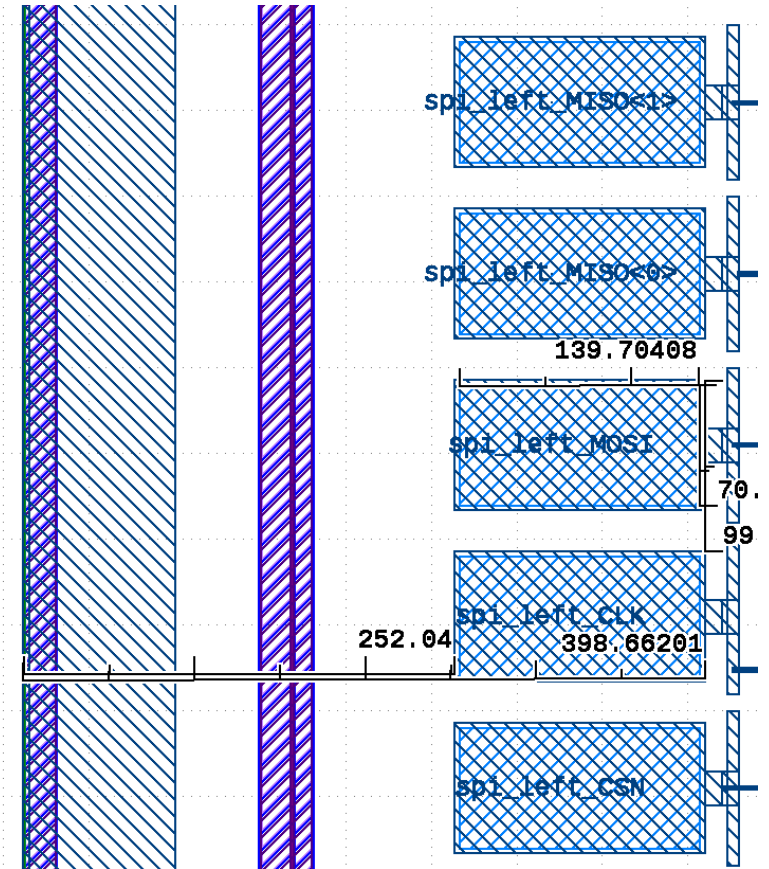
# Bonding distances in Astropix V3, V4

A follow-up from March 1<sup>st</sup> meeting:  
checking on the bonding dimensions

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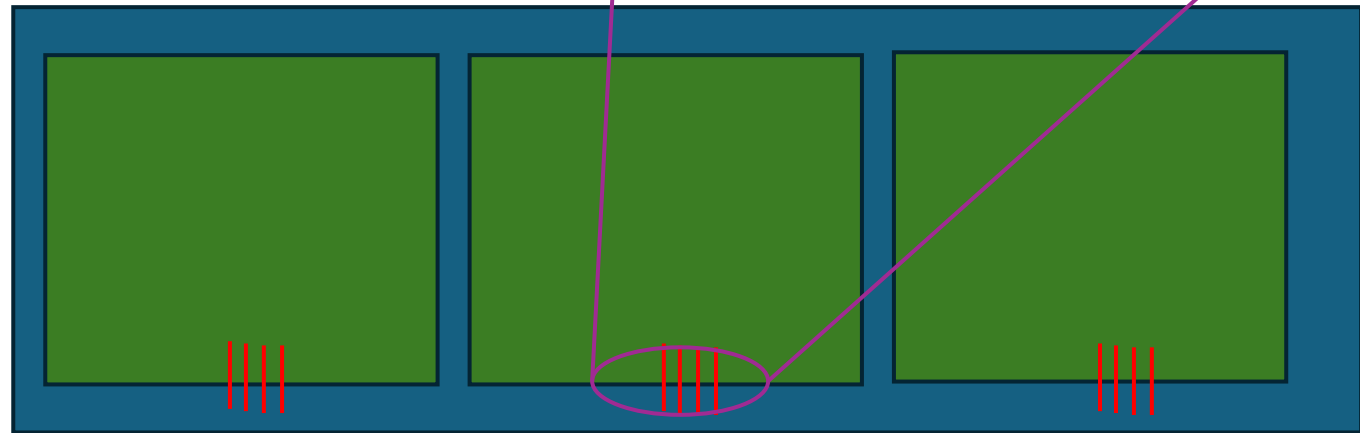
# Chip-to-chip connections (SPI)

- 5 pads with pitch of 100  $\mu\text{m}$  for V4
  - 6 pads for V3, with additional “sample\_clock\_left/right”
- Pad area is  $70 \times 140 \mu\text{m}^2$
- Distance between the edge and pad center is  $275 \mu\text{m}$
- Same dimensions for both chip edges
- $\rightarrow$  The dimensions look ok for bonding:
  - $275 \mu\text{m} + 275 \mu\text{m} + 50 \mu\text{m} (?) = 600 \mu\text{m} > 500 \mu\text{m}$



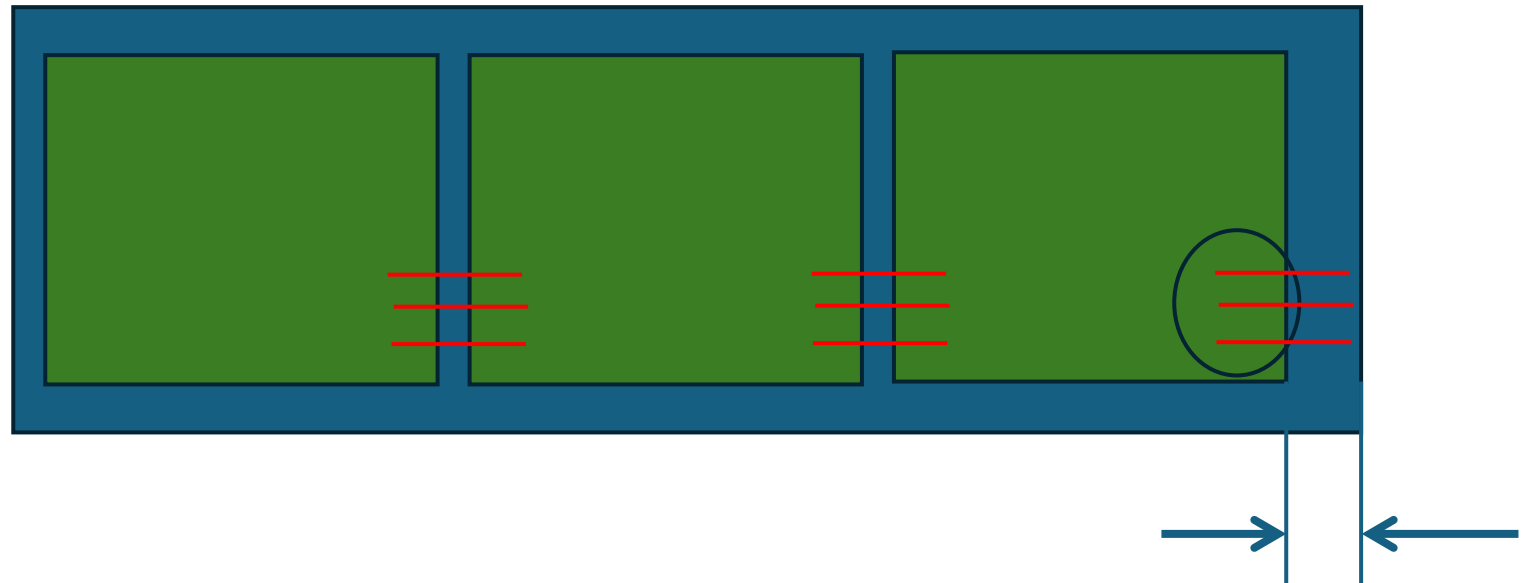
# Chip-to-PCB bonding (1)

- The (numerous) bonds on another edge have the same dimensions and distance to edge.
- Will need the PCB margin, but it's available in this direction.



# Chip-to-PCB bonding (2)

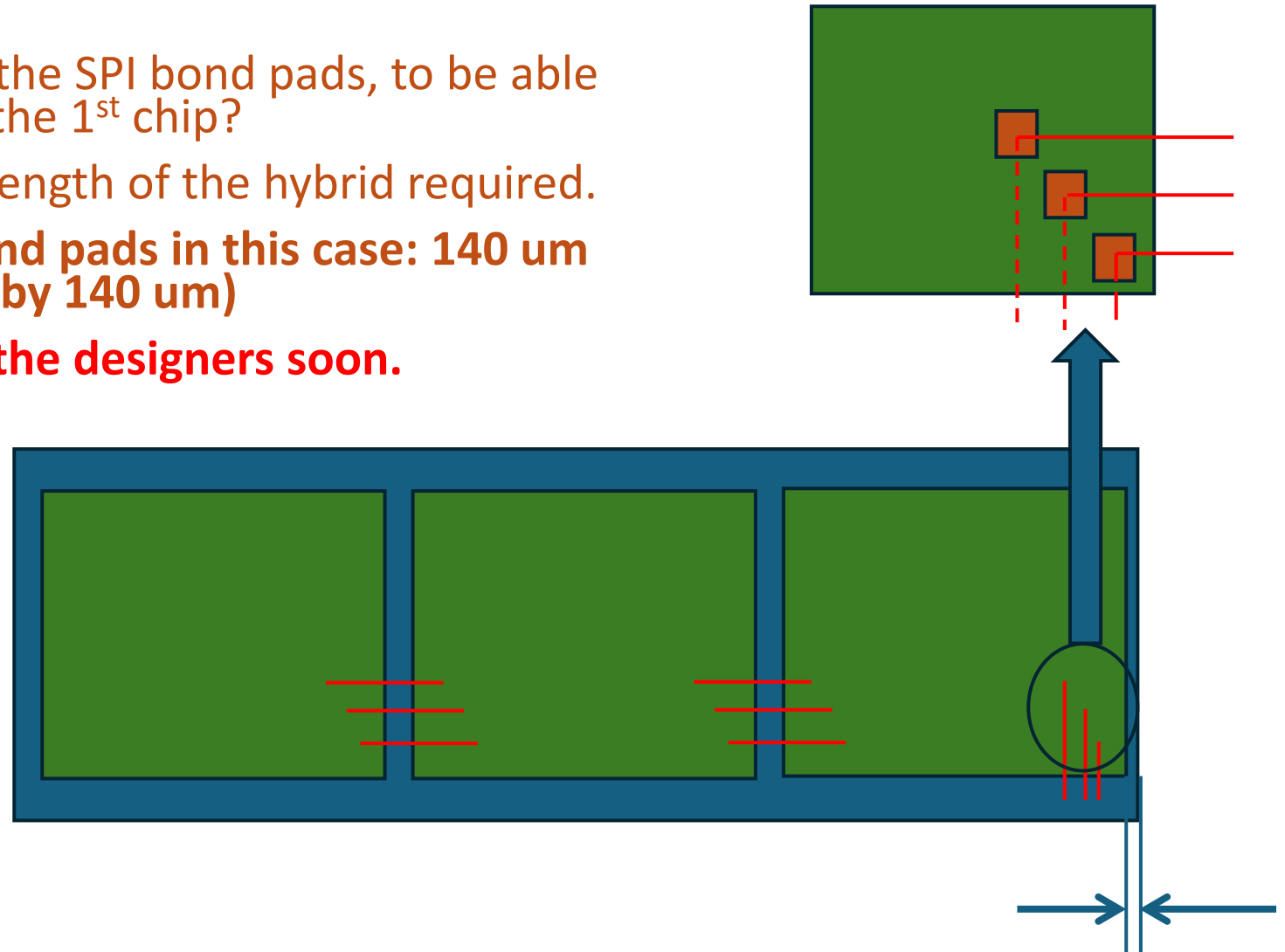
- For the existing chips (V3, V4) would have to allow the necessary distance/margin on the PCB at the end, due to the space needed for the bonds.
- Would prefer ~800 um between the chip edge and the bondpad center.



Undesirable gap in  
active area coverage

# Chip-to-PCB bonding (3)

- For V5: Would like to stagger the SPI bond pads, to be able to bond to the other side for the 1<sup>st</sup> chip?
- This would allow to limit the length of the hybrid required.
- **Would want to widen the bond pads in this case: 140 um by 140 um (instead of 70 um by 140 um)**
- **If in agreement, need to ask the designers soon.**

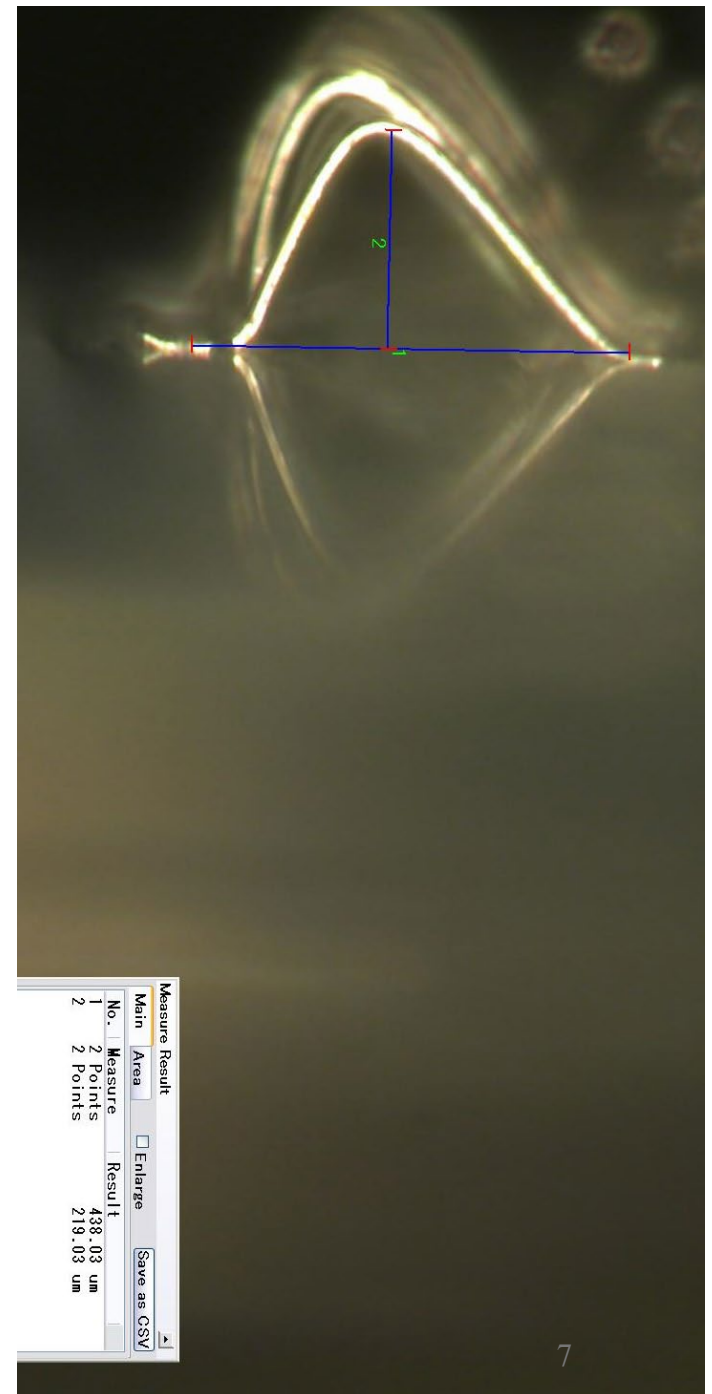
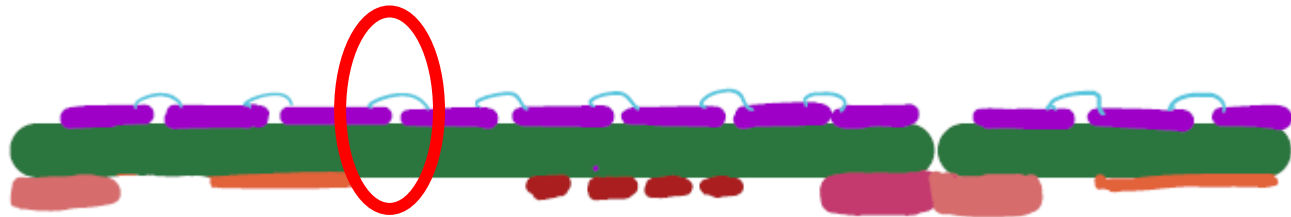


Less gap in  
active area coverage

# Backup

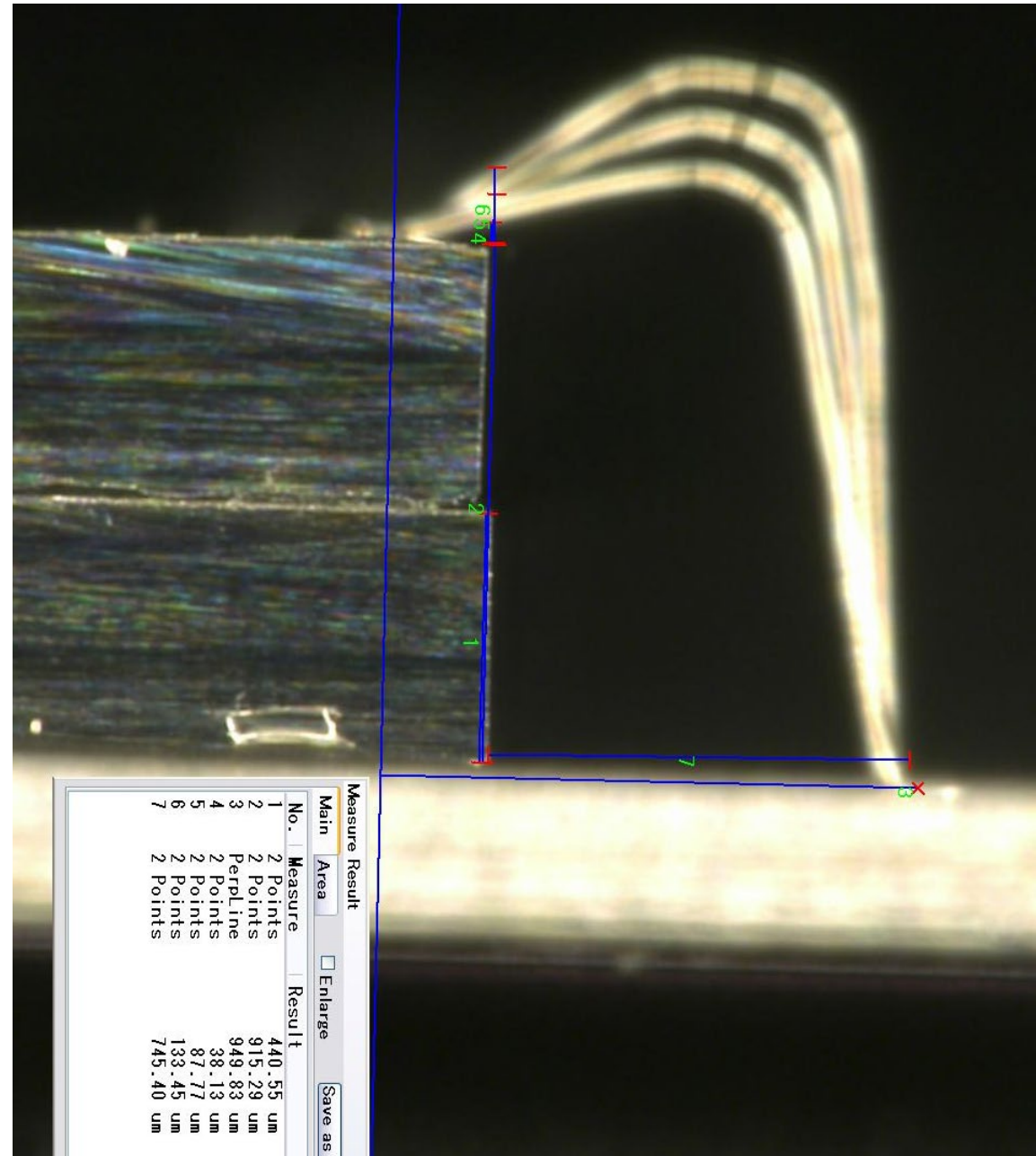
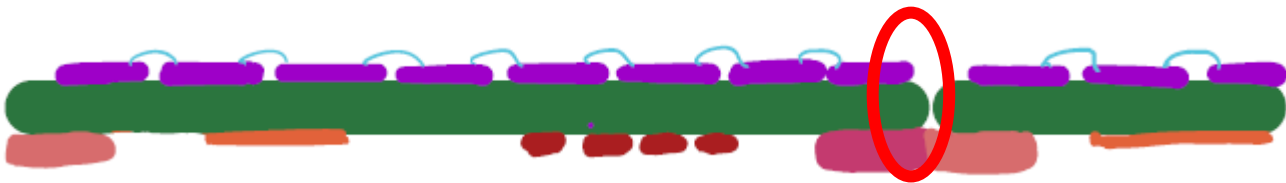
# Checking on the bonding distances/constraints: chip-to-chip

- Have to have a bond height at the chip edge (which is at HV!)
- Assuming x2 safety factor and  $\max(\text{HV}) = 400 \text{ V}$ , would need 266  $\mu\text{m}$  loop height.
- $\rightarrow > \sim 500 \mu\text{m}$  pad pitch distance for the same height.
- Is this the case for V4/5 chips?



# Chip-to-PCB bonding

- Still need the loop height (HV)
- Cannot get too close to the chip edge without making unreliable bond due to kinks at **both** source and destination locations.
  - Note the horizontal distance limits the max loop height to avoid “vertical” portion of the wire and a large part of the wire pressing against the bonding wedge.
- Would prefer ~1 mm. This is probably too much.





# Chip-to-PCB bonding (2)

- An extreme case – got very close, but:
  - Wire against the wedge, kinks.
  - Limitations on the wire pitch (due to the wedge width)

