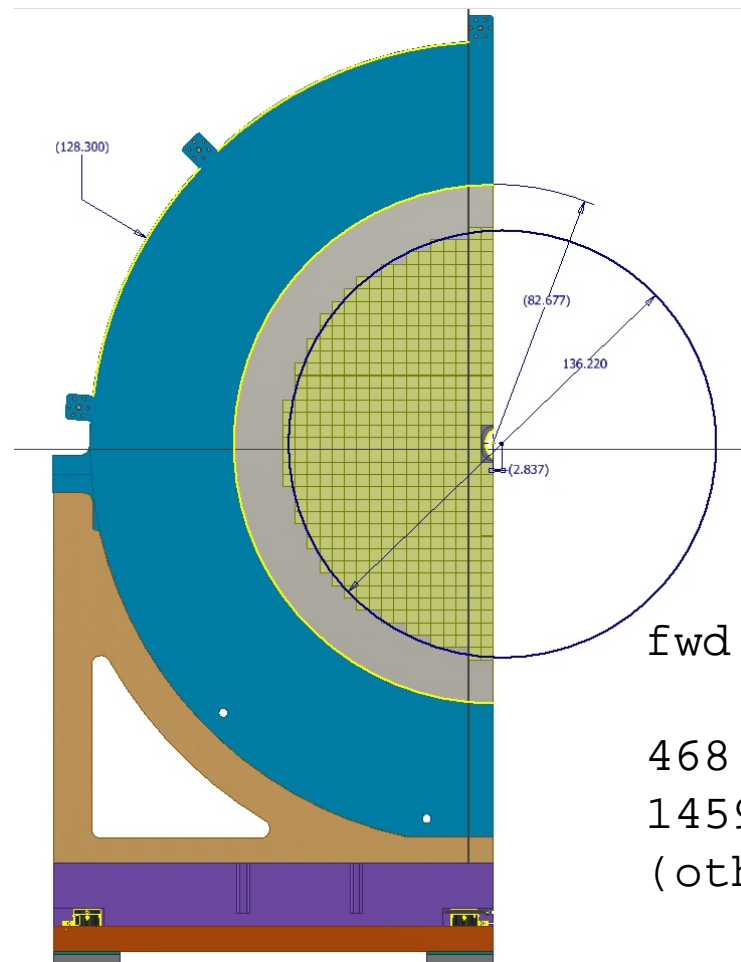


eRD109 COTS Waveform Readout FEB – update Apr. 4 2024

Slide 2 details added after meeting

G. Visser, Indiana University

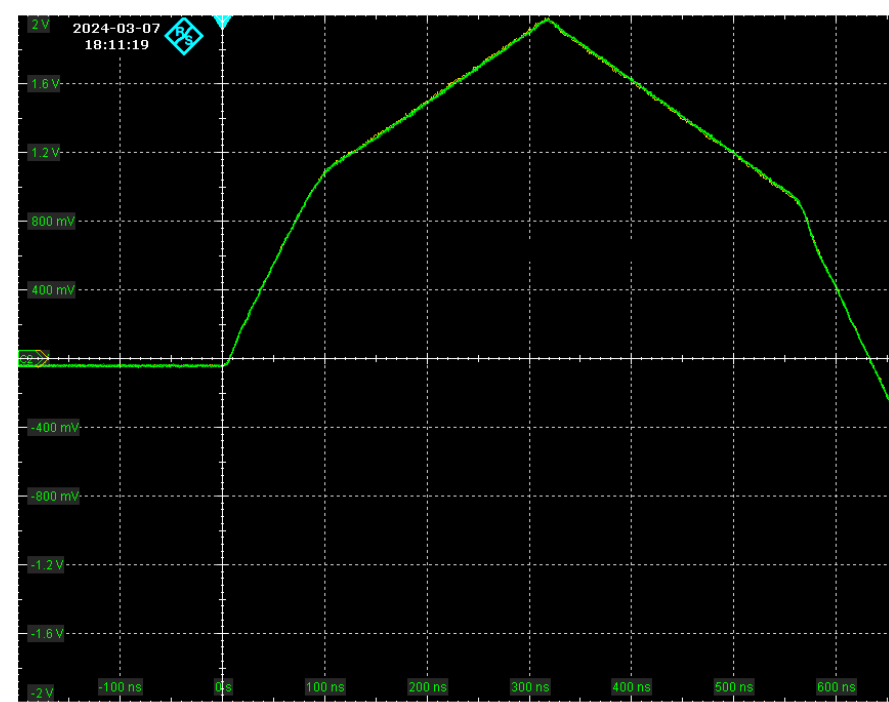


fwd ECAL:

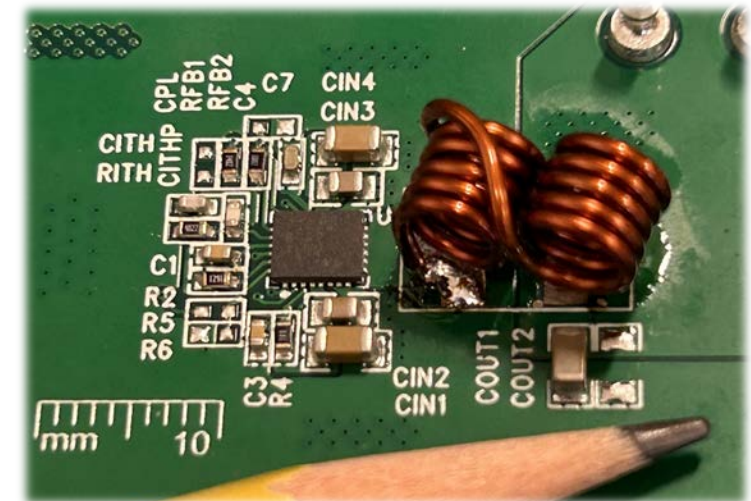
468 FEB (14976 channels)
14592 channels really used
(others masked)

Progress 3/7 – 4/4

- Tested “dynamic range compressor” – works although some difficulties with faster pulses (not unexpected). Shelved for now, better avoid the circuit complexity. It seems not needed (14 bit linear range is enough).
- Started on revision of SiPM bias circuits from STAR FCS for fwd ECAL application
 - SiPM bias plans presented in more detail 3/14 Electronics & DAQ meeting
- Further DC/DC converter testing (LTC7151 with dual solenoid inductor), 15 A. Measured >80 % efficiency at up to 20 V in (1.2 V out).
 - Not for baseline FEB (on-board 1.5 A DC/DC) but it’s a possible alternative plan with a separate power board, and perhaps useful for other ePIC applications
- 98% completed fwd ECAL SiPM board design (see next slide)
- A little further progress on FEB PCB design
- Working to demonstrate shorter shaped pulse (73 ns) to reduce dark counts and fluctuations in pulse while maintaining resolution in integral by summation



Compressed output w/ full scale triangular input pulse

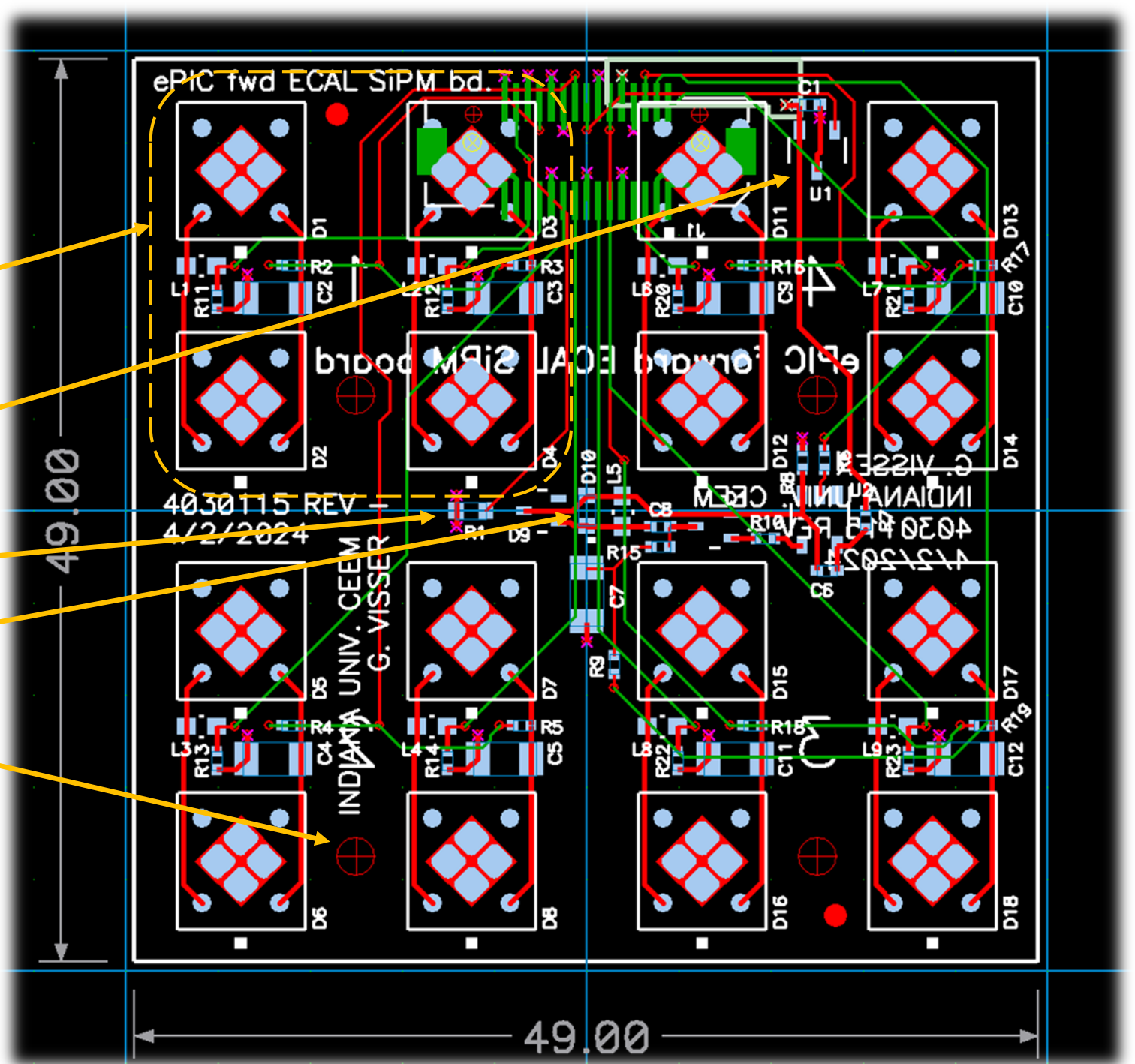


LTC7151 air-core 1.2 V 15 A test

Fwd ECAL SiPM Board aka "Adapter"

Connector: JAE # AX01R030VABB
mating on FEB # AX01F030VABB

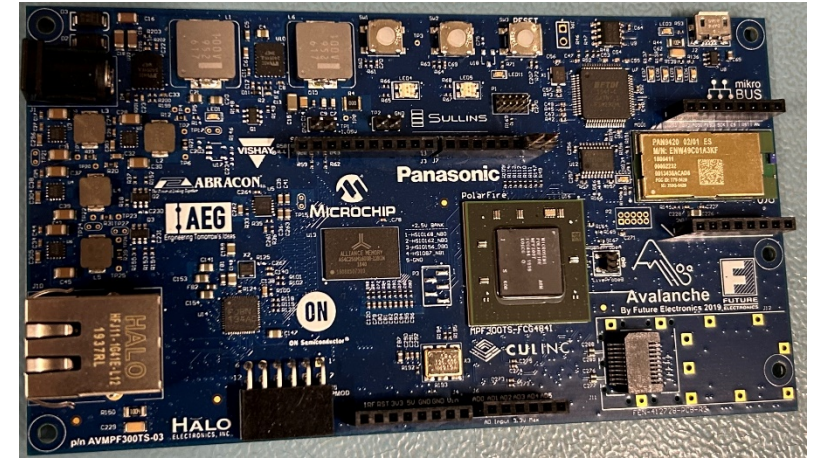
- 4 towers, 2x2 of 6x6 mm² SiPM's each
Hamamatsu # S14160-6015PS
- frontend in groups of 2 SiPM's for faster pulse (for DCR mitigation)
- serial number IC
AD/Dallas # DS2411R
- thermistor (as in FCS)
Vishay # NTC50603E3103FHT
- LED pulser (similar to FCS)
LED: Bivar # SM0603UV-400, same as in SPHENIX
- gluing alignment holes
 - also serve as broken board removal handle holes



There's some fab documentation details to do, then RFQ & get prototypes built

eRD109 status/plans

- Specifications/requirements documented
 - (Still) seems like close to finalizing rate requirements, good enough
- FEB-detector integration: basically all finalized at this point
- Key parts procured: ADC, FPGA, DC/DC, preamp
 - Including more FPGA dedicated to bwd ECAL application
- Learning PolarFire FPGA details; *need to pick this up again...*
- **SiPM board design completed**
- Lightguide improvements (→ Required for FEB mechanical, and possible light yield improvements are of the greatest importance for readout – min signal size challenge!)
- LTC3600 DC/DC circuits with air-core inductor – low noise proto needed
- SiPM frontend prototyped / improved from STAR FCS → real FEB layout in progress
- Working to define FEB-RDO interface
 - Expect to make simple FMC board to interface to ppRDO (Tonko)
- **Next steps / in-progress**
 - **Two channel signal path prototype to fit to PolarFire eval board**
 - **Build SiPM board prototypes**
 - FEB Main Board layout & produce prototypes
 - Considerations for application to bwd ECAL
- Other to-do:
 - **Radiation testing**



PolarFire Eval Board – nice/simple/\$200

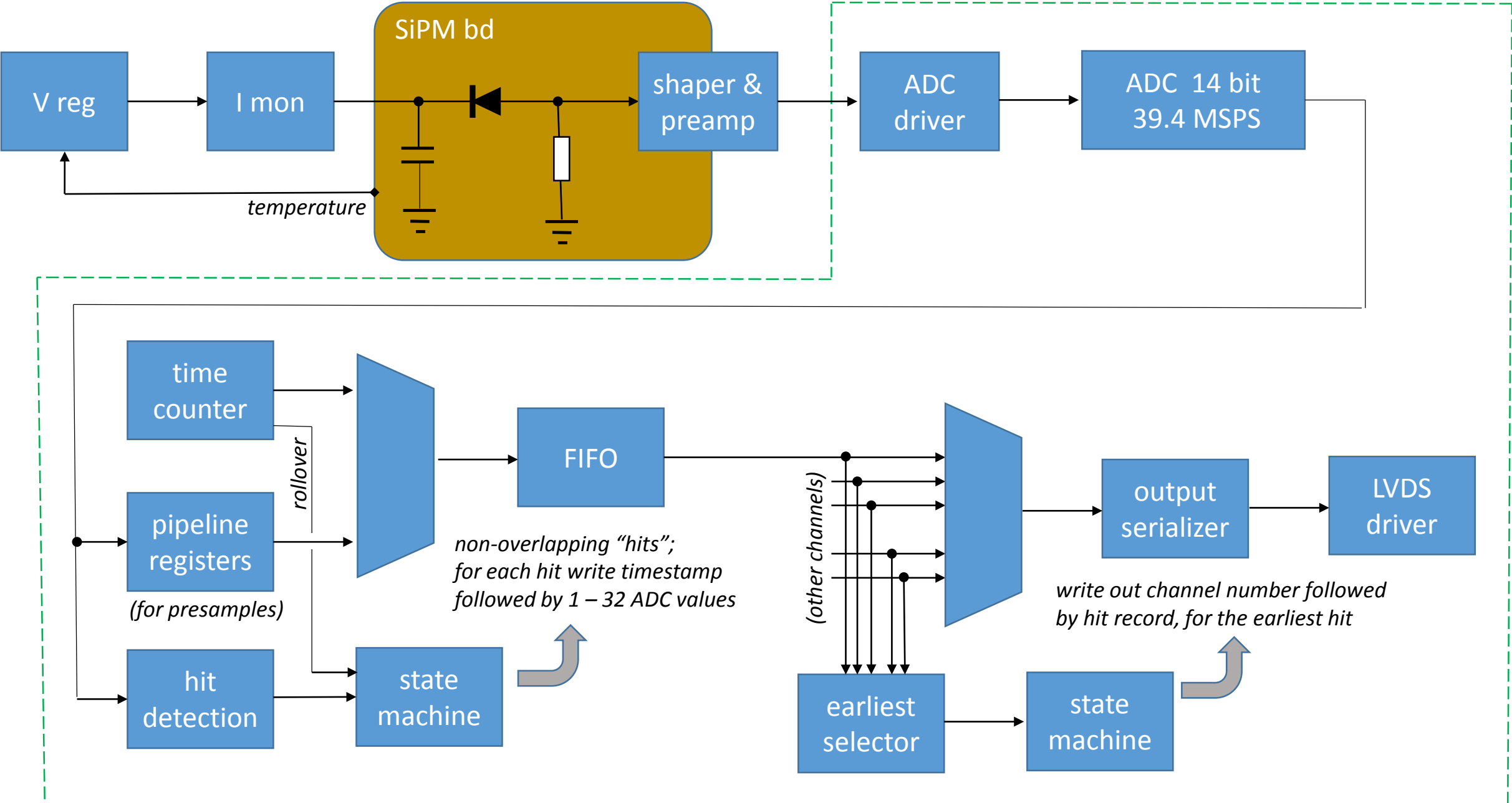
I've deviated somewhat from the sequence of milestones in contract. Trying to do always what is best to push forward the design.

So far have not really tackled comparisons to HGCROC nor waveform ASIC possibilities. These will be done, but I think the first emphasis has to be on design.

On the other hand, have put early effort into possible application to bwd ECAL.

backup slides

Block diagram



FEB & SiPM carrier mechanical cartoons (dimensioned sketches will be made later)

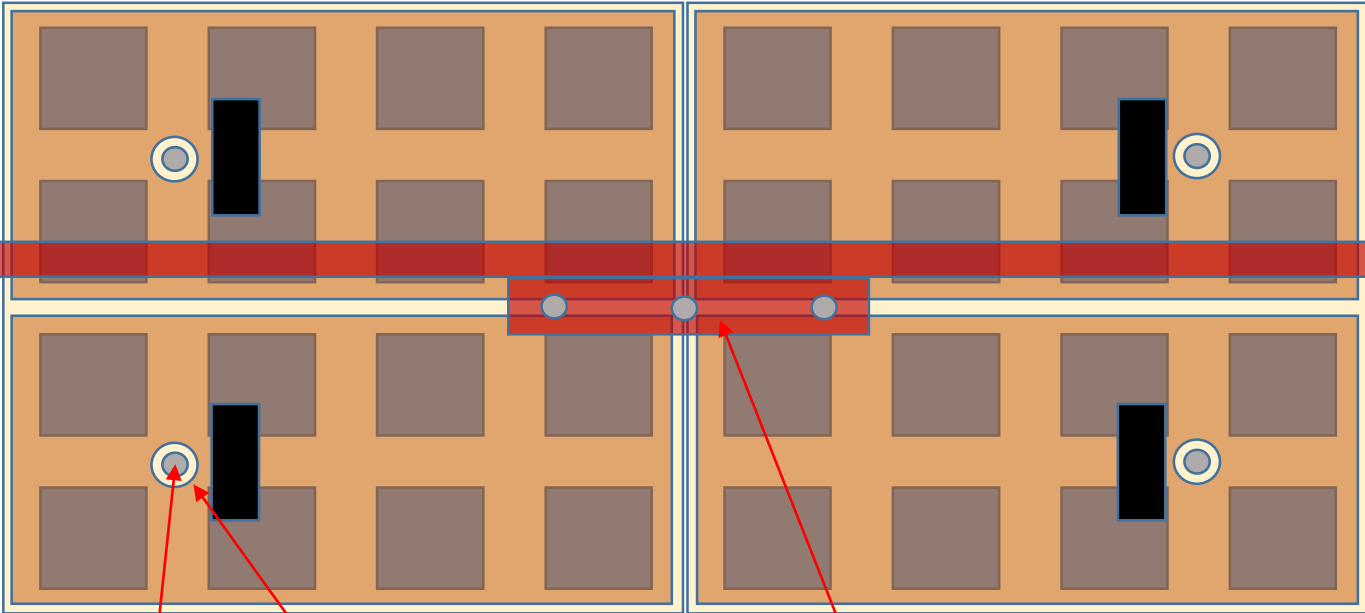
2-block (32 tower) FEB

(forced) air cooling option now ruled out, too difficult to integrate

This was sketched with old lightguide (one pyramid per tower). This is out of date (see Oleg's presentation). No impact on FEB, so for simplicity (or laziness) I'm not updating it here.

actually also the SiPM board & connector scheme is changed

FEB not shown (in this view only)
(but see next page)



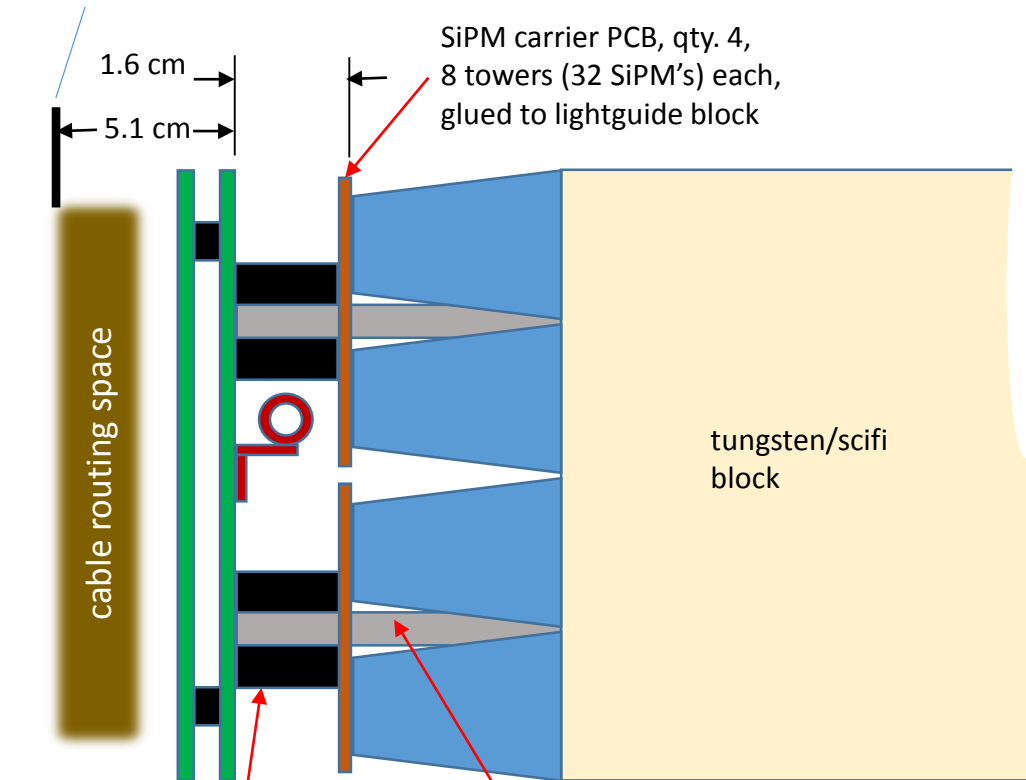
standoff clearance hole through SiPM carrier PCB

6 or 7 4-40 pan head screws to attach FEB on 4 standoffs and 2 or 3 thermal tab nuts

water tubing connection to FEB is also an electrical ground for FEB (important for noise/EMI and safety)

cooling water tubing & small "tab" to PCB
0.19" OD, 0.13" ID
copper "refrigeration tubing"
no fittings inside detector

Integration limit (new)



SiPM carrier PCB, qty. 4, 8 towers (32 SiPM's) each, glued to lightguide block

tungsten/scifi block

4x aluminum 3/16" hex 4-40 standoffs to LG, support FEB independent of SiPM boards

FEB PCB stack
2 - 3 PCB's

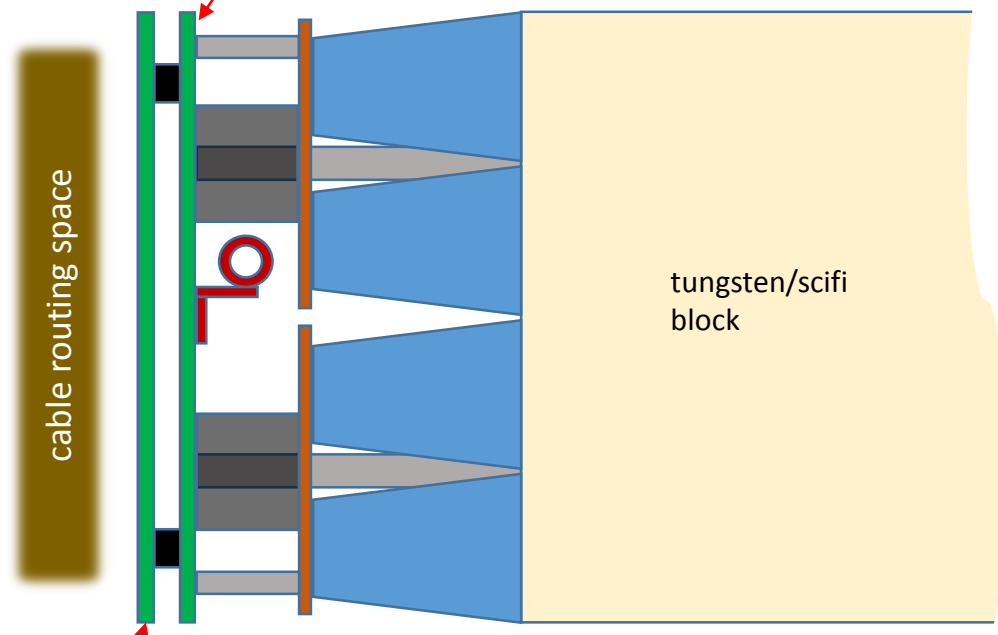
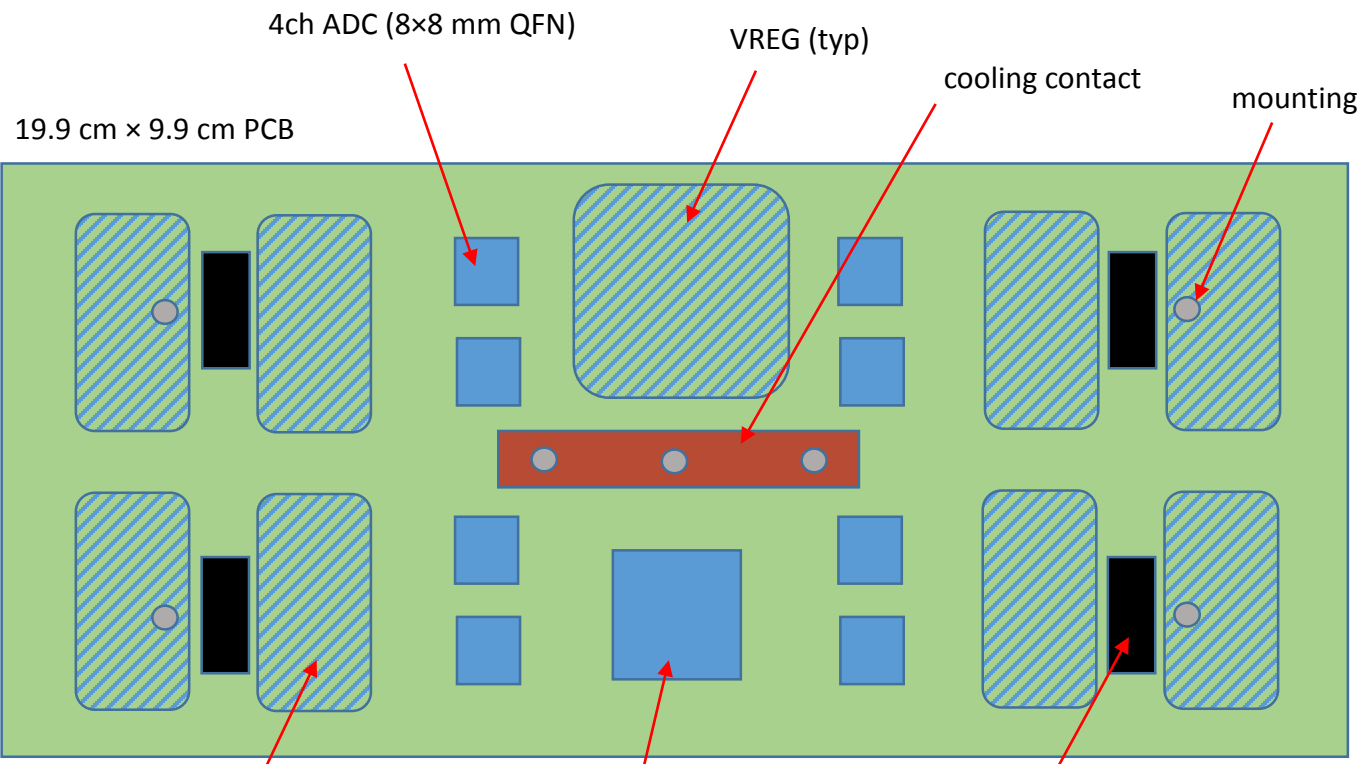
floating connectors, 1 per SiPM carrier
JAE AX01 series (30 pos) or similar



prototype FEB mounting standoff

all cables and water tubing route basically *only horizontally* on detector

rear view of inner FEB PCB



4x amplifier/shaper
(4 places)

FPGA (17x17mm BGA)

floating connectors
JAE AX01 series (30 pos) or similar
(8 places)

outer FEB PCB(s)
(bias voltage regulators & current monitors,
cable interface circuits and connectors,
misc. lower power stuff)

tungsten/scifi
block

