eRD109 progress report
dRICH RDO design @INFN Bologna

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but… a lot of other people contributing in Bologna and also from INFN-TO (F. Cossio, M. Mignone G. Dellacasa) and INFN-FE (R. Malaguti). Truly a joint project!

Update on dRICH RDO design (March activity)

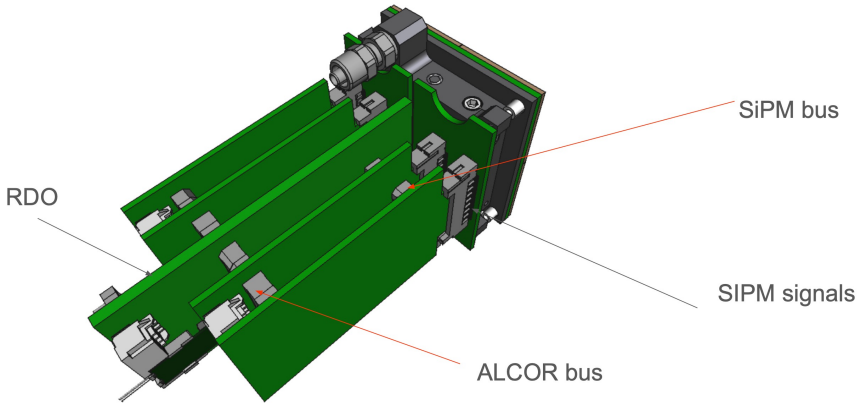
- challenging constraints on dimensions for dRICH (4x9 cm)
- design for schematics/selection of components **in advanced progress**
- pinout further studied (definition of I2C branches, etc.)
- delivered 10 AU15P (Artix)
- ordered 10 MPF050T (PolarFire)

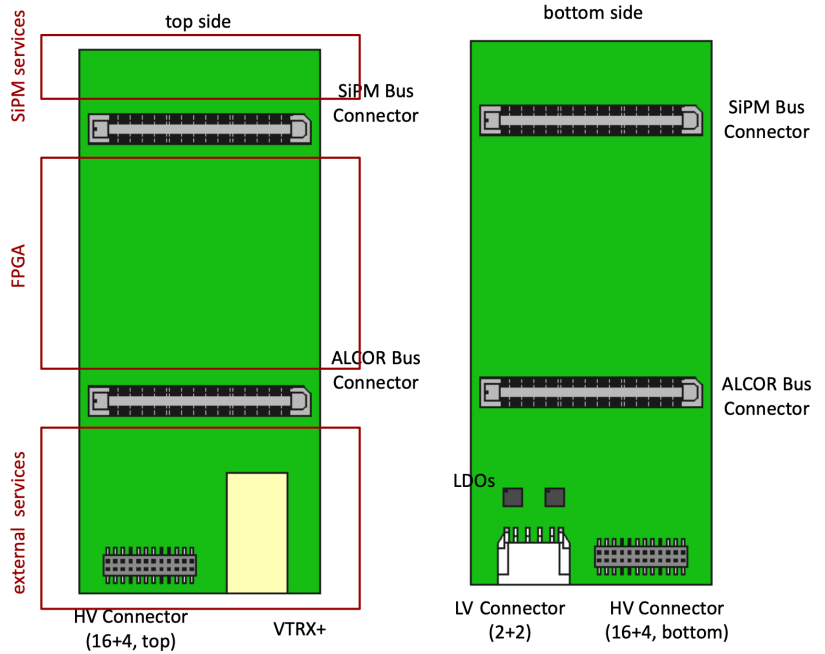
Current components candidates:

- Main FPGA: Xilinx AU15P-SBVB484
- Opt. tranc. VTRx+
- Scrubber FPGA: Microchip MPF050T-FCS9325
- QSPI Flash: MT25QU01
- Samtec connectors (SiPM bus: ERF5-020-05.0-L-DV-TR and AlcorBus: ERF5-050-05.0-L-DV-K-T)
- Clock multiplier/jitter cleaner: SkyWorks SI5326 + additional crystal at 11
- T sensor: TMP119AIYBGR (close to LDOs and VTRX+)
- 1 MCU: ATtiny 416
- LDOs and current monitor: LTM4709 + LTC3203
- I2C I/O expander: Microchip MCP23017
- ADC for NTC sensors on SiPM carrier: ADS1219IRTER

Report highlights on:

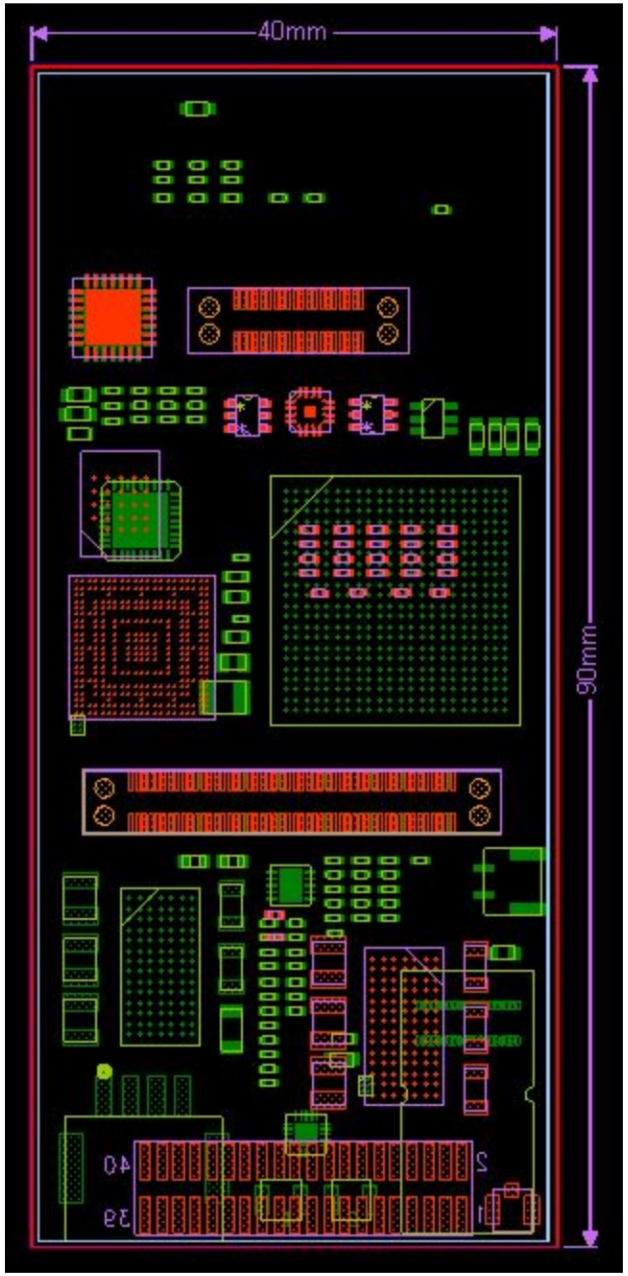
- design progress (pre-placement)
- design about remote programming
- NTC sensors





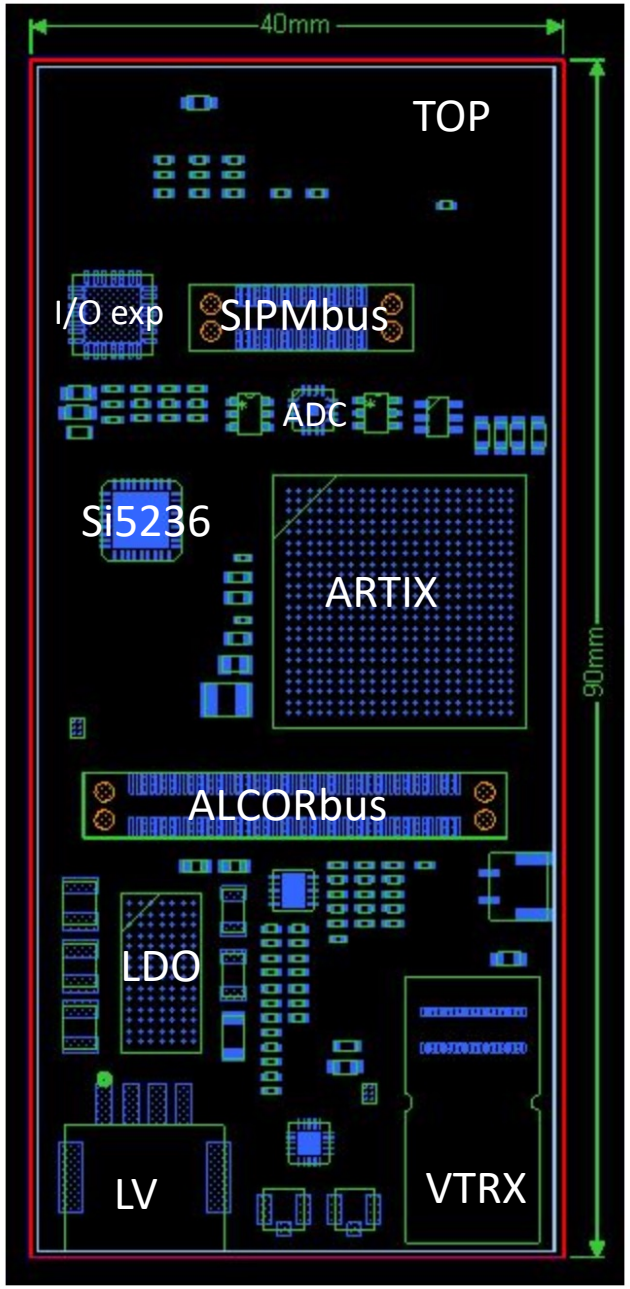
Application to TIFPA PAC for access to proton in Trento for irradiation of components in July and December (ALCOR and FPGA) **accepted**

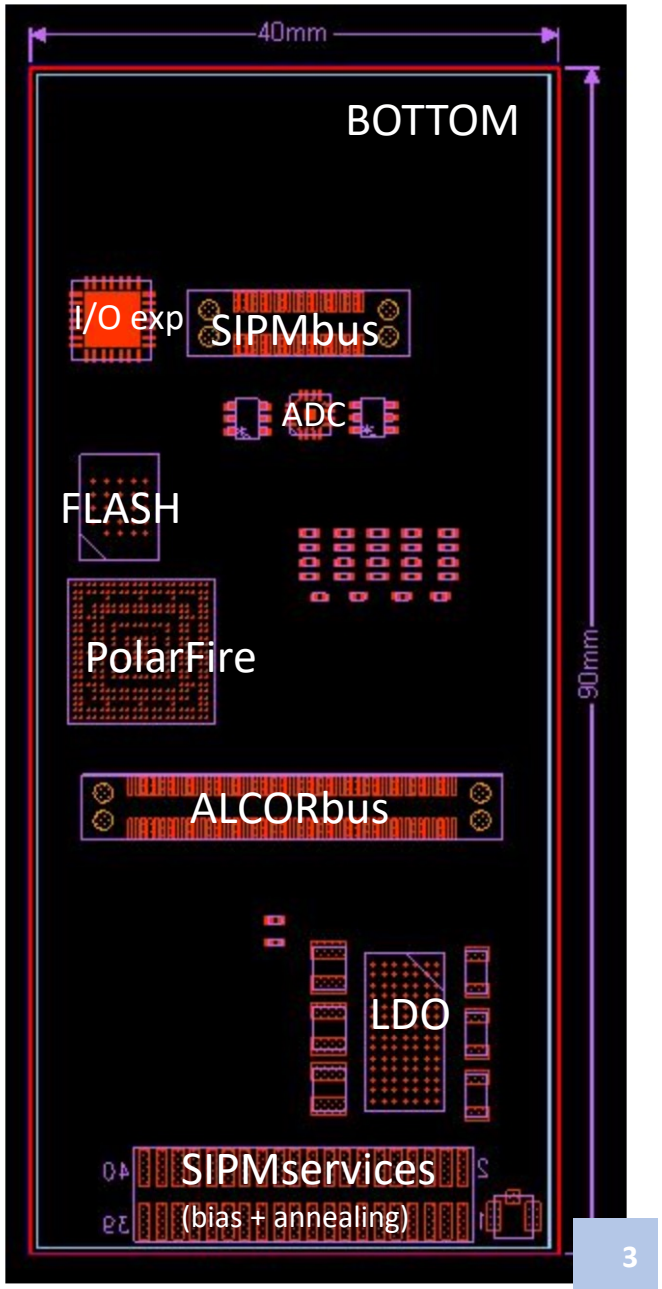
Design progresses



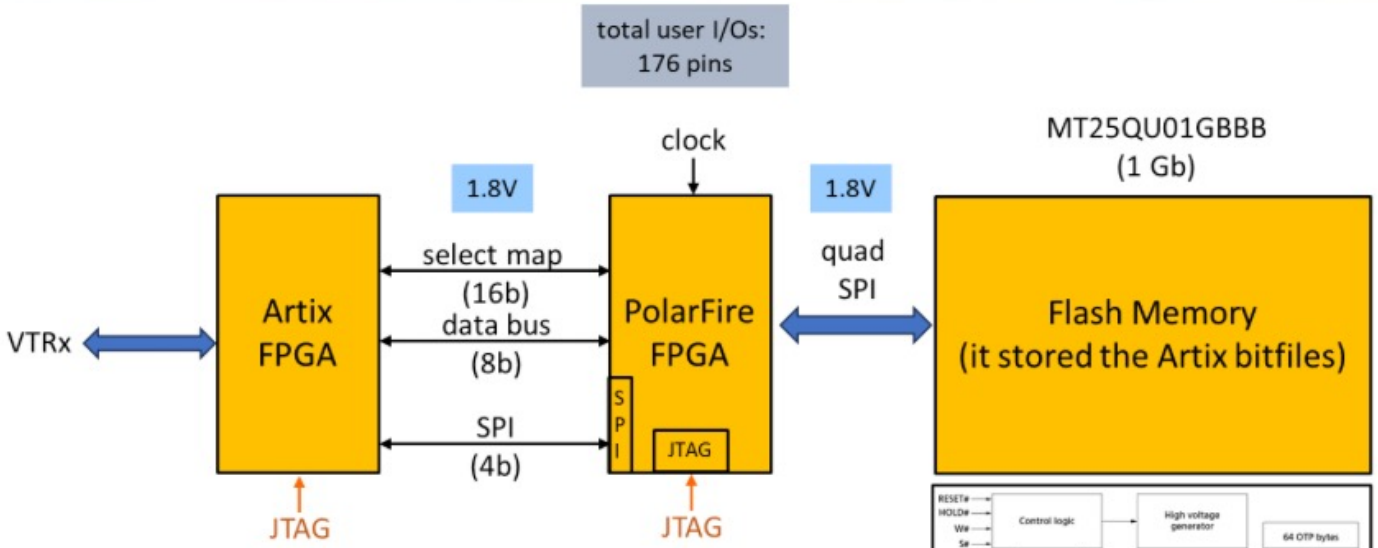
Space seems ok!

Still some margins of maneuvering, but still some components to be added!



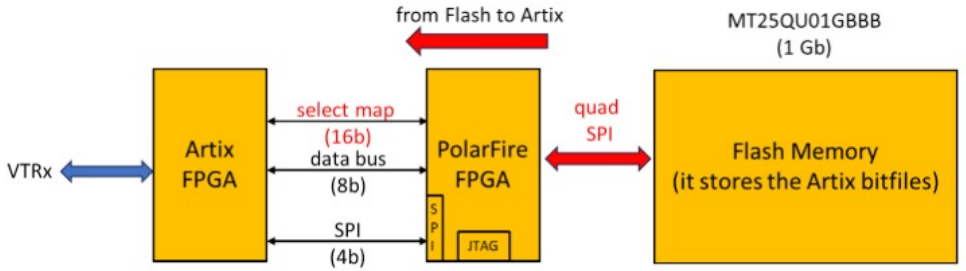


FPGAs - FLASH memory configuration scheme

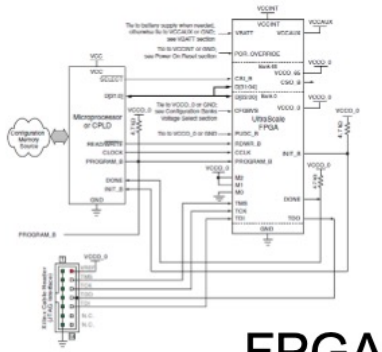


FPGAs - Artix programming from Flash

Step 1: Artix Ultrascale+ programming from Flash

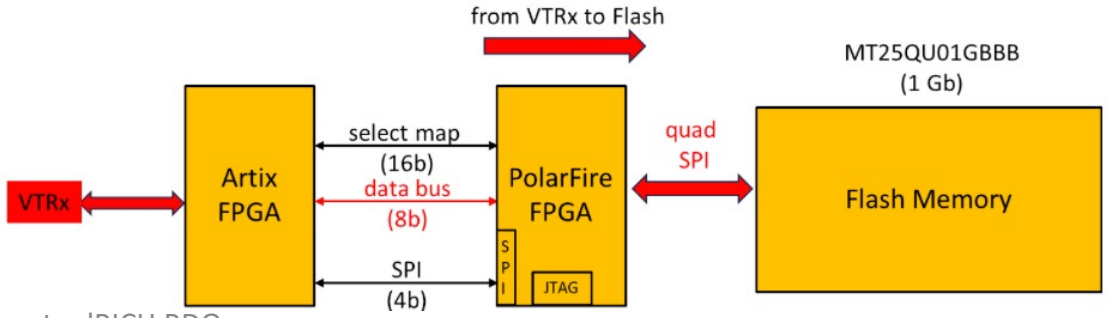


from Xilinx ug570

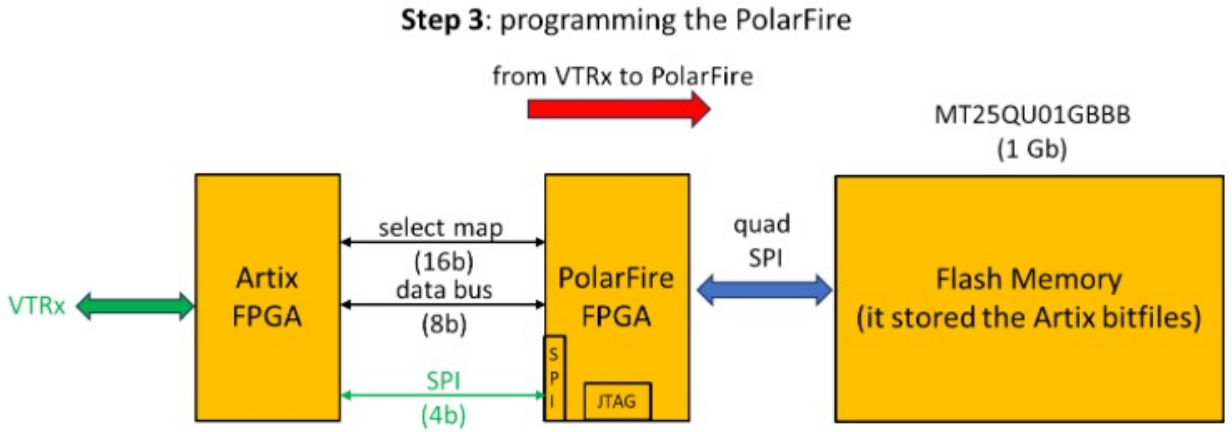


FPGAs - FLASH programming

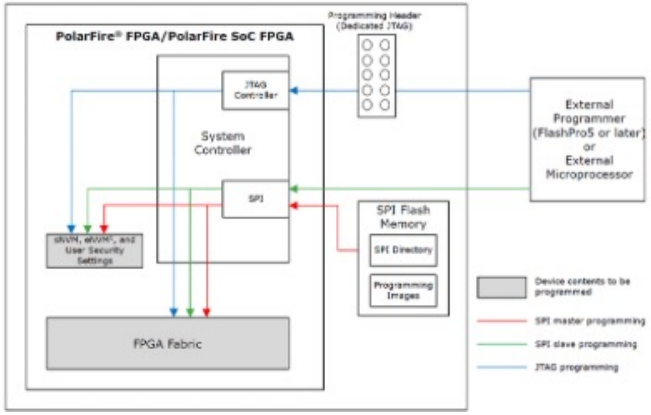
Step 2: programming the Flash memory



FPGAs - Polarfire remote programming



from "PolarFire and PolarFire SoC FPGA programming User guide"



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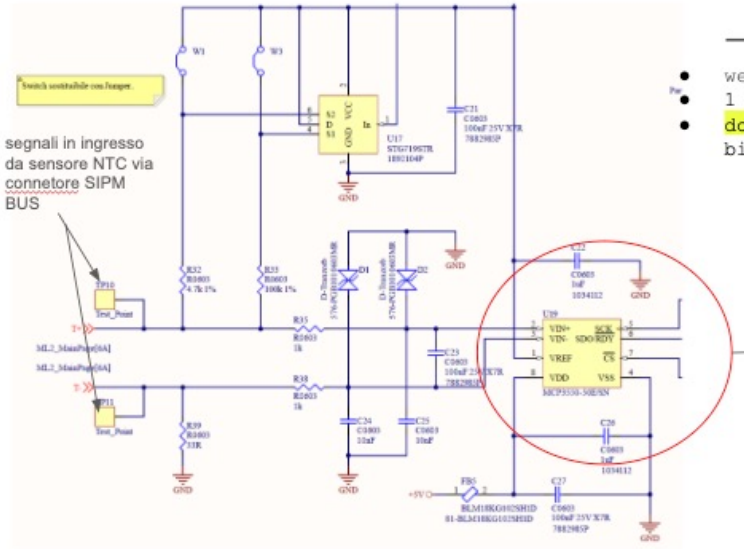
NTC sensor measurements

- we foresee external ADCs
- for NTC we used resistor net with drivable switch to have adequate resolution at low temp (-30/-40) and annealing temp (150 C)
- we select ADC multi-channel with differential input to make parametric T measurement
- we read ADC via I2C / FPGA



→ requirements for RDO:

- we mount 4 analogue switch STG719STR to select resistance load for NTC sensor
- 1 I/O from FPGA connected to parallel input of 4 switch STG719STR
- double check resistor choice RL=47k e RH=0.5 kOhm This choice increases a little bit current during annealing may be.

replaced by ADC from TI
ADS1219-4

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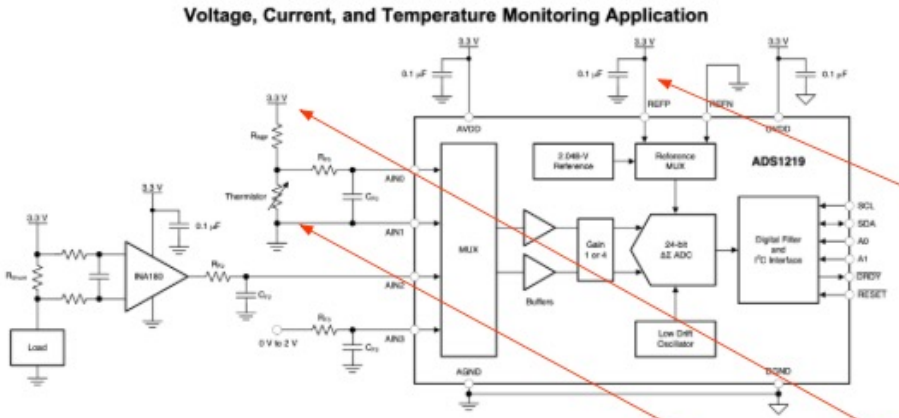
We evaluated possibility to use ADC inside Artix FPGA but due to PIN I/O constraints and limitations of SYSMON package in ARTIX, we moved to discrete ADC, building on experience of last test beams. There is also a layout benefit likely.

NTC sensor measurement (2)



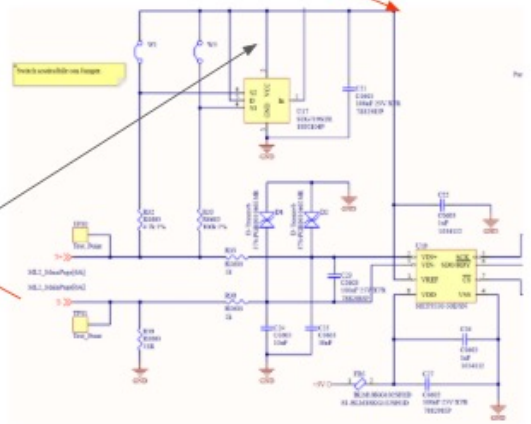
ADS1219 4-Channel, 1-kSPS, 24-Bit,

1 Features

- Easy to Use With Only One Register to Program
- Current Consumption as Low as 315 µA (typ)
- Wide Supply Range: 2.3 V to 5.5 V
- Rail-to-Rail Input Buffers to Achieve High Input Impedance
- Programmable Gains: 1 and 4
- Programmable Data Rates: Up to 1 kSPS
- Up to 20 Bits Effective Resolution
- Simultaneous 50-Hz and 60-Hz Rejection at 20 SPS With Single-Cycle Settling Digital Filter
- Two Differential or Four Single-Ended Inputs
- Internal 2.048-V Reference: 5 ppm/°C (typ) Drift
- Internal 2% Accurate Oscillator
- I²C-Compatible Interface
- Supported I²C Bus Speed Modes: Standard-Mode, Fast-Mode, Fast-Mode Plus
- 16 Pin-Configurable I²C Addresses
- Package: 3.0-mm × 3.0-mm × 0.75-mm WQFN

We use ADC input as “differential” as recommended for T measruement

VREF for ADC is given via 2.5 V connected to the resistor net



The MOSFET swittch is routing VREF
Note VCC MOSFET must be 1.8V (or 2.5V depending which bank we use on FPGA)

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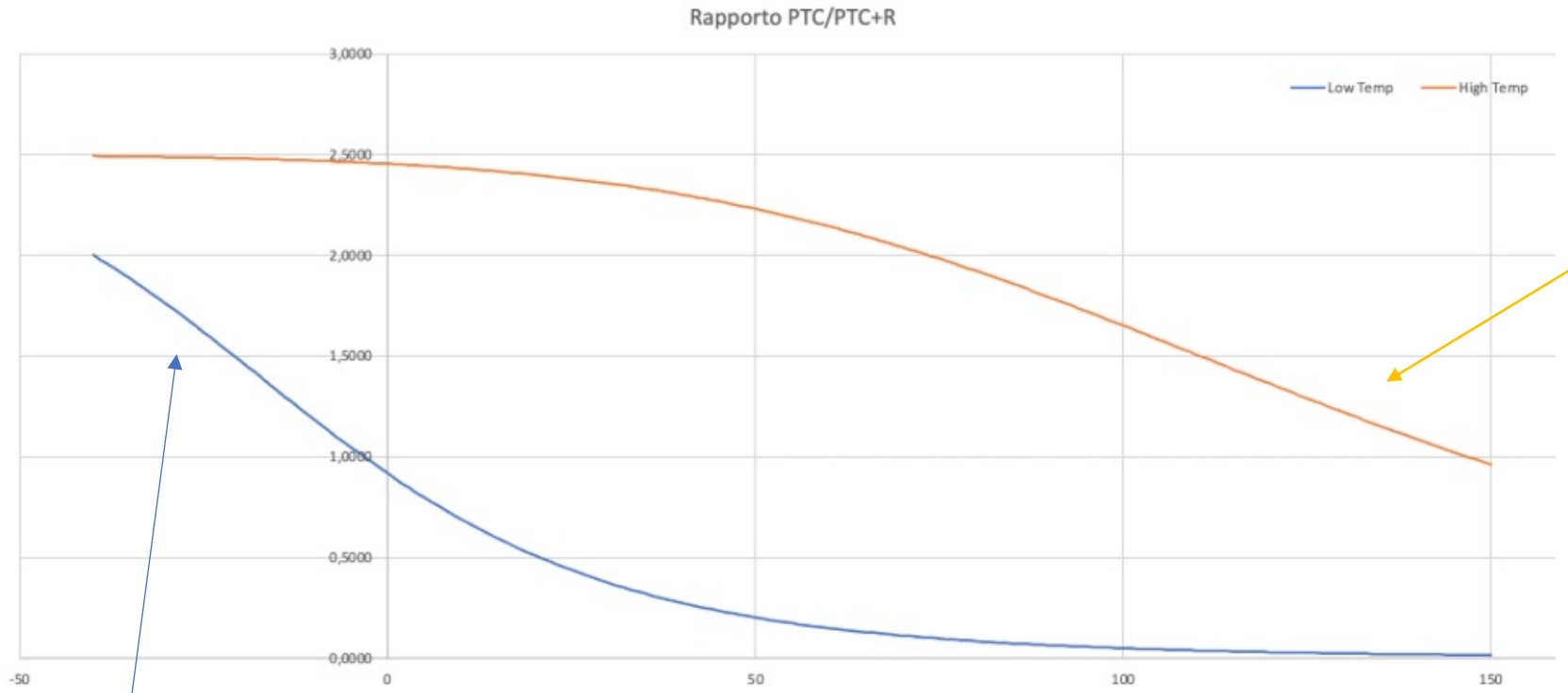
NTC sensor measurement (3)

P/N	NTCG103JF103FT1S					R1 low t=	47	k ohm			
R25	10	kf¶ +/-	1	%		R1 Hi t=	0,5	k ohm			
325/85	3435	K +/-	1	%		Nbits	24	bits	Vref	2,5	



good sensitivity at high temperatures, during annealing

good sensitivity at low temperatures

RDO SoW - Milestones status & outlook

- Design and realisation of a specific ePIC RDO card prototype, housing a FPGA, LDO, optical transceiver and I/O and LV power connections to provide the read-out to four ALCOR v3 ASIC. A high degree of integration is foreseen between the RDO card and the 4 FEBs that will house each an ALCOR64 v3 chip.

- as per report design is in progress, no major show stoppers identified

- Realization of a RDO card ePIC-compliant for the ALCOR readout: 10/2024

- on target, schematics should go to ext. company for layout in May. Delivery in October possible. Full FW development/test will go beyond 10/24!

Next steps:
- Finalize schematics/components + several details in bus pinout and geometrical/electrical constraints
- Inclusion of VTRX, Flash and FPGAs connections in firmware design