NUCLÉAIRE & PARTICULES

Omega

ÉCOLE POLYTECHNIQUE

IP PARIS

CALOROC
status and plans

monthly report 4 April 2024

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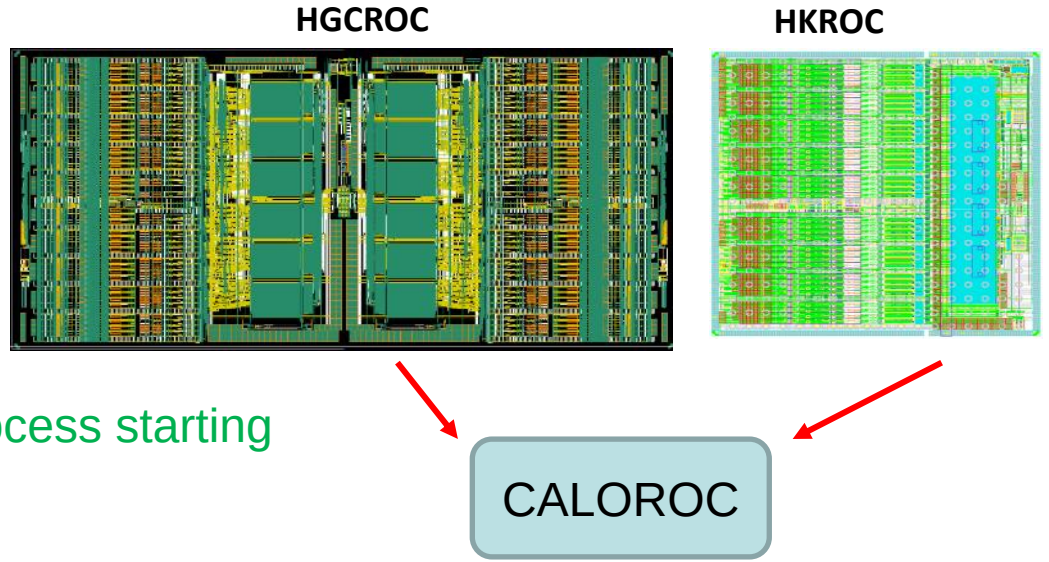
Organization for Micro-Electronics desiGn and Applications

CALOROC1 [F. Dulucq, P. Dumas, C. Munoz, M. Nguyen, D. Thienpont et al.]

- SiPM readout calorimetry: CMS H2GCROC with EIC readout and clocks (fast commands)
  - SiPM from 500 pF to 2.5 nF (or 10 nF)
  - ~5-10 mW/channel



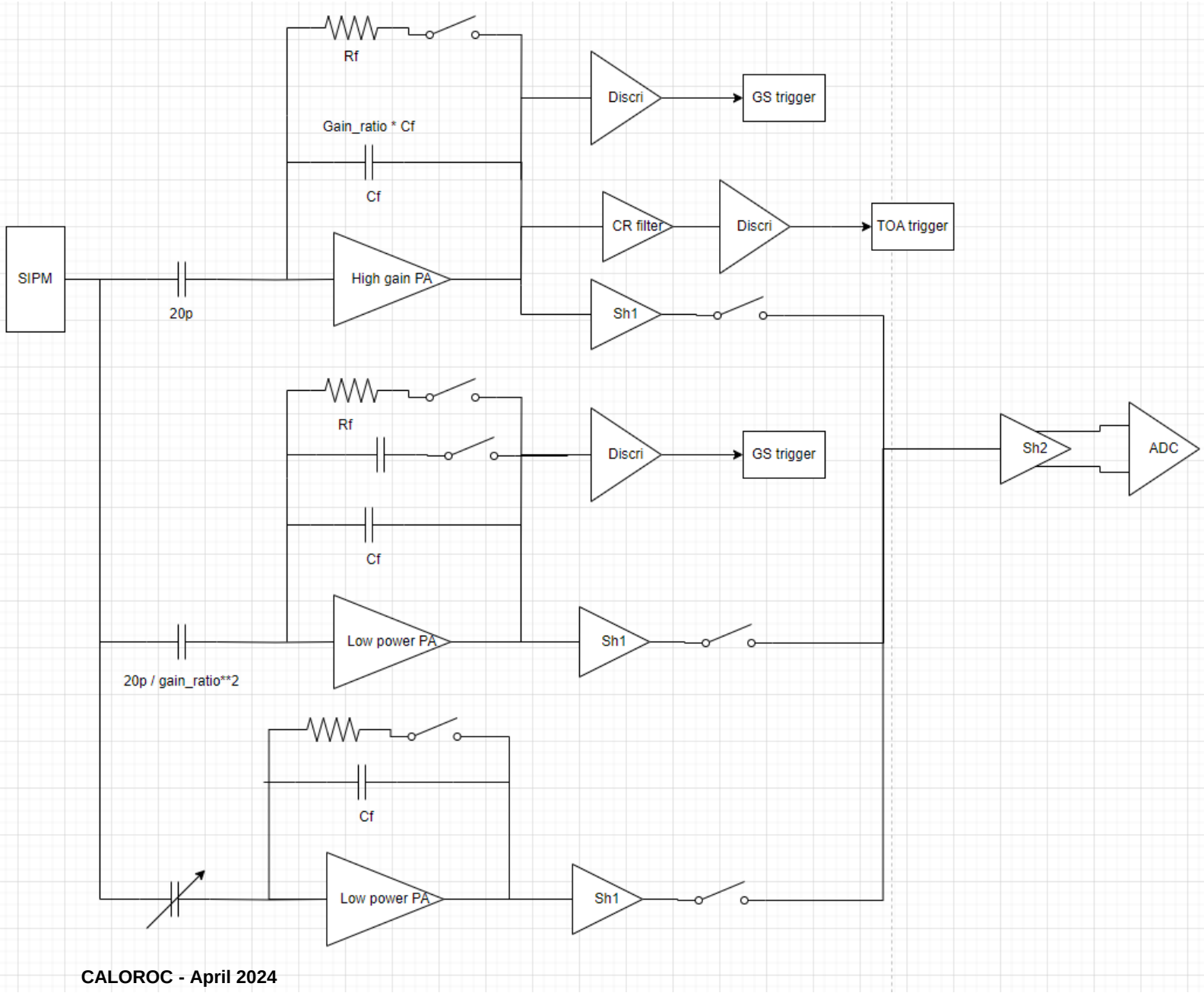
- CALOROC1A: conservative version
  - Uses H2GCROC (ADC, TOT) analog/mixed + new backend
  - Analog/mixed part complete
  - Digital part v0 available (with zero suppress) - verification process starting
    - Next steps: schematic + layout

- CALOROC1B: exploratory version (pin-pin compatible)
  - New analog part without TOT (dynamic gain switching)
  - Backend « à la HKROC » : auto-triggered, zero-suppressed
  - Status : simulations in progress with SiPM flavors
  - Digital part (common with CALOROC1A) to be adapted

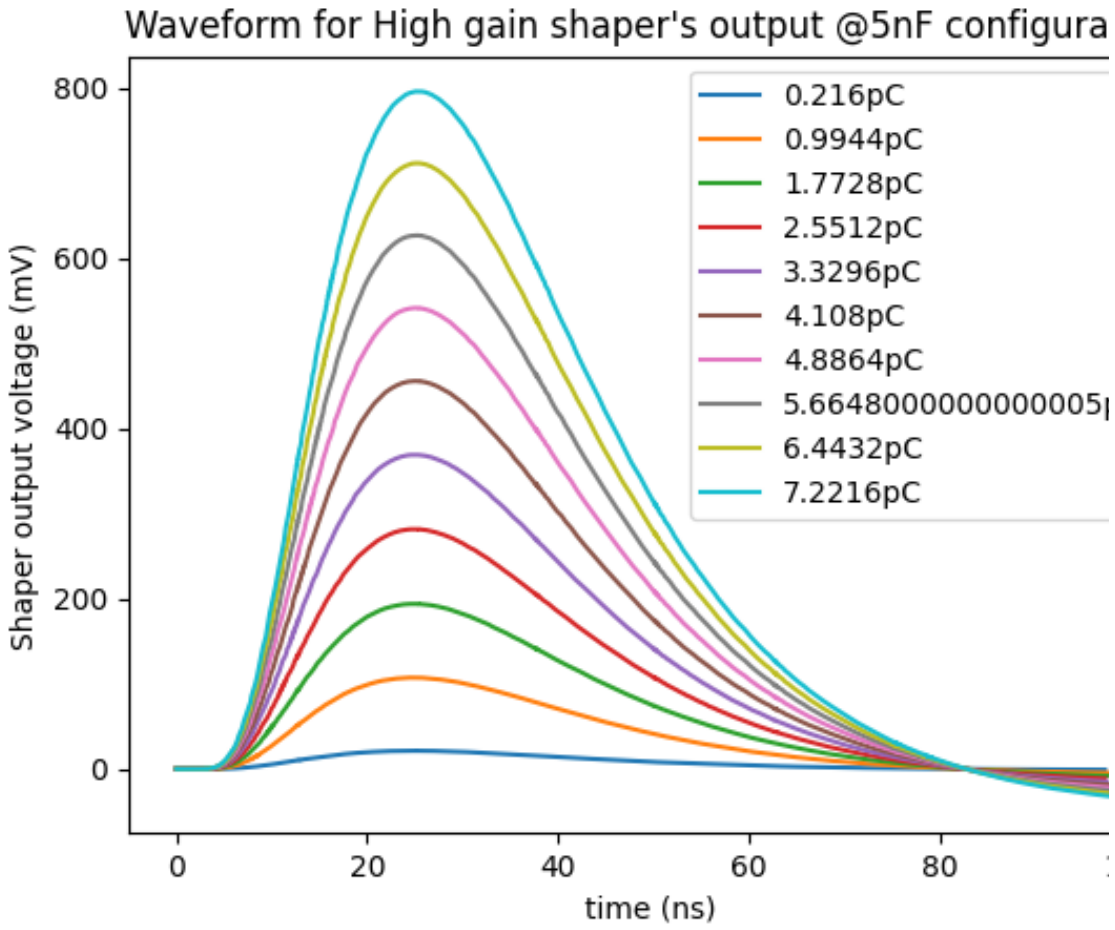
- New staff: S. EXTIER (2-year position) will design EIC-specific part (clocks + fast commands)

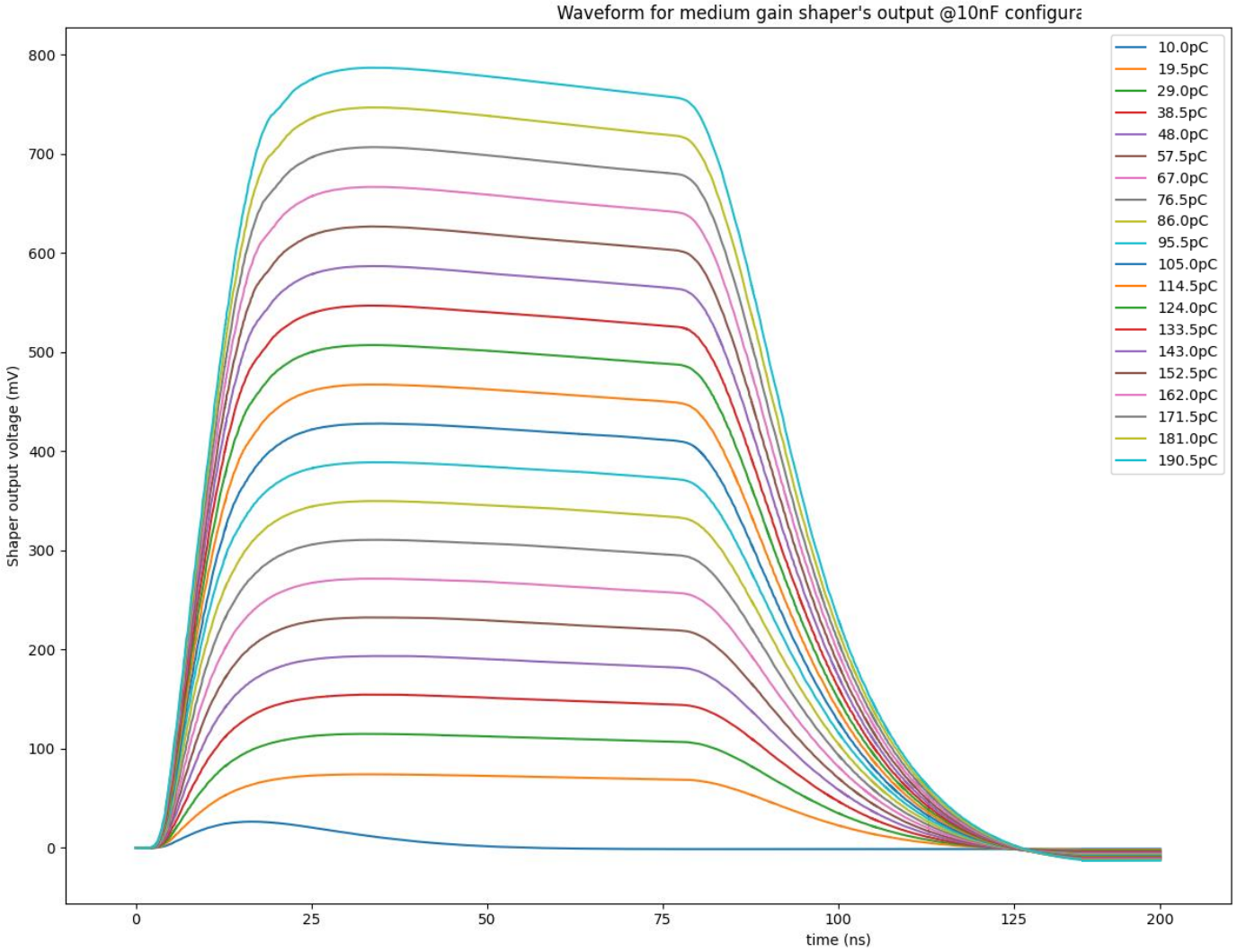
CALOROC1B: studied architecture [P. Dumas]

- 3 preamp divided in:
  - High gain
  - 2x medium gain
  - Low Gain
- 10b 40MHz ADC (Krakow)
- 25 ps TDC (Saclay)
  - Possibly 12.5 ps



CALOROC1B: Simulated waveforms (HG + MG)





Common: Fast commands for EIC

- Internal clock generator + external fast commands (x2 EIC clock bitstream, x2/5 internal clock)
  - 5 unique fast commands
  - 2 dual uses (link + calibration): 1 or 2 consecutive FC
  - Not included: 3 dedicated FC for parameters (I2C emulation) + 1 spare

Fast commands	Value	Description	Comment	Possible back to back	HD to IDLE
Idle	00011	Default, 40M phase inside	~99% of the time	Y	0
External trigger	01101	Pedestal measurement	For calibration	Y	3
ChipSync	01110	Fast digital only reset	Only when problems	N	3
BCR	10101	Load default value (parameter)	Real time operation	N	3
EBR	11001	Empty readout buffers	Free all internal memories	N	3
Link-sync-ROC or Link-reset-ROC	10110	Send sync pattern (x400) or Internal serial link reset	Link sync procedure or Link bit shift recovery (PLL SEE)	Y (1 or 2)	3
Calibration int or ext	11010	800 ns or 100 ns calib pulse		Y (1 or 2)	3
SC0	00101	Send SC bit 0	To built R or W frame	Y	2
SC1	01001	Send SC bit 1	To built R or W frame	Y	2
SC_Valid	01010	Validate action	Validate if frame + ID are valid	Y	2
Spare1	10010			Y	2

Common: Rates per channel

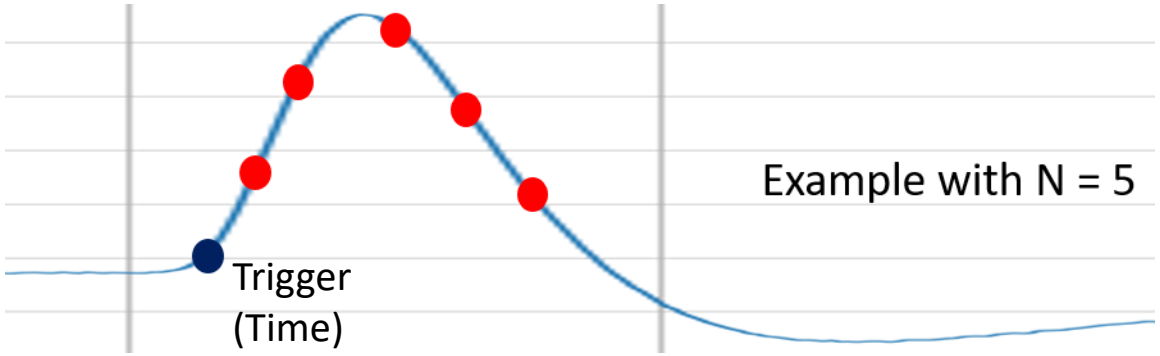
- Present HGCROC rate calculation: 1 serial link for 36 (+2) channels (HGCROC is arranged by 36 channels)

Version	Number of points (N)	Max rate	Remarks
Present HGCROC-36ch	1	976 khz / ASIC	LHC is 1 snapshot
Per channel (1 link/36 ch)	4 or 3	7-9 kHz / chn	Divide by N and by 36 (could be exercised)
Caloroc (1 link/18 ch)	4 or 3	24-32 kHz / chn	
Caloroc with zero suppress	4	55 kHz / chn	With 6 channels triggered (over 18)

Present HGCROC

CALOROC

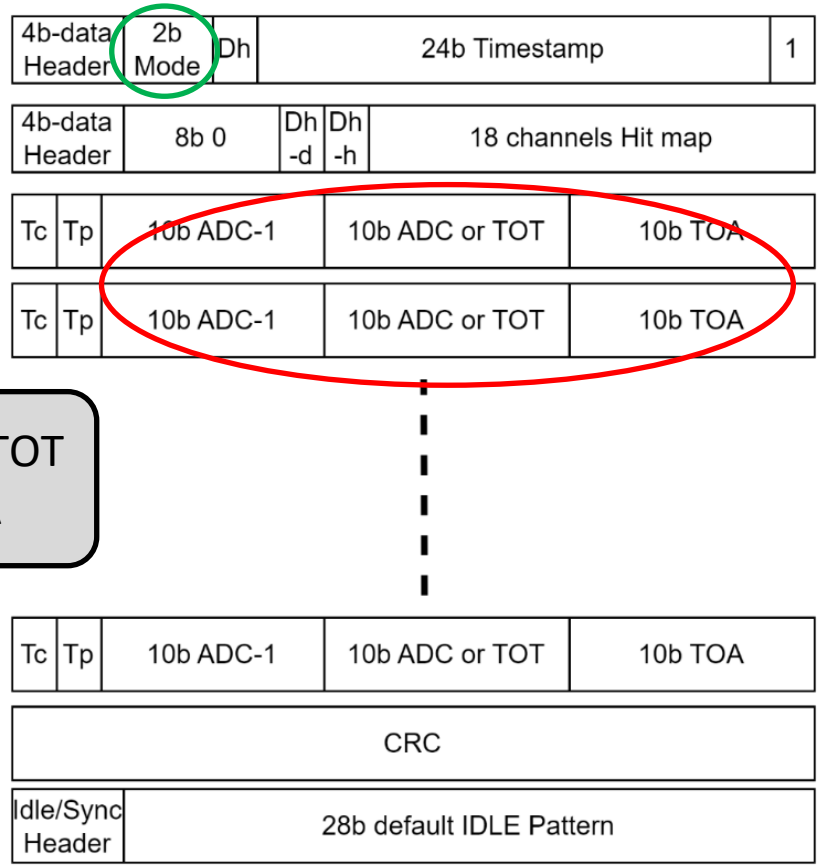
Conclusion: ZS with 2 serial links mandatory



CALOROC readout frame - WIP

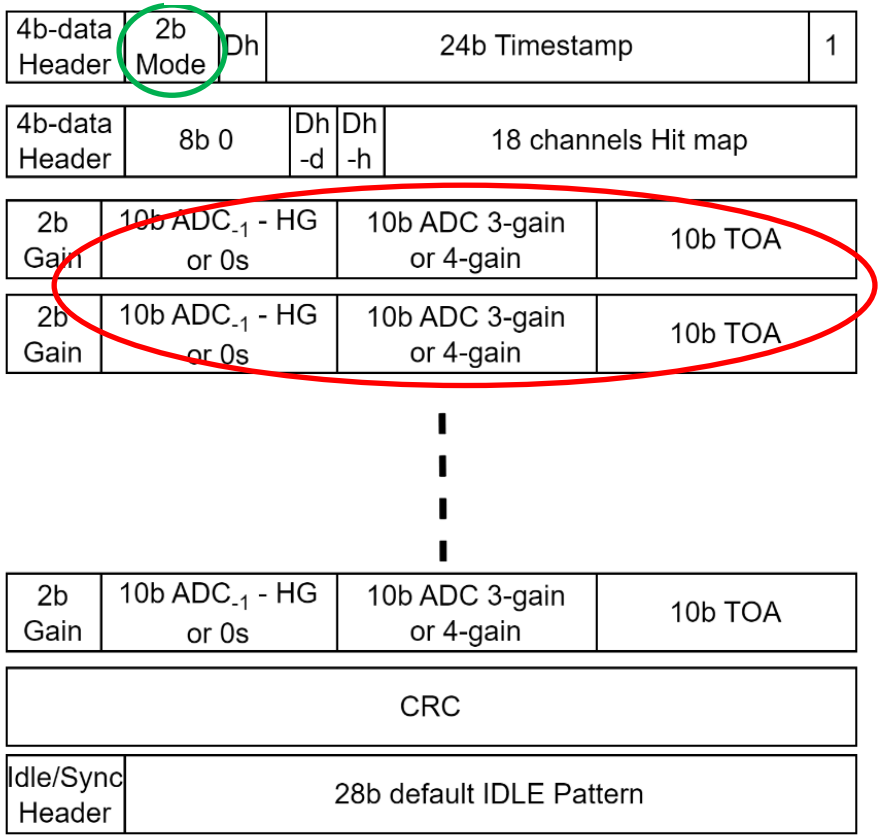
- Common to both CALOROC

CALOROC1A – similar H2GCROC



ADC – TOT TOA

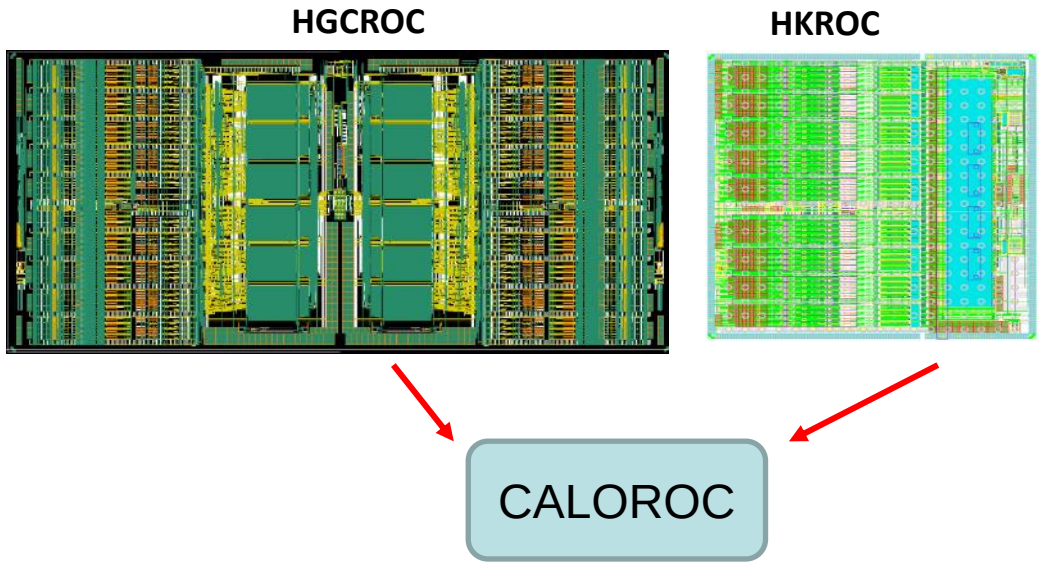
CALOROC1B – no TOT



4-gain ADC TOA

Plans for 2024

- CALOROC = CMS-H2GCROC (SiPM) for EIC
  - Analog part = H2GCROC, backend EIC specific
    - New position to design EIC-specific part (common)
  - Need to choose HGCROC pin-pin compatibility (64 ch) or HKROC size (32ch)
  - 2 versions : conservative (ADC/ToT), improved (multi-gain)
  - Cost in MPW : 2 * (50 or 100 mm²) * 2 k€ > Engineering run = 250 k€
  - Fall 2024



backup