EICROC Progress Report

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F. Bouyjou (CEA/Irfu/DEDIP)

Objective: **Development** and **characterization** of an **ASIC EICROC (32 x 32)**
able to read-out the new generation of pixelated (500 x 500 μm^2) silicon sensors: **AC-LGAD**
(**L**ow-**G**ain **A**valanche **D**iode) coupled **AC**
for the **Electron Ion Collider** (EIC)
1st intention: optimized for **Far Forward detectors:** the **Roman Pots**

Method: stepping up through succesive ASIC iterations
to control performances fulfilling ePIC detector requirements

- **EICROC0 prototype** (16 channels; 4 x 4): under test

EICROC Project: update (April 4th, 2024)

- **Studies of Probe PA jitter: on-going (BNL, Hiroshima Univ., IJCLab)**
- **Scrutinizing Discriminator Efficiency (S-Curves): Threshold Scan (varying charge injected): on-going (OMEGA, BNL, IJCLab)**
- **Scrutinizing TDC and ADC data for all 16 channels: on-going (OMEGA, IJCLab)**
- **EICROC0 chips**
  - Feb. 20th, 2024: **24 EICROC0** ASICs were delivered to BNL in view of hybridation (EICROC0+AC-LGAD)
- **10 pieces Updated EICROC0 PCBs (test boards) and Related topics**
  - Cabling performed at IJCLab: **finalized March 6th, 2024**
    [omitting crossing components to allow for the wire-bonding]
  - **Wire-bonding of EICROC0 onto 2 PCBs achieved** by IPHC (Strasbourg, France)

New The 2 boards are being shipped to IJCLab ⟶ 1 IJCLab, 1 OMEGA
We propose to first test this configuration (board operational)
* before wire-bonding an hybrid EICROC0+AC-LGAD
* before ordering 10 more PCBs

New
  - **March 22nd: 3 PCBs** were sent to BNL with associated crossing components
  - **Still waiting AC-LGAD sensors** (from BNL) to be transferred to CERN, to be given to IJCLab

* [*2 PCBs are intended to be sent later on to IPHC (Strasbourg, France) to wire-bond an EICROC0 + AC-LGAD*]
(Hybrid AC-LGAD provided by BNL)
* [*2 PCBs will wait for hybrids from BNL. They will be sent to IPHC (Strasbourg, France) for wire-bonding*]

New ***** Welcomed Mathieu Benoît (ORNL) at IJCLab on March 12th, 2024**

EICROC0 testing: ADC (charge) investigation

S. Conforti, A. Verplancke

OMEGA Microelectronics

Setting and method:

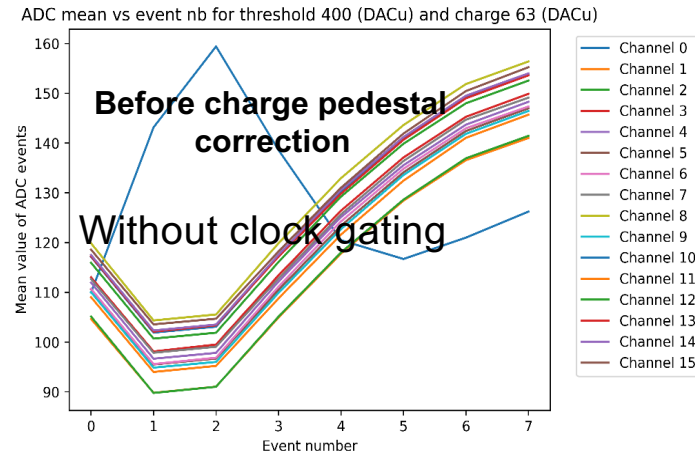
* Maximum charge injected into **channel #0** [DAC pulser 63 → 250 mV in 100 fF → **~ 26 fC**]
* Charge ADC values are measured for all channels

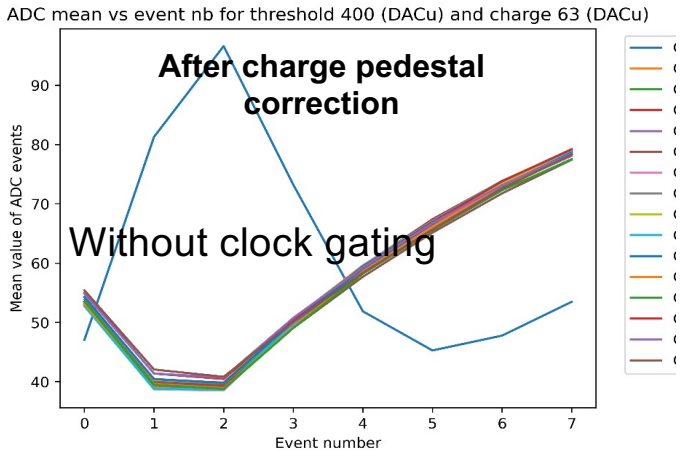
To measure the ADC pedestal, clock gating is deactivated to continuously measure the shaper output value and estimate the ADC pedestal

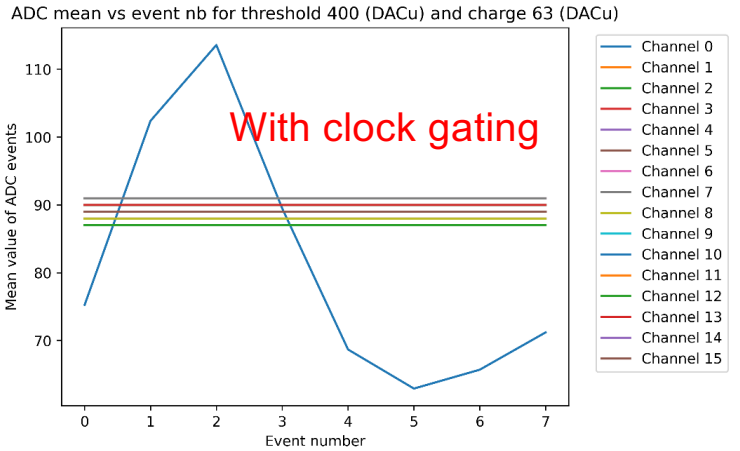
ADC pedestal before adjusting the shaper output DC level using a DAC (Vref_correction), which allows for adjusting the DC level on each #

The pedestal is evidently more uniform after the correction.

Charge measurement in channel #0 where the signal is injected (with clock gating activated).







The strange shape of the pedestal indicates couplings at the charge pedestal level

The shaper signal also observed on scope (analog probe): coupling is evident even in the analog part.

A preliminary observation of these signals on the scope suggests that **the coupling is between the CMD pulse and the shaper output**. Further investigations underway

EICROC0 testing: Cross-Talk investigation

S. Conforti, A. Verplancke

OMEGA Microelectronics

Setting and method:

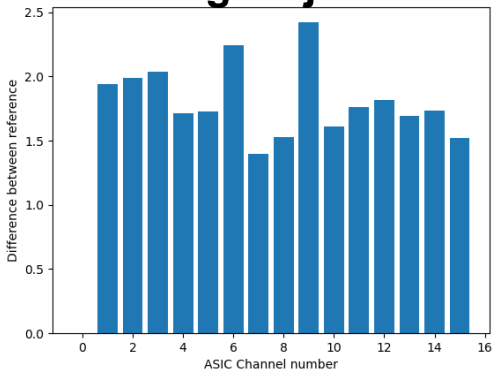
* Maximum charge injected into **#0, #6 & 15 separately** [DAC pulser 63 → **~ 26 fC**]

- The discriminator threshold is scanned across all channels to count the number of triggers generated by the internal signal (CMD pulse).
- Theoretically, when we scan the threshold without injecting a signal, the discriminator triggers on the noise present on the preamplifier DC level (the pedestal).
- If there is a coupling signal in nearby channels due to the signal injected into one channel, the pedestal of the nearby channel could shift.

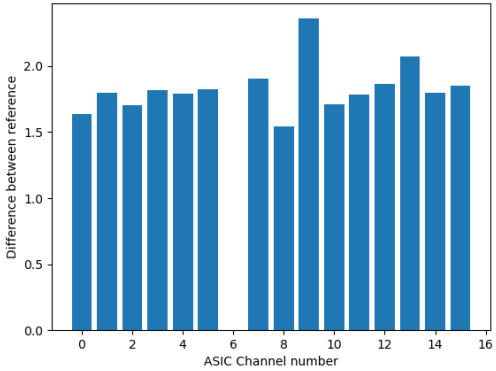
Pixel / Channel Mapping	Column 0	Column 1	Column 2	Column 3
Line 0	Pixel (0,0) #00	Pixel (1,0) #04	Pixel (2,0) #08	Pixel (3,0) #12
Line 1	Pixel (0,1) #01	Pixel (1,1) #05	Pixel (2,1) #09	Pixel (3,1) #13
Line 2	Pixel (0,2) #02	Pixel (1,2) #06	Pixel (2,2) #10	Pixel (3,2) #14
Line 3	Pixel (0,3) #03	Pixel (1,3) #07	Pixel (2,3) #11	Pixel (3,3) #15

In the figures, we plotted the **difference in the 50% trigger efficiency** when no signal is injected and when a signal is injected into only one channel

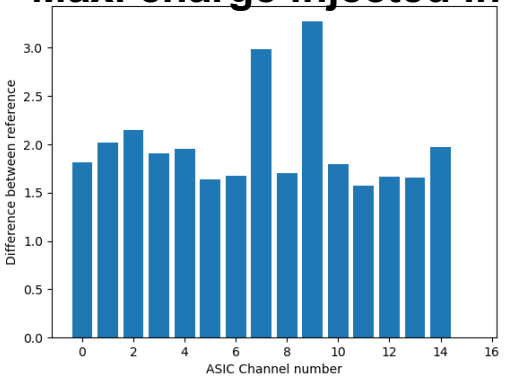
Max. charge injected in #0



Max. charge injected in #6



Max. charge injected in #15



The pedestal shifts of around 2 DACu that corresponds to 0.22 fC [~0.8%] (in agreement with previous measurements with Probe PA). This value is within the range of measurement error.

Low value indicates → no coupling signal present in the trigger path. Should be evaluated with ADC

EICROC Project: Update & Perspectives [1/2]

- Recurrent EICROC periodic meetings (every 2 weeks):
  Hiroshima University, BNL, IJCLab, OMEGA, CEA/Irfu/DEDIP **Update Reports**
  Gathering 12 persons (in average) involved in EICROC0 characterization
  https://indico.ijclab.in2p3.fr/category/538/

- Perspectives for ramping up on EICROC0 testing:
  - Exploiting EICROC0 analogical Probe PA output signals & digital outputs:
    * **Laser test bench** (at BNL) requires synchronisation capabilities,
    * **Beta source** (IJCLab & BNL) requires triggerless acquisition
    * **Premature to take part to the DESY test beam next June to be certain to get successful results out of it**
      (wire- & bump- bonded AC-LGAD & EICROC0 – Updated PCBs)
      Will consider future beam test scheduled within EIC collaboration

New

EICROC Project: Perspectives [2/2]

Next iterations: EICROC0A & EICROC1

- **EICROC0A: including a low power ADC (study on-going) + improved testing capabilities**

- **EICROC1:**
  - **4 x 32 (study on-going) to investigate floor planning**
  - **improved/additional testing capabilities**

*EICROC (0A & 1) and CALOROC ASICs will be submitted together for fabrication within an OMEGA Engineering run **(fall 2024)***

The EICROC project team

EICROC — D. Marchand

WP1 – Micro-electronics — C. De La Taille

Front-End	C. De La Taille, A. Verplancke
Low power ADC	A. Verplancke
TDC	F. Bouyjou, E. Delagnes
Overall Design & Documentation	C. De La Taille, F. Dulucq, N. Seguin-Moreau, L. Serin
PCB	P. Dinaucourt
Firmware	B.-Y. Ky
Data acquisition	F. Dulucq

WP2 – Characterization — L. Serin

ASIC Functionnal Response	F. Bouyjou, S. Conforti, D. Marchand, N. Seguin-Moreau, L. Serin, A. Verplancke
ASIC + AC-LGAD Functionnal Response	S. Conforti, D. Marchand, N. Seguin-Moreau, L. Serin, A. Verplancke
Source Beta IR Laser Test beam	S. Conforti, D. Marchand, C. Munoz Camacho, L. Serin, A-S. Torrento, A. Verplancke

IJCLab Irène Joliot-Curie Laboratoire de Physique des 2 Infinis

cea Dedip Irfu

OMEGA Microelectronics

+ A. Tricoli's team — Brookhaven National Laboratory

synergy with Japan (Univ. of Hiroshima)

IJCLab : + 1 year postdoctoral position (June 1st '24, Univ. Paris-Saclay/P2I)

BACKUP

EICROC0 requirements and design: 16 channels (4x4)

Requirements:

- pixel size **0.5 x 0.5 mm²** *(HGTD 1.3x1.3 mm²)*
- low power consumption < **2 mW/channel**
- low jitter **~ 20 ps**
- low noise **~ 1 mV/channel**
- sensitivity to low charge **(2 fC)**
- time resolution: **30 ps**
- spatial resolution: **50 microns**

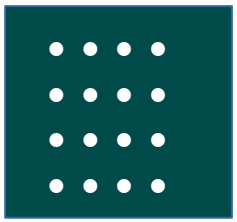
Charge sharing studies

(simulation + β source w/ **ALTIROC1**_v2)

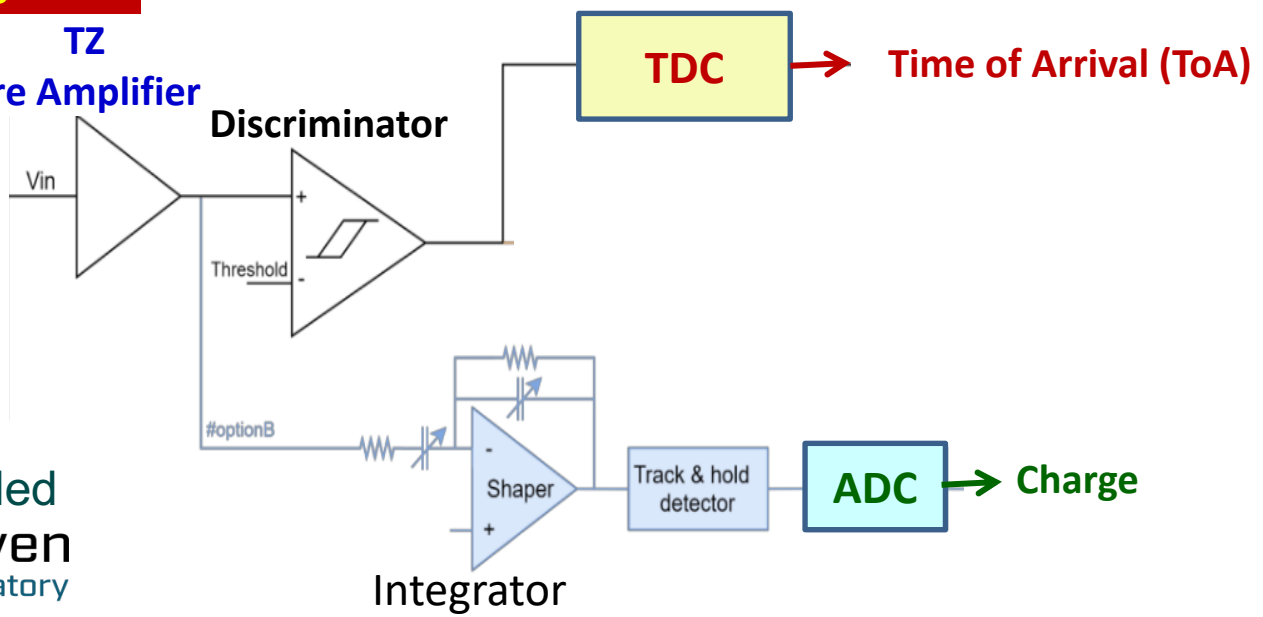
EICROC0 design:

- **TZ Pre Amplifiers** from ALTIROC (ATLAS/HGTD)
- 10 bit **TDC** from HGCROC (CMS, CEA/Irfu)
- **8 bit ADC** for time-walk correction (AGH Krakow, adapted from HGCROC)

1 channel (1 pixel) schematics



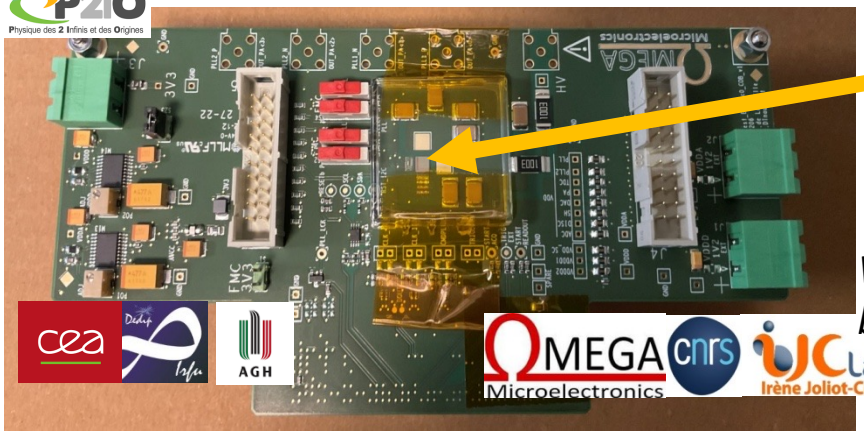
AC-LGAD
pixelated sensor
designed and provided
by Brookhaven National Laboratory



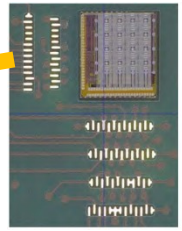
Compared to ALTIROC (ATLAS/HGTD), ToT TDC (non-linear behavior versus the deposited charge) replaced by an ADC

Status of EICROC0 Test Bench at IJCLab

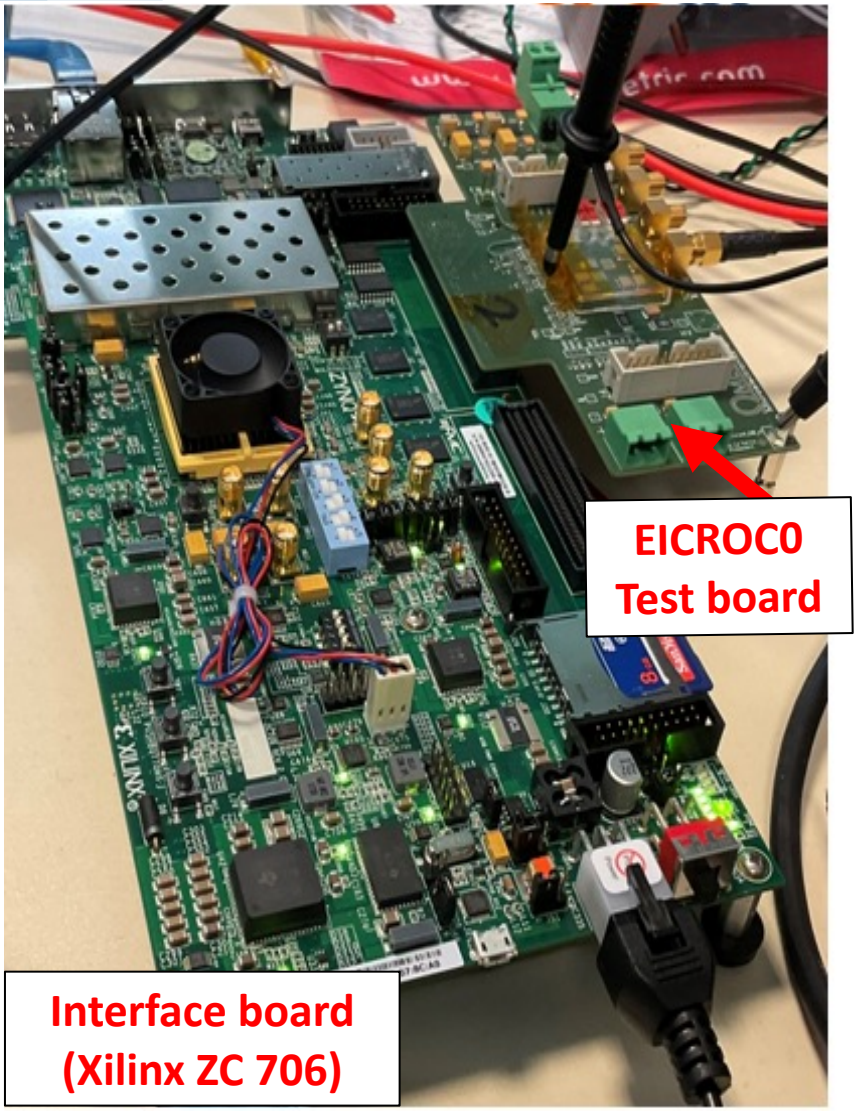
EICROC0 Test board



EICROC0 chip



Wire-bonding by Brookhaven National Laboratory



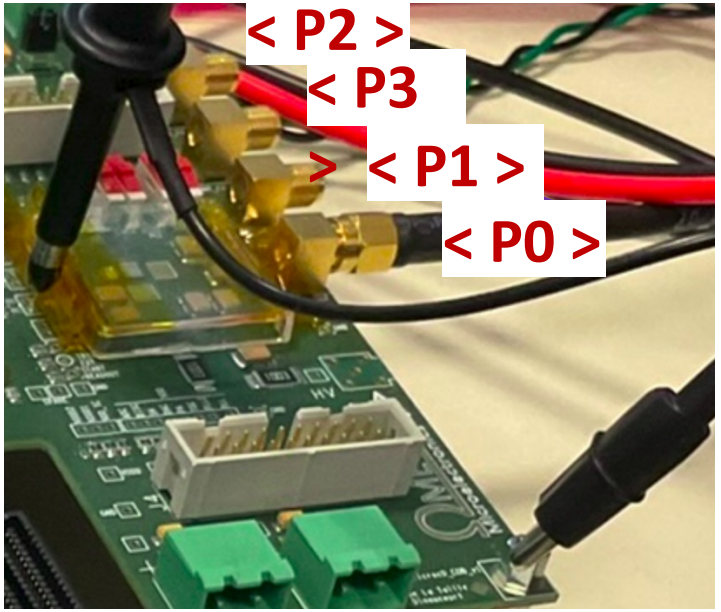
EICROC0 test bench operational at IJCLab since March '23

- ✓ I^2C communication (firmware + software developments)
- ✓ Data stream written/read
- ✓ EICROC0 DC levels
- ✓ Discri. threshold exploration
- ✓ **EICROC0 charge injection system (0 to 25 fC)**
- ✓ **EICROC0 decoding (TDC, ADC) Firmware + software**
- ✓ **External trigger**: *signal directly injected into TDC*

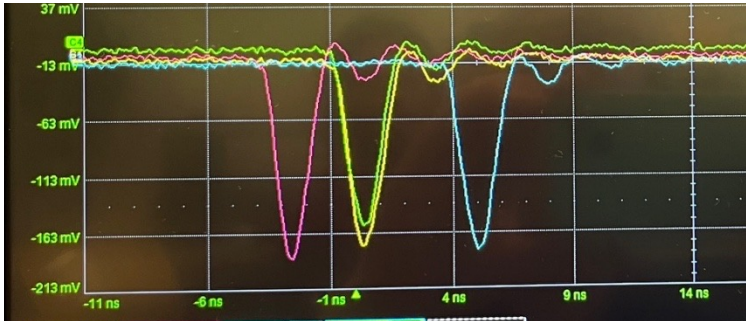
Additional EICROC0 test benches operational at:
OMEGA (May '23), BNL (July. '23), CEA/Irfu (Sept. '23)

EICROC0 TZ Pre Amplifier Probe output signals

Pixel / Channel Mapping	Column 0	Column 1	Column 2	Column 3
Line 0	Pixel (**0**,0) **#00**	Pixel (**1**,0) **#04**	Pixel (**2**,0) **#08**	Pixel (**3**,0) **#12**
Line 1	Pixel (**0**,1) **#01**	Pixel (**1**,1) **#05**	Pixel (**2**,1) **#09**	Pixel (**3**,1) **#13**
Line 2	Pixel (**0**,2) **#02**	Pixel (**1**,2) **#06**	Pixel (**2**,2) **#10**	Pixel (**3**,2) **#14**
Line 3	Pixel (**0**,3) **#03**	Pixel (**1**,3) **#07**	Pixel (**2**,3) **#11**	Pixel (**3**,3) **#15**



PA output signals through SMA connector s (PCB back plane)



Feature of EICROC0 test board:
Observation of 4 Probe PA channels simultaneously

1 Probe PA per column
Ex.: #00, #04, #08, #12