eRD109: Progress Report

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UC Santa Cruz UFSD group

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SCIPP
SANTA CRUZ INSTITUTE
FOR PARTICLE PHYSICS
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Status & Plans

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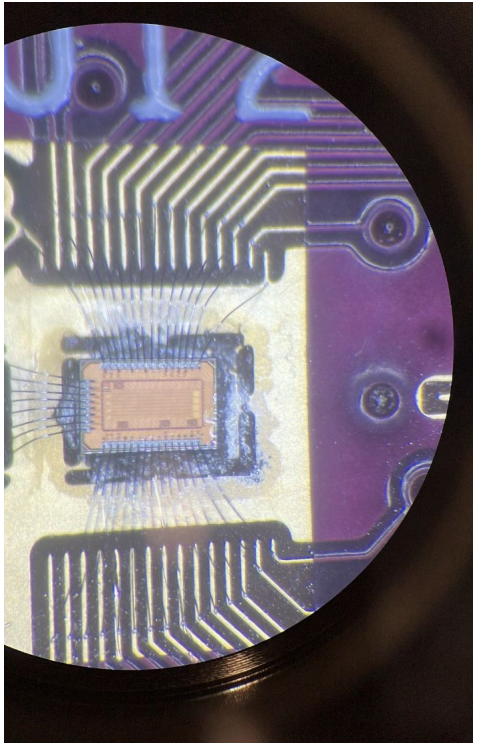
- ***HPSoC-v2 ASIC (Nalu Scientific)*:**
  - Chip with fixed digital back-end received back (“v2b”) from TSMC – passed initial “smoke test” at UCSC
  - Two readout boards have been loaded with the v2b chip and wire-bonded at SCIPP
    - One board sent back to Nalu for digital testing and firmware development
    - Another retained at UCSC – analog front-end re-characterization currently underway
      - From a quick look, we see similar performance as v1a (as expected)
    - Additional unpopulated boards at Nalu; planning to load 3-4 more boards in the next few months



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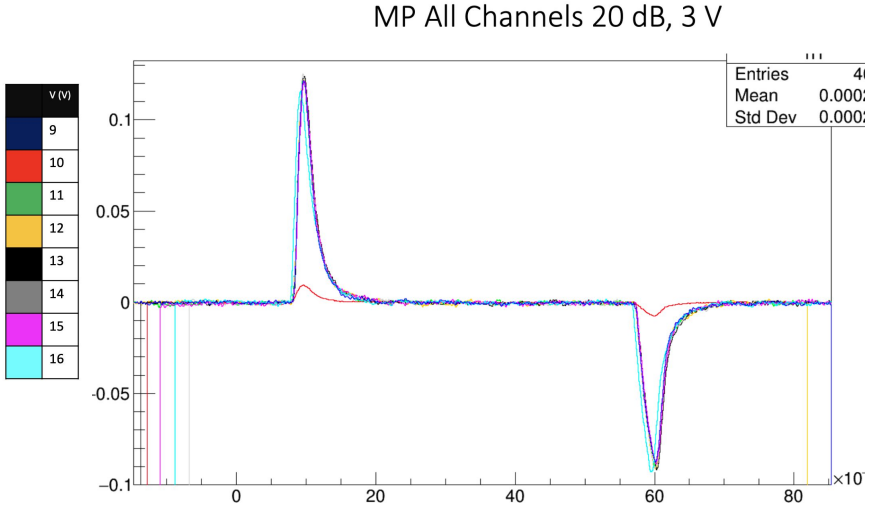
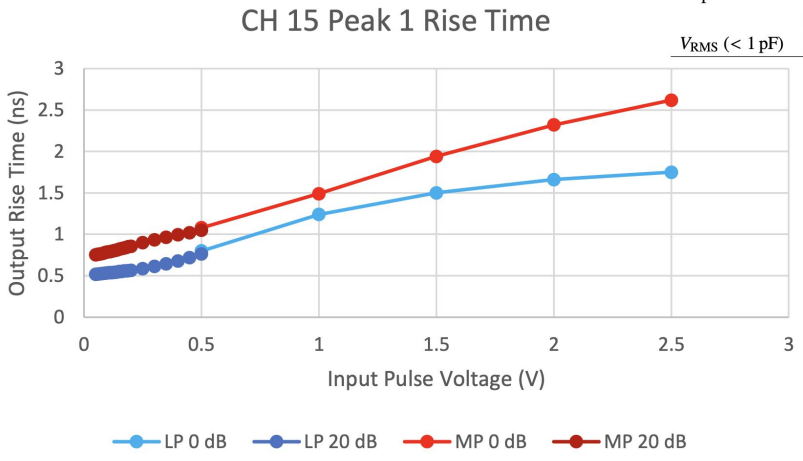
- ***AS-ROC (Anadyne Inc; low power SiGe)***
  - Full characterization of 8 channels performed by our undergraduate student
    - One of the channels exhibiting low gain (to be understood), all others channels behaving as expected; rise times from 500ps - 2ns

Parameter	Chip type	Target value
Power cons.	MP	1.1 mW/ch
	LP	0.6 mW/ch
Rise time	MP	600 ps
	LP	800 ps
10 ps Jitter @	MP	5 fC
	LP	8 fC
V_{RMS} (< 1 pF)	MP/LP	0.4–0.75 mV





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- ***AS-ROC (Anadyne Inc; low power SiGe)***
  - Chip designers have continued several more debugging sessions at UC Santa Cruz:
    - The signal shape and crosstalk has been dramatically improved and appears to be similar to simulation when the IC is only driving the trace up to the AC coupling capacitor, removing the buffers from the circuit.
    - Discriminator can now be properly characterized
      - Once debugging efforts with the chip designers have concluded, another complete recharacterization will be performed
    - The 50 ohm terminations loaded at the input of the buffers in previous tests also dramatically attenuated the preamp signa. The gain is even better than previously found, and actually around 40 percent higher!