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# Status report of the eRD109 project on SALSA chip development

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EPIC DAQ/electronics WG meeting  
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## ■ Versatile front-end characteristics

- Dedicated to MPGD detectors and beyond
- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1nF
- Large range of peaking times: 50-500 ns
- Large gain ranges: 0-50 to 0-5000 fC
- Large range of input rates, up to 100 kHz/ch with fast CSA reset (limit assumed for EPIC: 25 kHz/ch)
- Reversible polarity
- Front-end elements can be by-passed

## ■ Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s
- Possibility to double rates by coupling pairs of channels
- Integrated DSP for internal data processing and size reduction, treatment processes to be selected according to user needs
- Continuous readout compatible with streaming DAQ foreseen at EIC, triggered mode also available
- Several 1 Gb/s output data links

## ■ General characteristics

- ~1 cm<sup>2</sup> die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, TID), working at 2T magnetic field



## ■ PRISME prototype

- Test of new hybrid 65nm PLL block for SALSA with 4 clock outputs

## ■ Test bench

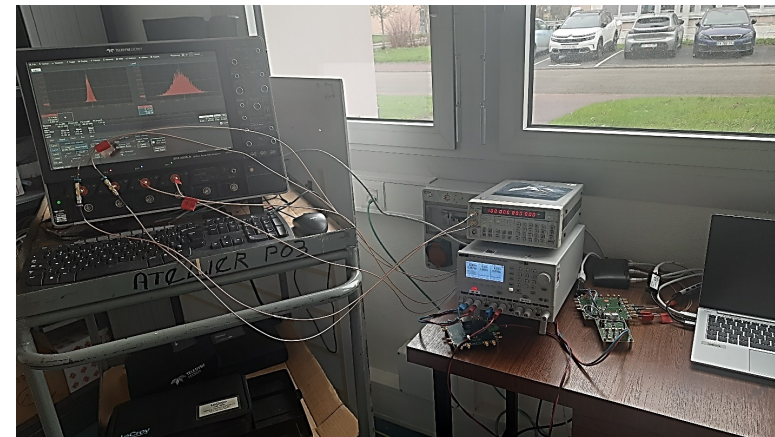
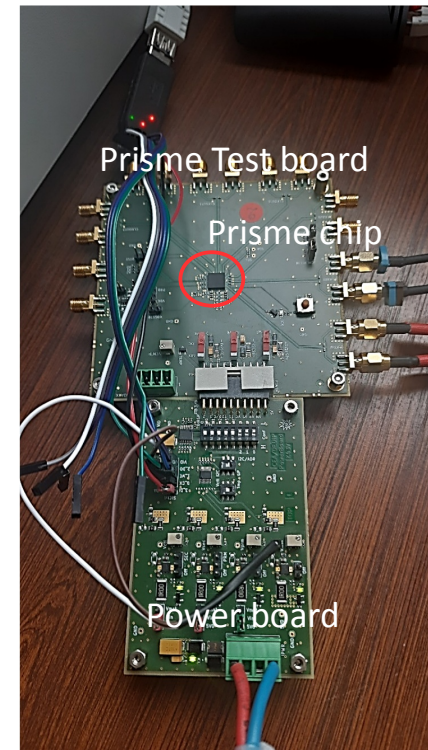
- Power boards + PRISME test boards
- Low jitter clock generator from CERN + high precision signal generator, high end 80GS/s scope and phase noise analyzer

## ■ Preliminary results

- Power consumption nominal
- I2C working to read and write registers
- Low voltage differential clock signals going in and out the chip

## ■ Tests on PLL block

- Digital branch of PLL operational
- Oscillator reaches the 3.2 GHz nominal frequency from 40 and 100 MHz input clocks
- Time jitter of 8 to 15 ps depending on the configuration, optimization still in progress
- All 4 configurable outputs tested → deliver right requested frequencies
- A few sources of noise found, fixed in PLL design
- Further studies foreseen after SALSA1 submission





## ■ Purpose and architecture

- Performance evaluation of front-end + ADC chain, + tests of different blocks
- 4 front-end channels + 2 direct inputs to ADC, 12-bits parallel output with dynamic multiplexer

## ■ General Status

- All block layouts almost done, some connections between them to be done (slow-control)
- Submission to TSMC April 17<sup>th</sup> (slot reserved) → tight time line
- Global simulations and verifications to be started very soon

## ■ Front-end stage

- Layout design of updated SALSA0\_analog version finished
- New version of front-end with improved pole-zero cancellation: schematics and layout done
- Simulations and checks in progress

## ■ ADCs

- ADC 1 (Sao Paulo): updated to 50 MS/s sampling rate, reduced surface ( $< 200 \times 250 \mu\text{m}^2$ )
- Layout done, sent to Saclay to be integrated in chip, simulations ok, some checks still ongoing
- Interface buffer between front-end and ADC (Sao Paulo): layout done, sent to Saclay, some simulations to be done of the full chain front-end + buffer + biases
- ADC 2 (Saclay): layout design complete, simulations with other blocks in progress

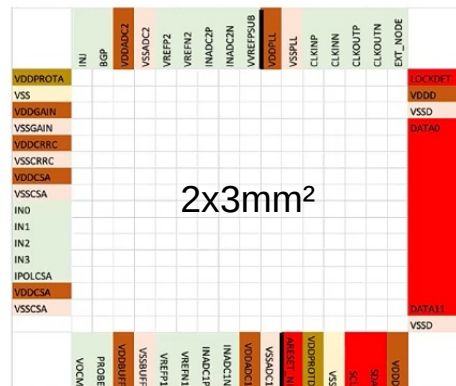
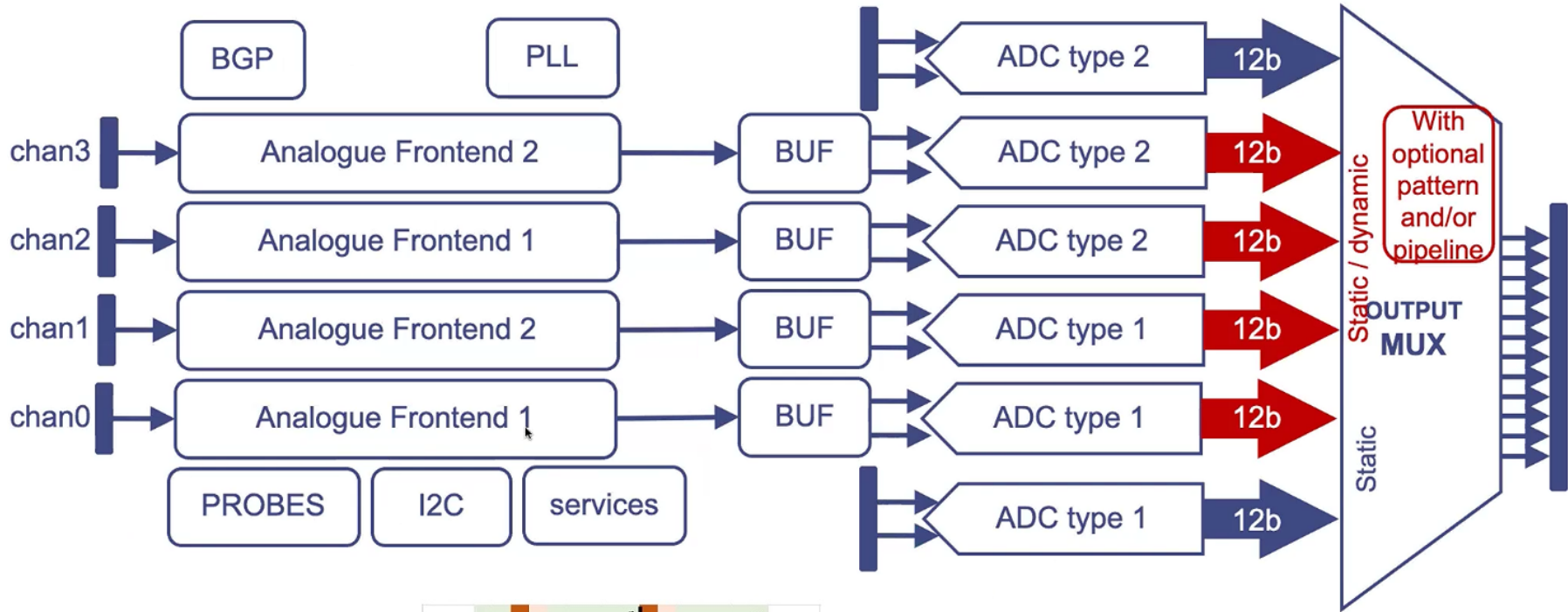
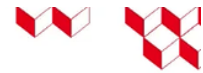
## ■ Services

- PLL (updated version), bandgap, probes,... taken from PRISME, bias blocks almost finished
- I2C and service layouts completed, basic I2C architecture validated with PRISME
- Multiplexer layout completed, simulations in progress





## Today Architecture / Building Blocks





## ■ Purpose and architecture

- Like final SALSA but with reduced number of channels - 32 ?
- Implement full chip architecture including DSP and input/output interfaces in a version close to the final one

## ■ DSP

- First draft of data processing established and presented at EPIC DAQ WG in January
- Design of architecture in progress, draft of data format in discussion,
- Draft list of processes: baseline correction, common mode correction, digital filtering, zero suppression, feature extraction, trigger management, generation of calibration data, data formatting
- Almost no progress in March as peoples are busy with SALSA1, to be resumed after mid-April
- **We still need inputs about DSP feature requests from MPGD and DAQ WGs ! (cf January presentation)**

## ■ Input interface

- Unified interface proposed, combining clock + synchronous commands + slow-control in one diff line, under study
- Synchronization of chip with EIC/EPIC time structure, connection with DAQ commands, etc... under discussion with EPIC DAQ community, **we also need inputs on this !**

Expected to be submitted first trimester 2025



## ■ eRD109 FY23 project milestones

- Specifications of SALSA1 design → done
- Production of SALSA1 prototypes → submission April 17<sup>th</sup>
- Packaging and test card production → expected Autumn 2024
- Performance evaluation → expected end of 2024 / beginning of 2025

## ■ Milestones of generic R&D program for EIC project (new 65nm PLL block)

- PRISME prototype submission → done July 19<sup>th</sup> 2023
- Packaging and test card production → done February 2024
- Radiation tests → Summer 2024 ?

## ■ eRD109 FY24 project milestones (proposal)

- SALSA2 specifications → July 2024
- SALSA2 submission → March 2025
- Beginning of SALSA2 tests → September 2025

## ■ Very next steps

- SALSA1 submission → April 17<sup>th</sup>
- Tests on PRISME prototypes → to be continued after mid-April
- SALSA2 specifications and architecture → Summer 2024