BTOF Readout Board Design

mostly just questions at this early stage…

not even PRELIMINARY

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Assumptions about the RDO but mostly unknowns

- Readout Board needs to readout/control 64 128-channel FCFD ASICs
- each ASIC
  - 1 lane clock (freq? 98.5 MHz or some multiple)
  - 1 lane fast command (xxx Mbs? can be as low as 98.5 Mbs)
  - 1 lane data (xxx Mbs? can be as low as 98.5 Mbs)
  - 2 signal I2C (1 MHz SCL?)
- connect to ASICs via flex PCB and some high-density connector on the RDO, TBD
- location & footprint not well known
  - assume on the order of 5 x 10 cm?
- what about LV to the ASICs?
  - how do we feed it? via same flex cable where the signals are? is the LV fed via the RDO or from a separate power board?
- what about bias voltage?
  - how do we feed it? via same flex cable as the signals? or with the LV? or separately?
- other non-ASIC signals e.g. for thermistors?
- cooling of the RDO?
- fiber, LV, HV routing?
- good grounding scheme to the detector mass? (BTW, I haven't seen any discussion about this important matter?)

ASIC signals

- I2C
  - we don't think we can talk to 64 ASICs over a single I2C bus, the load is too high
    - we will assume 4 buses with 16 ASICs each @ 1 MHz SCL clock
- ASIC clock
  - we need to distribute 64 (!) copies of the very-low jitter clock
    - need a 64x fanout scheme ⇒ use ***7x*** Si53302 fanout PLL buffers (each with 10 outputs)
  - do we need cable driver chips due to the long flex PCB length?
    - I think that 1.3+m is on the limit for ~100 MHz clocks/signals
  - can we multidrop the clock and still keep the jitter < 5ps? at least over e.g. 2 adjacent ASICs?
    - this will need verification
- FPGA pin needs
  - 64 fast differential "fast command" lanes
  - 64 fast differential "data" lanes
  - 8 I2C signals (for 4 I2C buses)

FPGA Selection

- 128 (64in+64out) fast differential signals are impossible to meet with the Artix+ architecture (max is 104 for the largest AU25P FPGA, 78 for the AU15P as for the FTOF)
  - Option A: we need to put **2x AU15P** (or smaller AU10P?) FPGAs, connect 32 ASICs to each, pass data from one (slave) to the other (master, with the optical interface) via direct copper Gbs transceivers ⇒ doable
  - Option B: multidrop Fast Command 1:2 and use **1x AU25P** (larger flavor from ppRDO)
    - 64 data in, 32 data out == 96 (<104)
    - depends on the ASIC design somewhat
  - Option C: move to an even larger FPGA from the **Kinetix+** series
    - but this gets pretty expensive for features we don't need apart from pin-count
  - Option D: design the ASIC to also daisy-chain the data-out e.g. 1:2 and use **1x AU15P**
    - 32 data in, 32 data out == 64 (<78)
    - this needs careful design on the ASIC side!

ASIC readout features table

	typical (64in/64out/64clk)	multidrop fast cmd (64in/32out/64clk)	multidrop fast cmd & daisy chain data (32in/32out/64clk)
FPGA choice	2x AU15P	1x AU25P	1x AU15P
connector/flex pins*	392 (128+128+128+8)	328 (128+64+128+8)	264 (64+64+128+8)
w multidrop CLK	328 (128+128+64+8)	264 (128+64+64+8)	200 (64+64+64+8)

*without LV, GND, HV, thermistors(?)

- various multi-drop and daisy-chain techniques lower the pin count on the flex cable/connector 2X!
  - but they need ASIC design efforts and serious verification

Summary

- number of signals from the 64 ASICs to the RDO is high
  - issues for the cable/connector & issues for the FPGA
  - we should try to lower the signal count using various ASIC features
    - ⇒ *need tighter collaboration with the ASIC designers* *(as always)*
- we don’t have a good idea about the geometry of the RDO
  - size, placement?
  - associated cooling?
    - assumed to be the same as for FTOF (water)?
  - LV, bias V routing to the staves need more work
- I would like to start working *towards* a prototype BTOF RDO (& Power Board?)
  - even if we don’t have all the answers
    - possibly target ETROC as an existing ASIC since same ASIC designers are working on FCFD so digital backend likely similar? Needs discussion with FCFD ASIC designers (as always).
  - goal is to submit a PED in Sep/Oct/Nov (thoughts?)
  - groups/people involved?