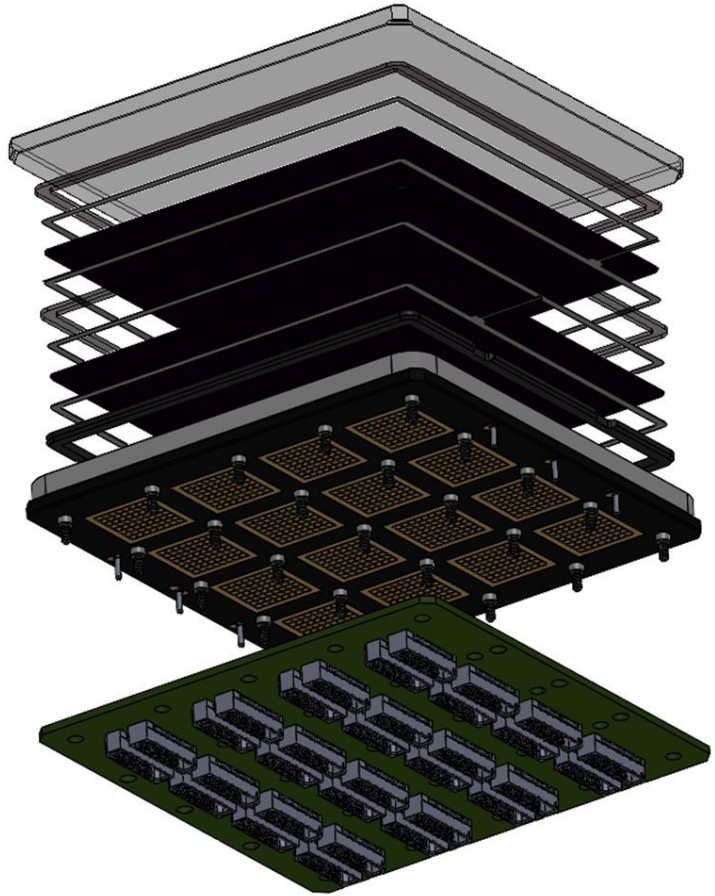
HRPPDs for ePIC Cherenkov PID

Alexander Kiselev (BNL)

ePIC TIC Meeting, May 13, 2024

Production & testing status

- Six out of seven ordered EIC HRPPDs produced and shipped to JLab
  - One is at BNL already
- All tiles come with an extensive internal test report
  - Confirm a compliance with the requested specs
  - High QE, high gain (if needed), low DCR
- Primary QA procedure is ongoing at JLab
  - Mechanical & electrical interface [issues, see next slides]
  - Pad connectivity [OK]
  - Pulse shape, timing resolution, DCR [all OK]
- First results are coming from BNL
  - Single photon timing looks very promising



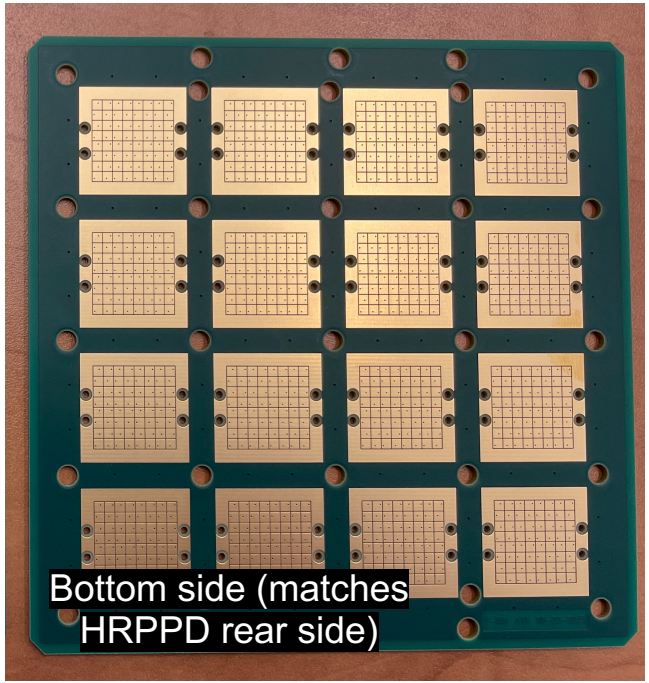
EIC HRPPD evaluation procedure

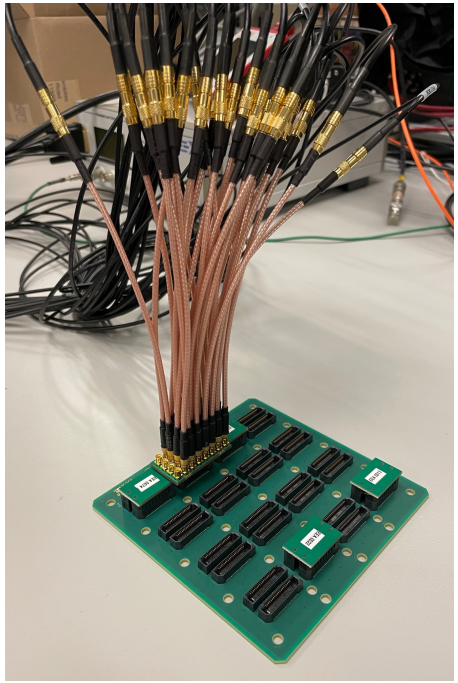
- Primary QA at JLab
- More systematic active area scans (including ps timing) at BNL

- Magnetic field resilience studies at Argonne in late summer 2024
  - *Parasitic to MCP-PMT evaluation*
  - Staffed by Argonne, BNL, JLab, USC
  - Main objective: gain and timing performance recovery in a “typical” pfRICH and hpDIRC B-field

- Photocathode ageing studies by INFN
- Side by side Photek Auratek, Photonis Planacon & Incom HRPPD comparison in Glasgow
- Work on HRPPD HGCROC3 ASIC backplane (Debrecen / Brookhaven)
- Setting up a Brookhaven test stand clone at Yale

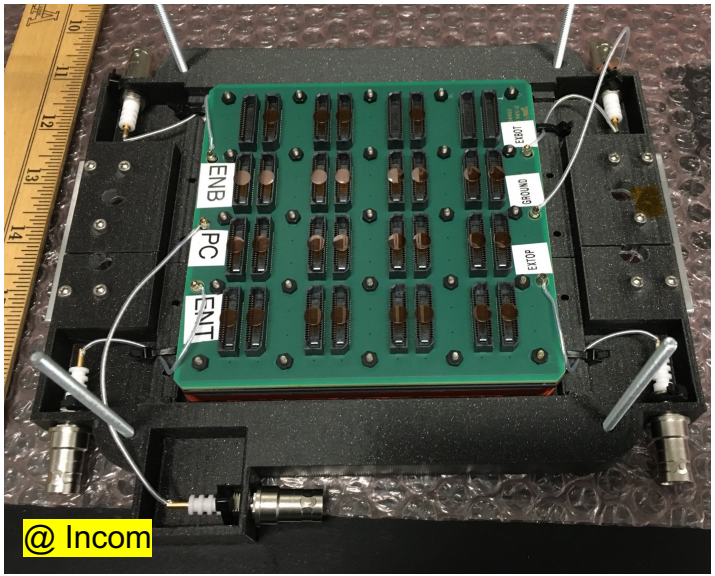
HRPPD passive interface

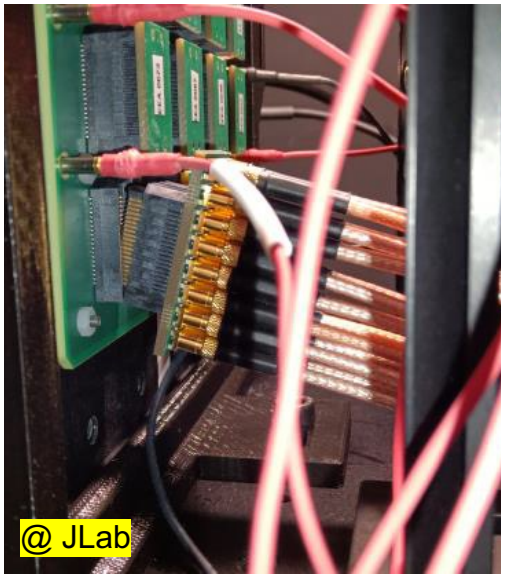


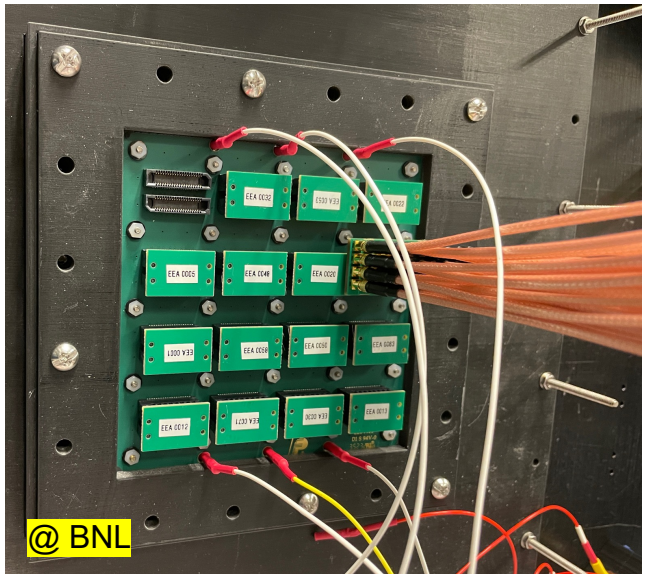


- For installations with a low electronics channel count
- Samtec -> MMCX adapter; MMCX -> MCX pigtail cables, grounding caps

HRPPD passive interface

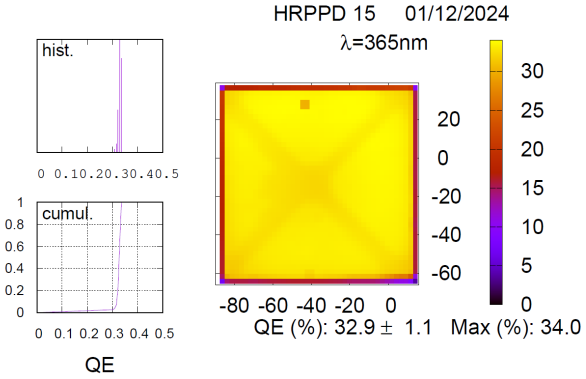


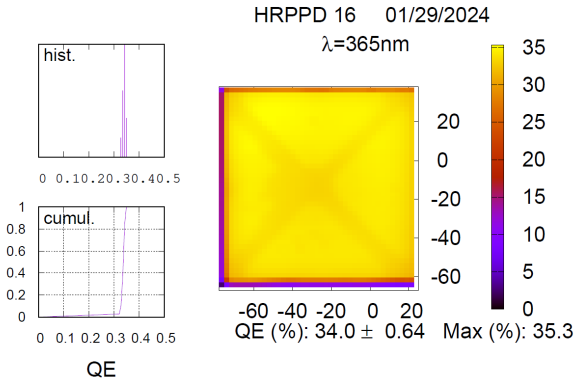


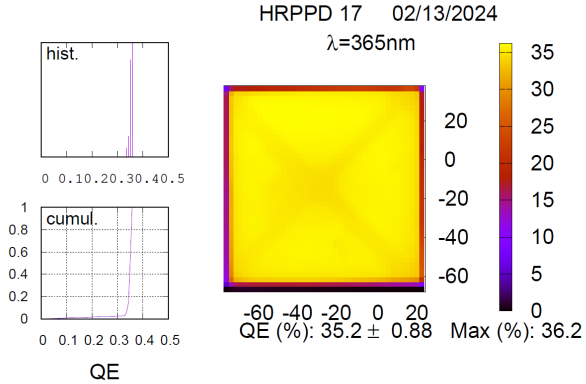


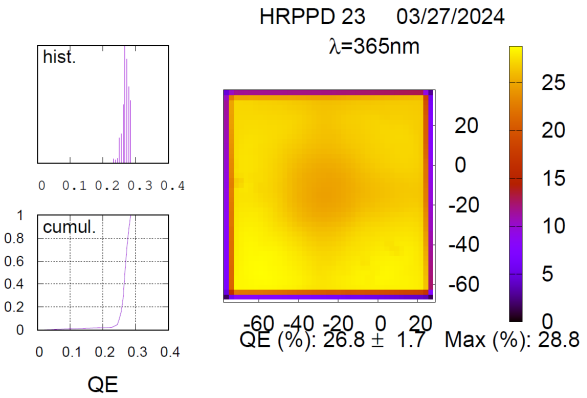
- Universally used at all three presently functional test stations
  - Together with the compression interposers, spacer, [3D printed enclosure]
- Functionally equivalent (?) to a Photek Auratek backplane

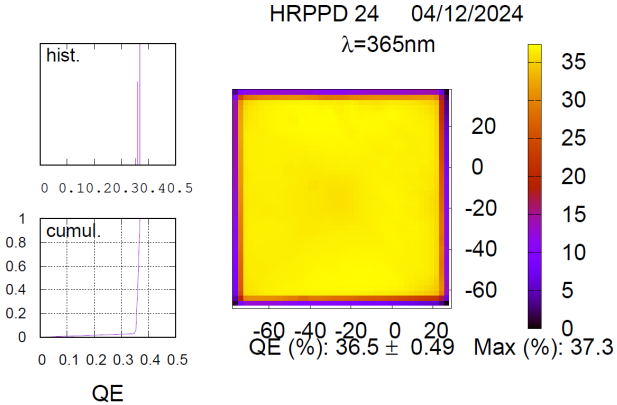
Highlights from Incom's internal testing: QE









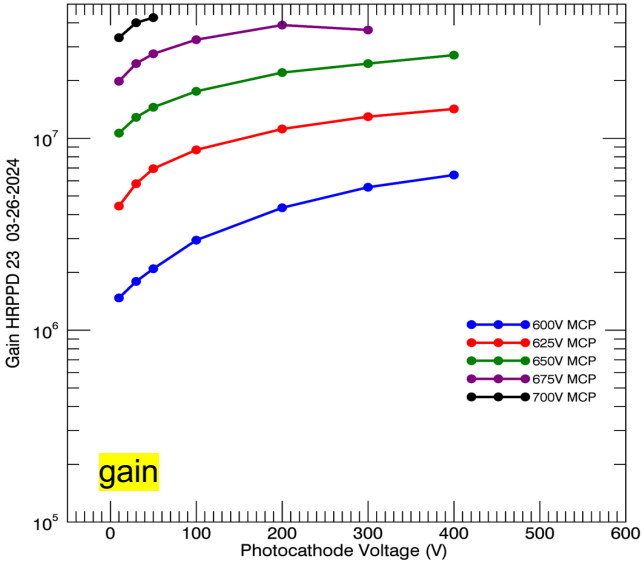


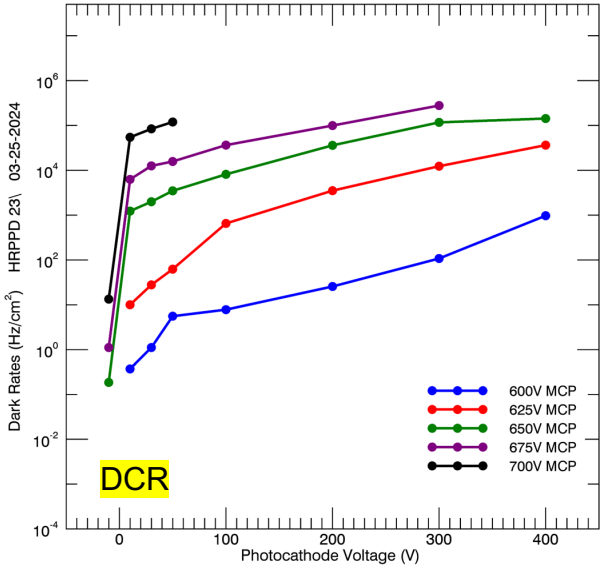
- Typically, well above 30%
  - We require: 27% min, >30% avg
- Uniformity better than expected
- Issues with a fraction of produced tiles are understood

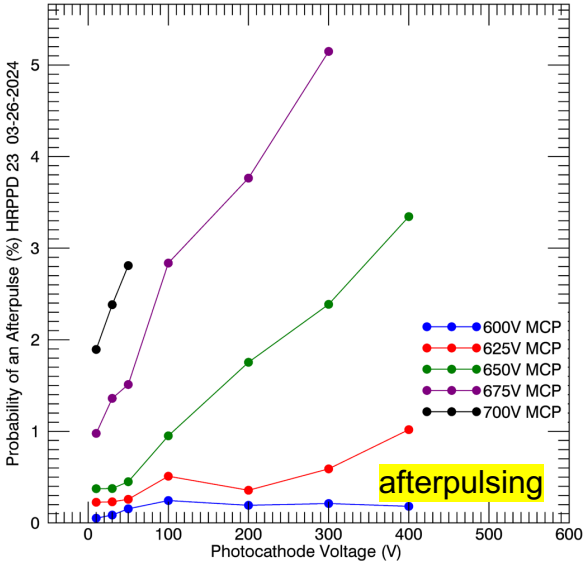
[Link to a May 8th LAPPD / HRPPD Workshop talk]

by Mark Popecki (Incom)

Highlights from Incom's internal testing: DCR & gain







- Newly developed ALD process allows for a high gain at a remarkably low bias voltage
  - HRPPD #23: dark rates at mid-10^6 gain are below 1 kHz/cm^2 with afterpulsing on a ~1% level
- *Gain uniformity yet to be confirmed, especially towards the acceptance edges*

by Mark Popecki (Incom)

Highlights from Incom's internal testing: summary

HRPPD #	Operating Voltage Range (V/MCP)	Dark Rates @ 1X10^6 Gain (Hz/cm^2)	EIC Standard – Dark Rates
15	750-850	160	≤ 2E3Hz/cm^2 at ≥ 10^6 Gain
16	625-725	0.18	
17	600-700	19	
18	825-975	3.60	
23	600-700	0.37	
24	575-700	69	

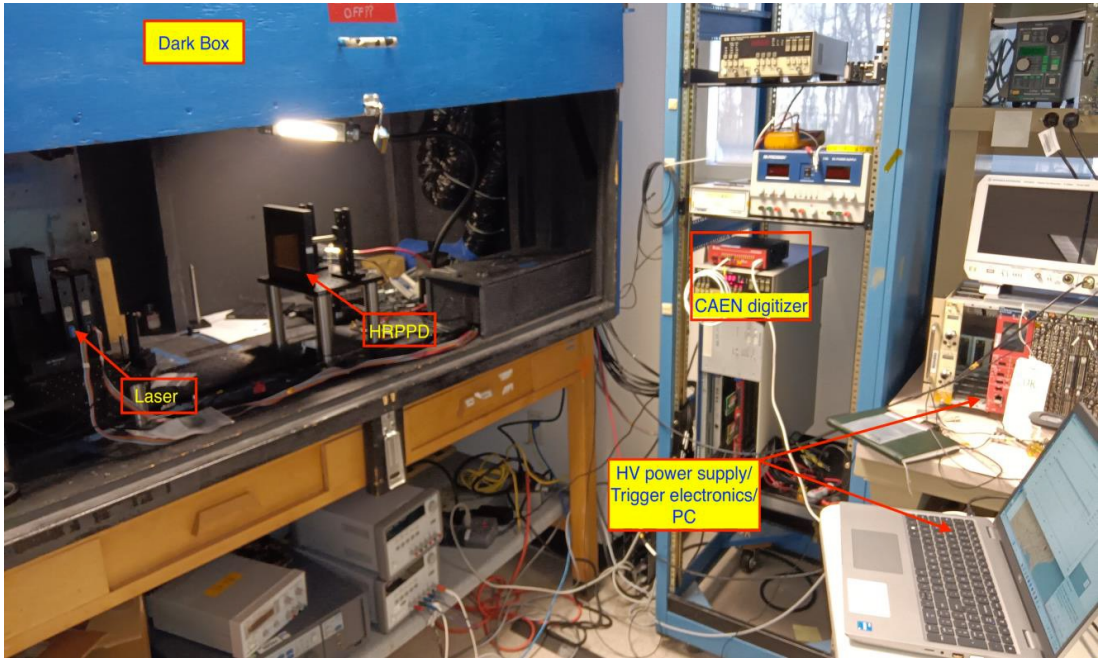
HRPPD #	Transit Time Spread (lowest recorded, in ps)	EIC Standard – TTS
15	59	≤60 ps, validated at BNL utilizing a femtosecond laser
16	59	
17	58	
18	68	
23	58	
24	70	

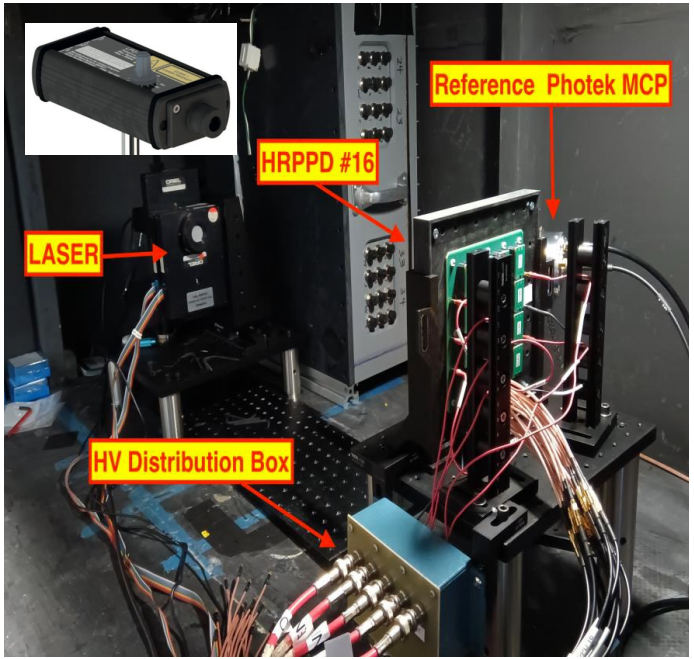
HRPPD #	Operating Voltage Range (V/MCP)	Gain Range at ≥ 100V Bias on Photocathode (PC)
15	750-850	6.5E5 – 1.4E7
16	625-725	9.2E5 – 1.3E7
17	600-700	1.0E6 – 1.8E7
18	825-975	9.6E5 – 1.4E7
23	600-700	2.9E6 – 3.7E7
24	575-700	6.8E5 – 2.2E7

HRPPD #	QE @ 365nm (Avg./Max.)	Std. Dev.
15	32.9%/34%	1.1%
16	34%/35.3%	0.64%
17	35.2%/36.2%	0.88%
23	26.8%/28.8%	1.7%
24	36.5%/37.3%	0.49%

by Mark Popecki (Incom)

Present HRPPD test stand at JLab



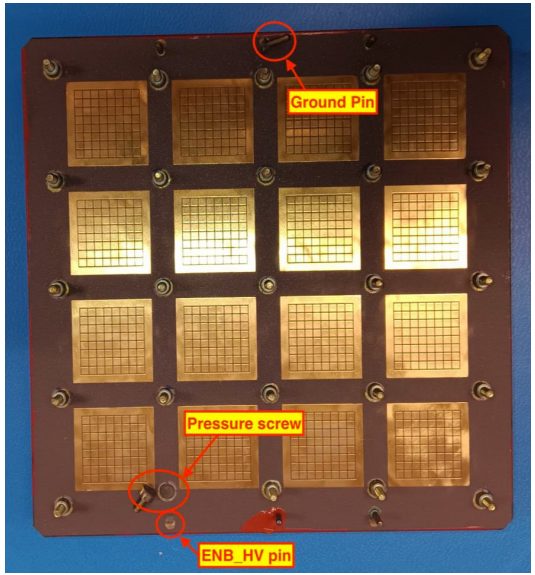


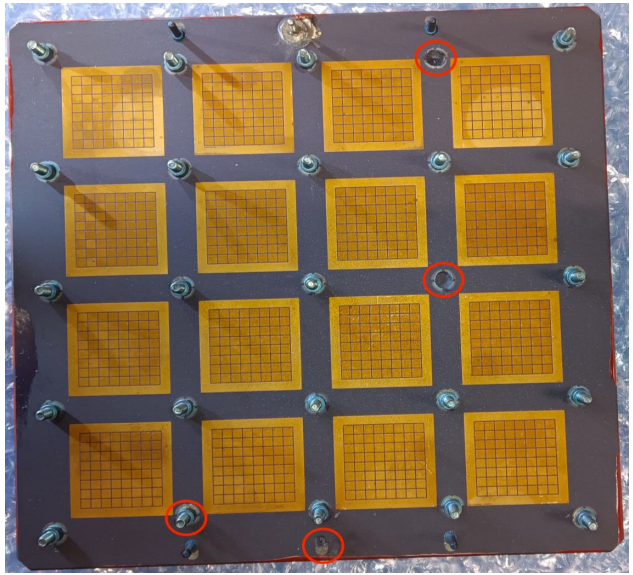
- ARC – Detector Group Lab
  - Large dark box, V1742 digitizer, NIM logic, Tektronix MSO scope, etc
  - Pulsed free space 405 nm laser (~75 ps FWHM) with a diffuser

Link to a May 8th LAPPD / HRPPD Workshop talk

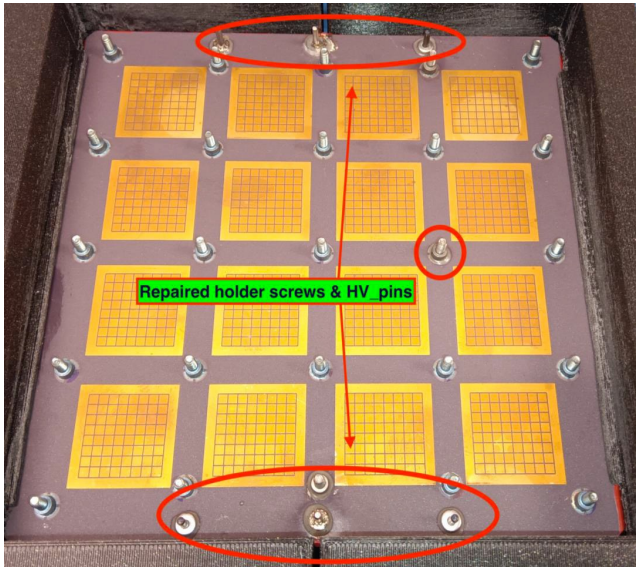
by Arshak Asaturyan (JLab)

Highlights from JLab QA process: screws & HV pins





Examples of failed HV pins and screws

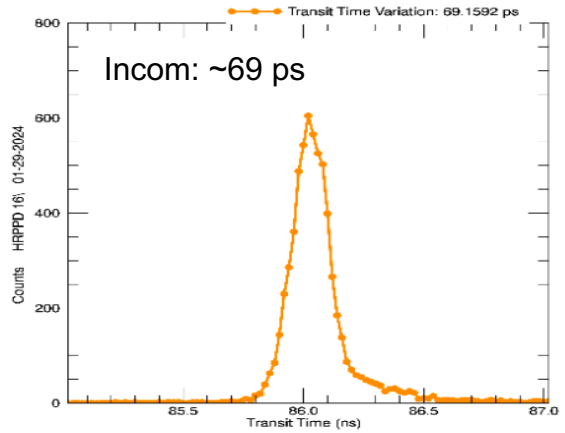


A present fix by Incom

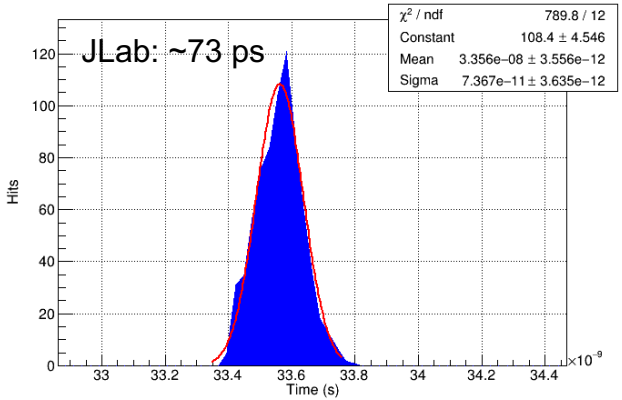
- Several HRPPDs showed issues with falling off HV pins and mechanical screws
  - Those were promptly fixed by Incom
- Solutions for a “final EIC HRPPD design” are being developed
  - Get rid of HV pins (?); embed screws into the ceramic anode body

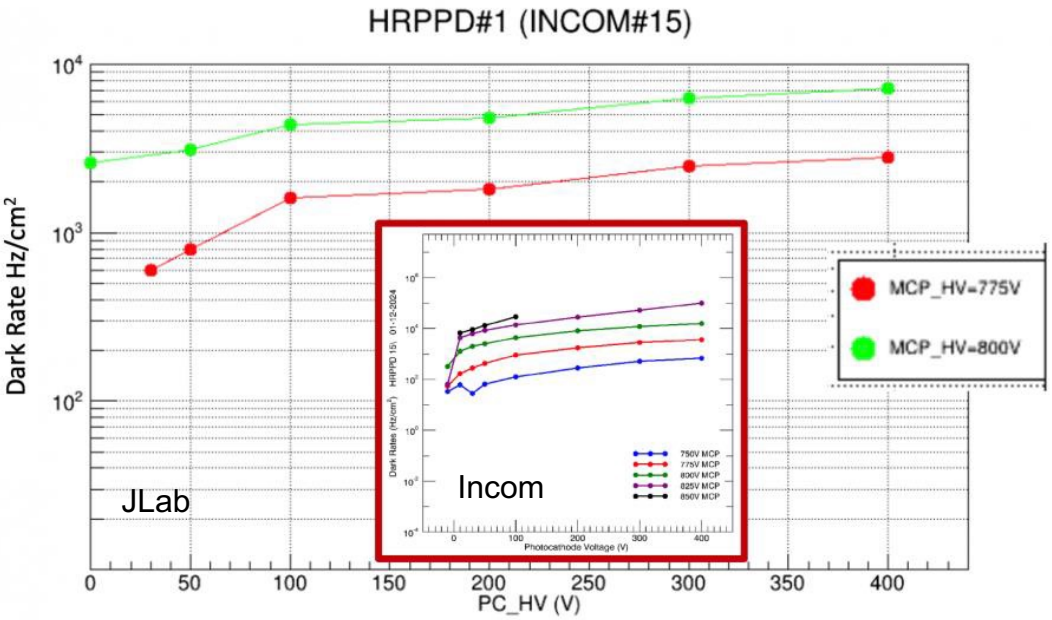
by Arshak Asaturyan (JLab)

Highlights from JLab QA process: DCR & timing



HRPPD #16

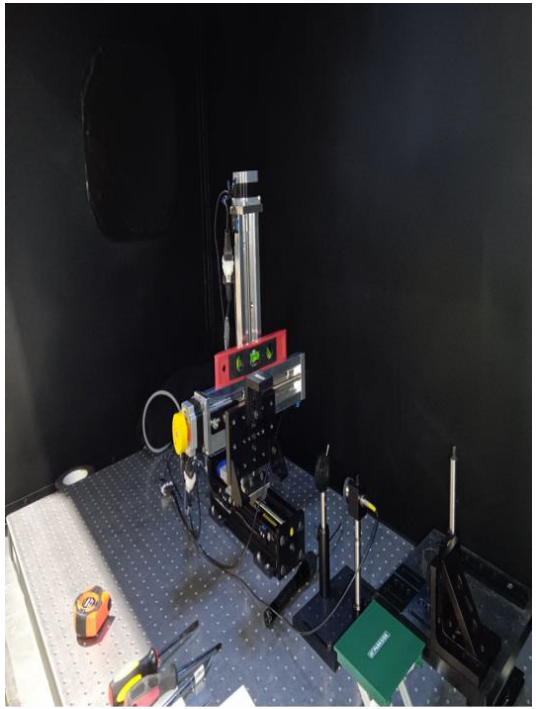




- Timing evaluated using a high-performance scope
- Both TTS ad DCR numbers are consistent with Incom's report

by Arshak Asaturyan (JLab)

New HRPPD QA station at JLab

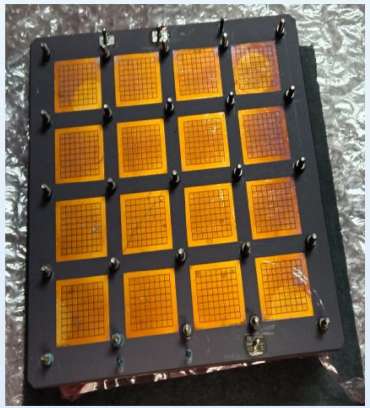


- EEL 108 Mezzanine area
  - Large dark box, multi-channel readout system, motion control, etc
  - Fiber coupled PiLas laser

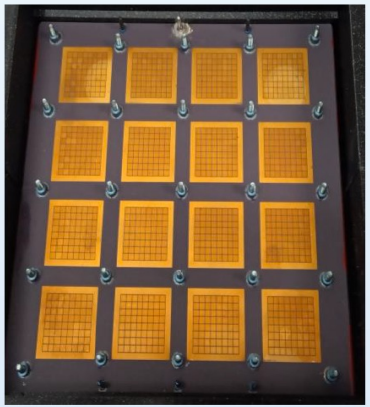
by Arshak Asaturyan (JLab)

Arshak's view on how EIC HRPPDs develop ☺

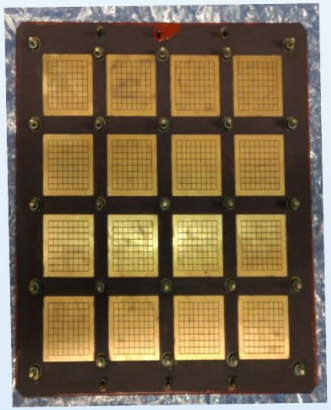
The HRPPD evolution



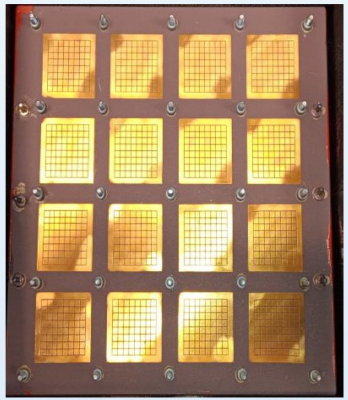
HRPPD#1



HRPPD#2

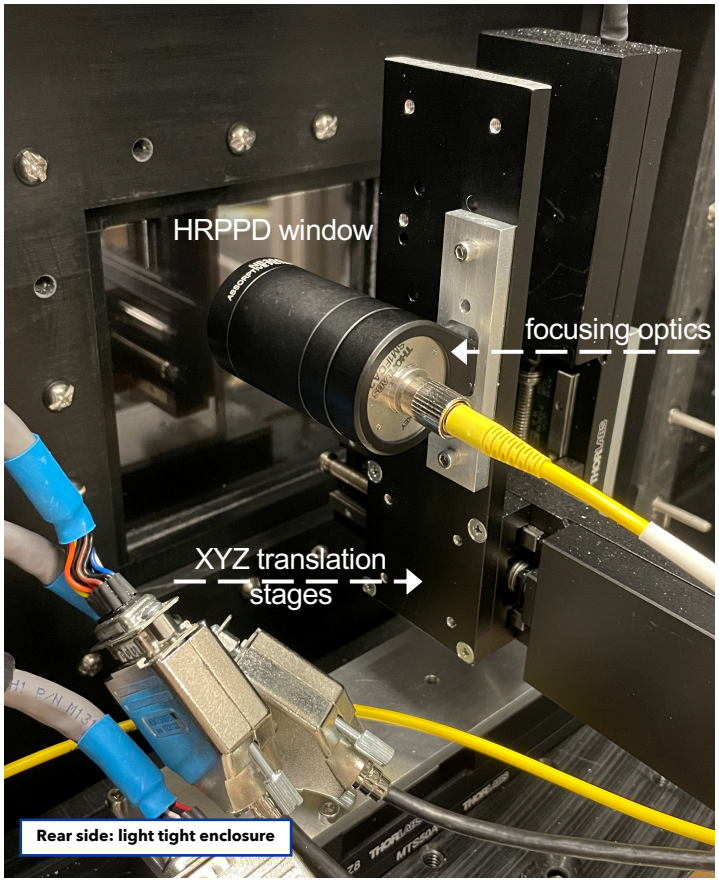


HRPPD#3



HRPPD#4(INCOM #23)

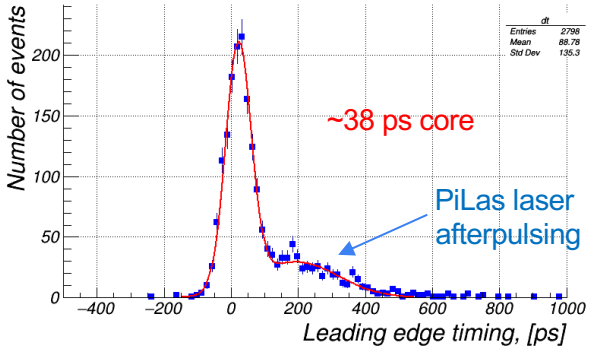
Present HRPPD test stand at BNL



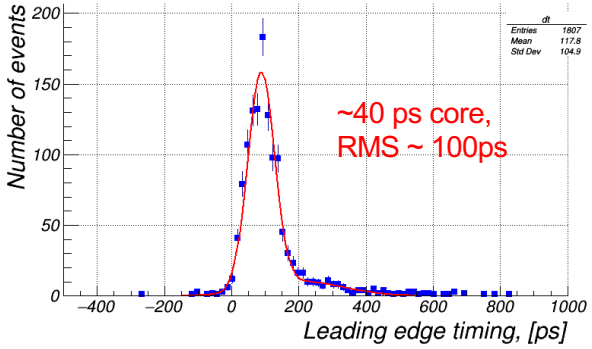
- Picosecond PiLas laser
- Compact light-tight enclosure
- 480 DRS4 channels (V1742 digitizers)
- Interface board with a compression interposer interface
  - MMCX and high-density Samtec connector interface to DRS4

[Link to a May 8th LAPPD / HRPPD Workshop talk]

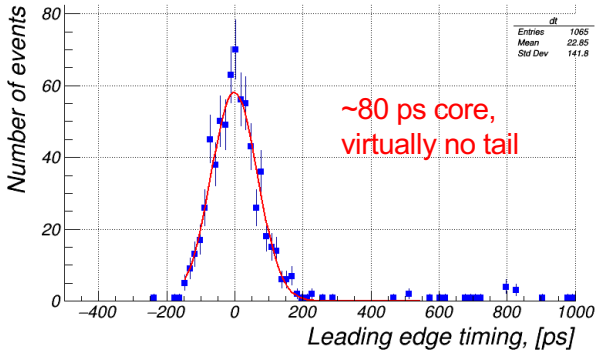
HRPPD #15: timing performance with a 420nm laser



0% laser tune, 200V on photocathode

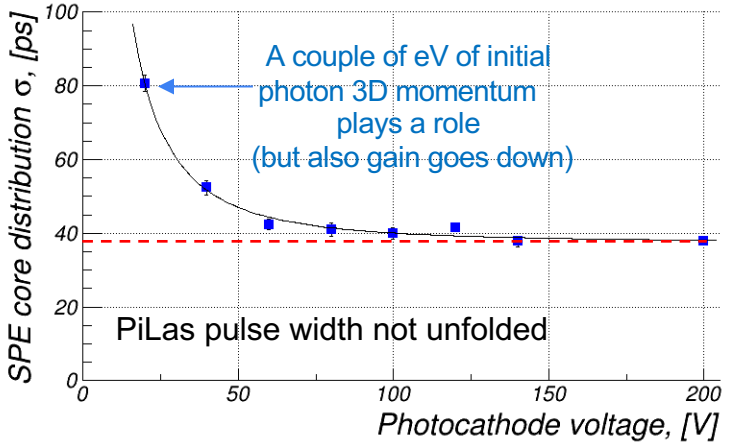


25% laser tune, 200V on photocathode



25% laser tune, 20V on photocathode

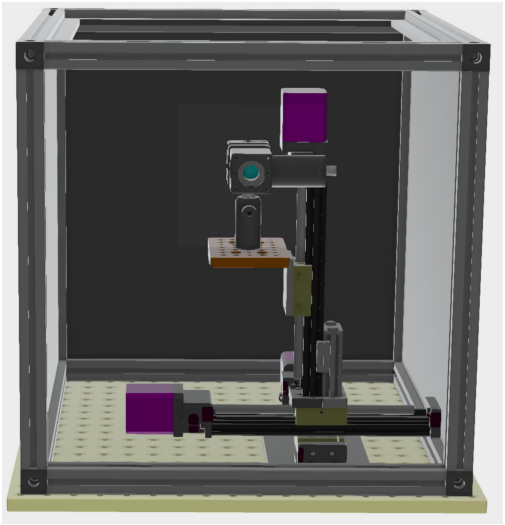
- *PiLas (ps) laser* beam focused on a single pad center
- Intensity tuned down to >99% empty events
- Δt data taken with a V1742 DRS4 module
  - Channel #0 – HRPPD pulse
  - Channel #1 – laser synchro pulse

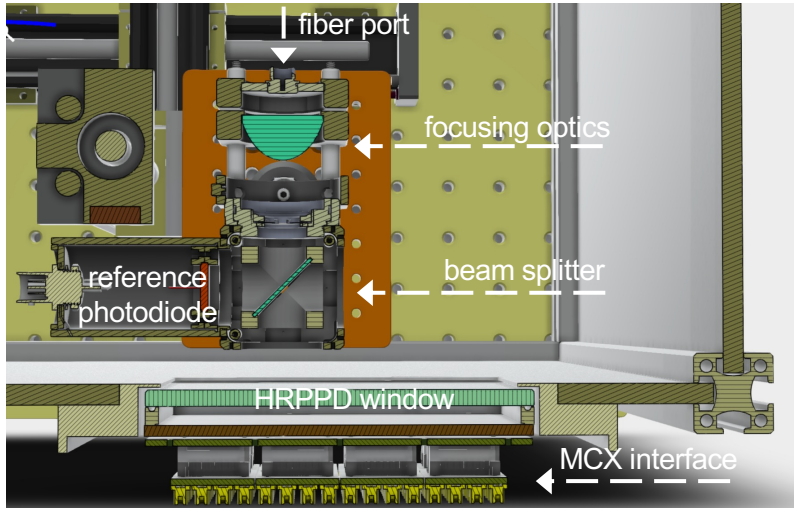


- *First data with Elmo (fs) laser look even more promising*

HRPPD QA station upgrade at BNL

- Consolidate all HRPPD equipment in a new lab space
  - A new dark box with 6” Velmex translation stages & a 256ch MCX interface
  - [PiLas (picosecond)] and Elmo (femtosecond) lasers
  - Oriel 77250 monochromator
  - DAQ PC, NIM & VME crates, 8x V1742s
- Re-use the original setup on a new HGCROC backplane test bench





ASIC considerations

- **A standard requirement list**
  - Provide timing resolution <20ps and amplitude measurement
  - Work with collected charge from few dozens to few hundred fC
  - Work with a relatively high detector capacitance up to 10 pF
  - Have high channel density (64 channels per ASIC and more) and few mW/ch power dissipation
  - Streaming mode (either this or that way)

Waveform digitizer (e.g. by Nalu Scientific)

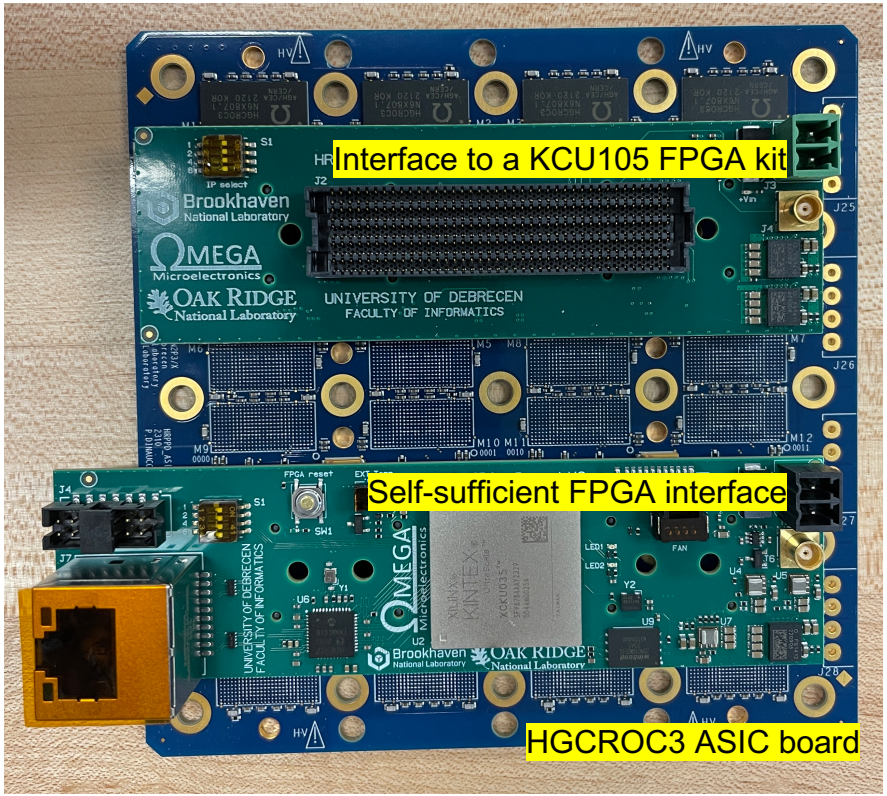
- Pros
  - Expect higher timing resolution overall
  - Performance less affected by signal shape
- Cons
  - Higher expected power dissipation
  - Not readily available with a high enough channel count

TOA/ADC (EICROC by OMEGA group)

- Pros
  - Supported by the EIC project
  - HGCROC3 is available as a starting point
  - Expected power dissipation ~1-3mW/ch
  - Should work with HRPPDs at a lower gain
- Cons
  - Assumes signals have a “regular” shape

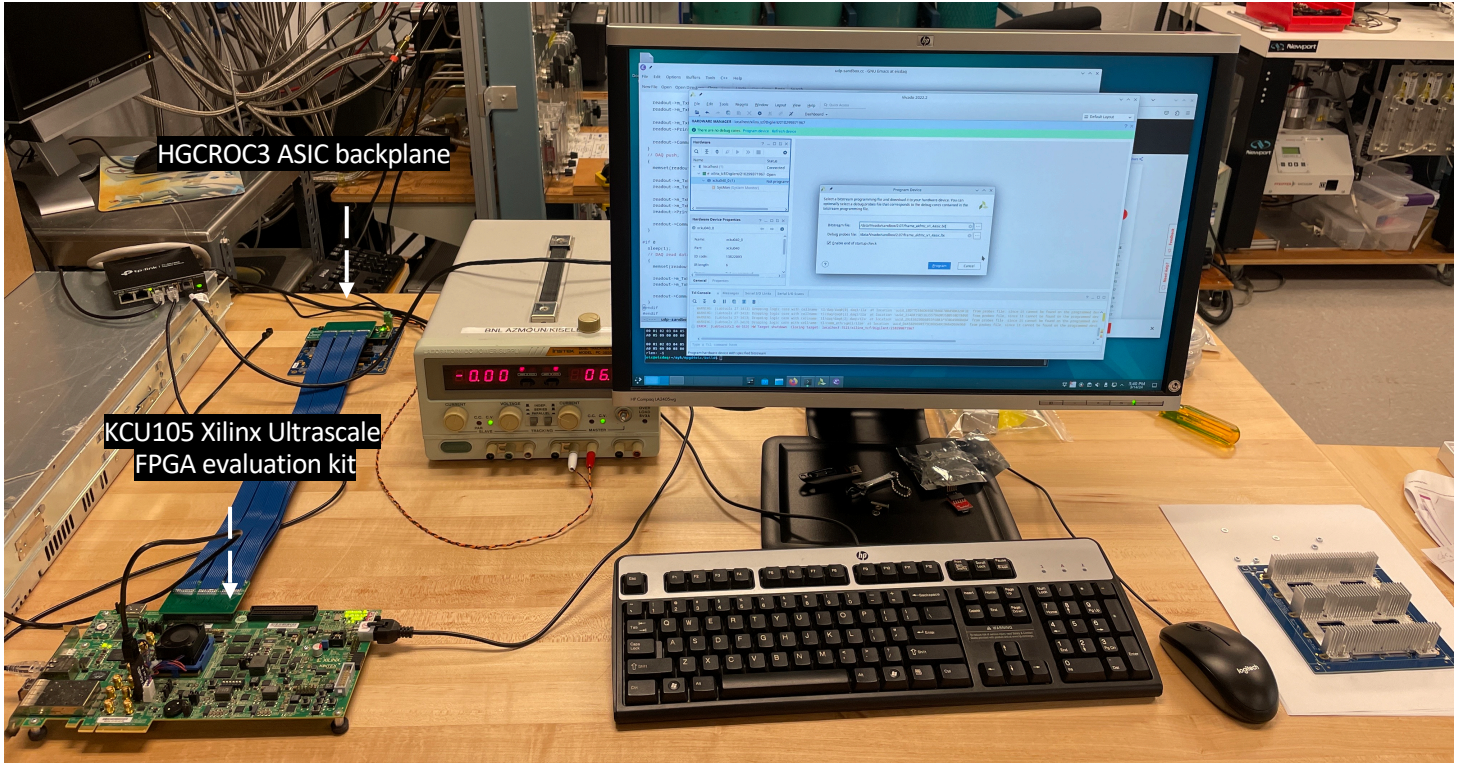
HRPPD HGCROC3 ASIC / FPGA backplane

IN2P3 [OMEGA], Uni Debrecen, BNL, Oak Ridge



- V0 iteration is ~complete
  - Four partly staffed ASIC boards
  - Few passive interface boards (for use with a KCU105 kit)
  - One FPGA board
  - Cooling stuff (heat sinks, fans) for five HRPPDs
- Passive interface debugging takes more time
  - Host PC -> FPGA -> ASIC connectivity is established
- Current effort & next steps:
  - Debug the driver using FMC+KCU105 configuration
  - **Make sure HRPPDs work with this analog frontend**
  - Verify that FPGA-based implementation works
  - Proceed with ordering V1 backplane sets for 5-7 HRPPDs

HRPPD ASIC backplane test stand at BNL



- Presently based on a non-FPGA version of the interface board
- **Will be complemented by its own HRPPD test stand clone shortly**

Summary & outlook

- An EIC PED contract to re-design HRPPDs and procure a small batch is pretty much complete
- 5+2 HRPPDs were ordered and sis of them delivered to JLab already
  - The extra two are for hpDIRC evaluation

- Evaluation effort is ramping up in several EIC institutions around the world
- Work on ASIC backplane is in progress

- Further plans will depend on the evaluation outcome by the end of summer 2024