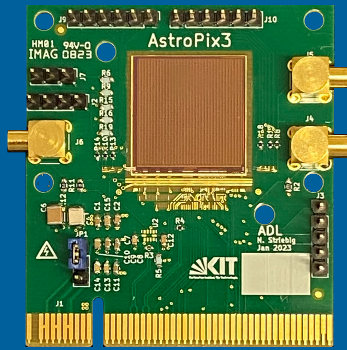
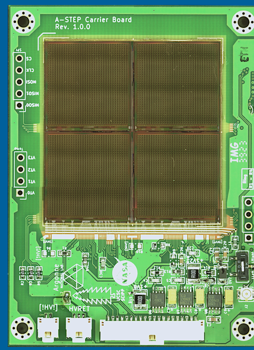
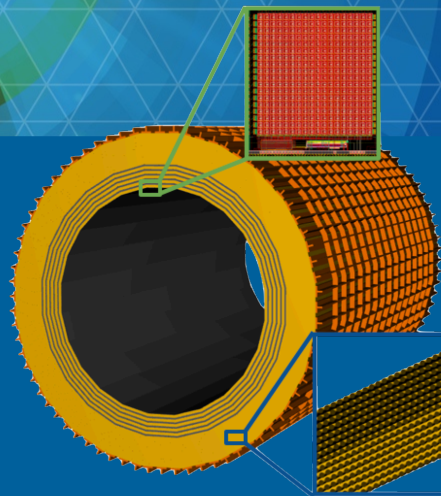
ePIC TIC Meeting

AstroPix







Manoj Jadhav
Argonne National Laboratory

May 20, 2024

ePIC

Argonne
NATIONAL LABORATORY

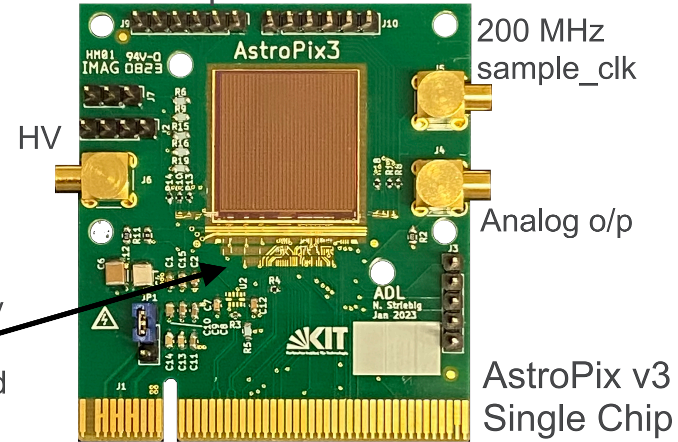
AstroPix Status - v3

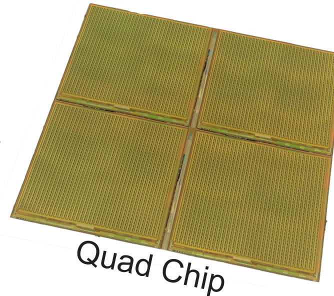
AstroPix v3

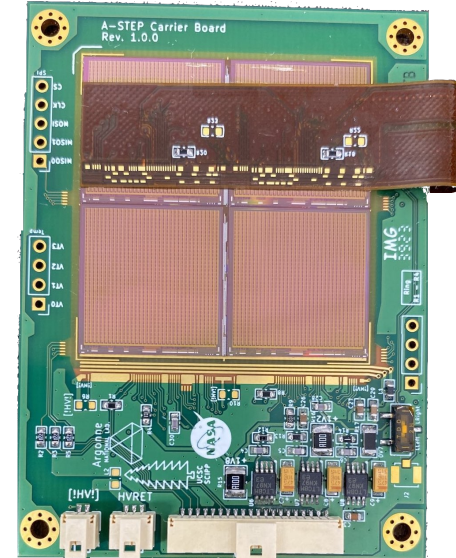
- 2 × 2 cm^2 full-size chip with 35 × 35 pixel matrix
- 10-byte data frame per hit
- Currently under test - Characterization (signal, depletion, test beam)

AstroPix v3 Quad-chip

- 2 × 2 daisy-chained array
- Ongoing testing with the bottom two chips
- FW/SW development
- Analog and Digital signal
- Respin of the board with few modification
- Application in NASA ComPair2 Project - Tray prototype (20 × 20 chips) - June 2024



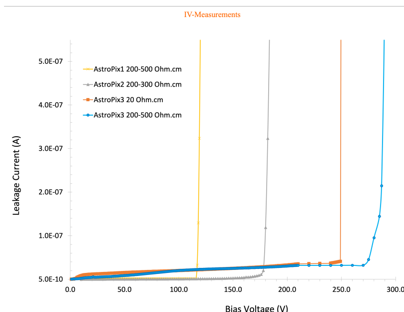




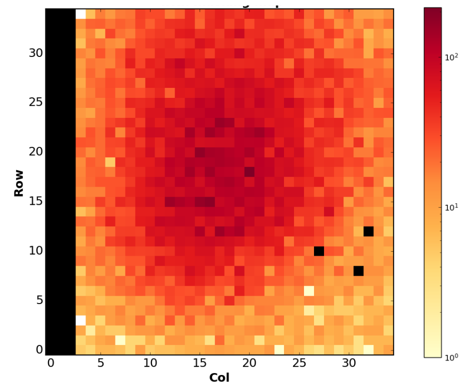
AstroPix v3

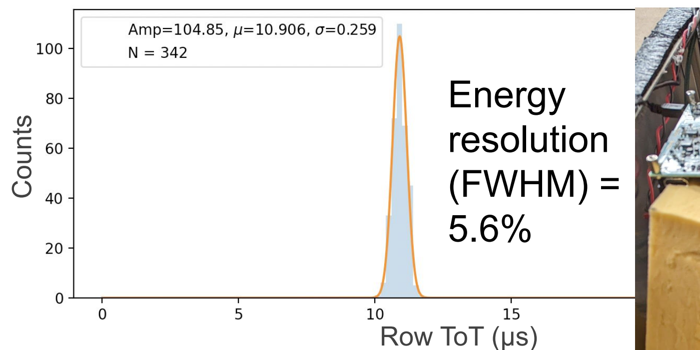
Ongoing Characterization - Test bench

- IV-CV measurements
- The energy resolution of 5.6% is measured using an injected pulse
- Source Scans for energy calibration
- TCT measurements for depletion depth measurements
- Test beam 2023 - 120 GeV proton

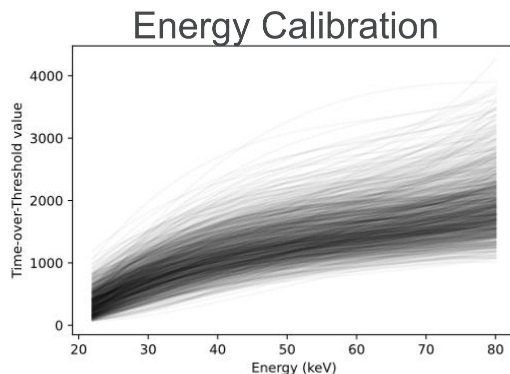


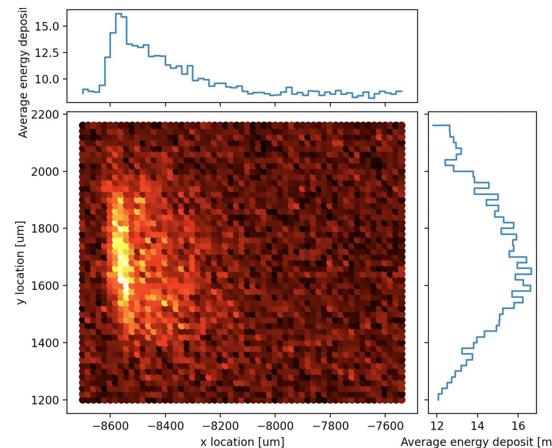
Test beam 2023





Energy Calibration





TCT measurements at UCSC

AstroPix Status - v4

AstroPix v4: The final design version with Multi-Project Wafer run

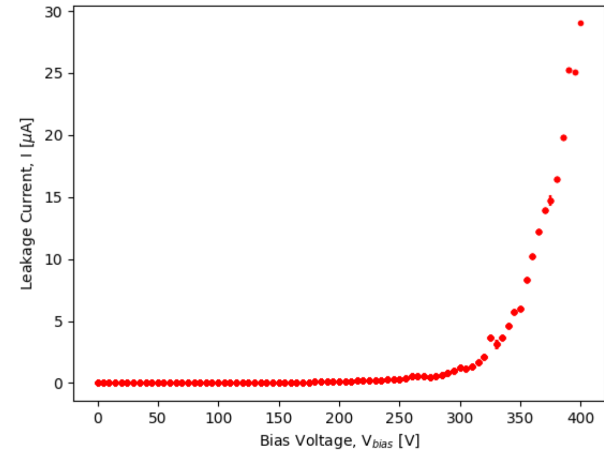
- Chip size 1 $\times$ 1 cm^2; Thickness 700 μm, V_{BD} ~ 400V
- Wafer resistivity available - 200-400 Ω.cm and 25k Ω.cm
- Pixel pitch 500 μm with pixel size 300 μm
  - 13 $\times$ 16 pixel matrix
- Individual pixel readout with individual hit buffer
  - No identification issue due to ghost hits
- 3 Timestamps - 2.5MHz (TS), 20 MHz (Fine TS), and 16-bit Flash TDC
- Individual pixel TuneDACs
  - Pixel-by-pixel threshold tuning and pixel masking
- Additional bits for ToT measurements to avoid bit wrapping observed in v3 chip

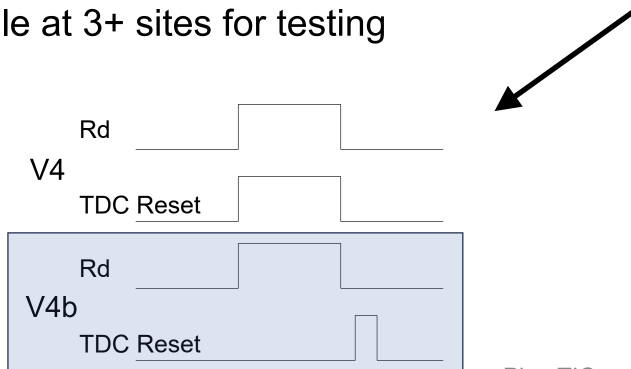
AstroPix Status - v4

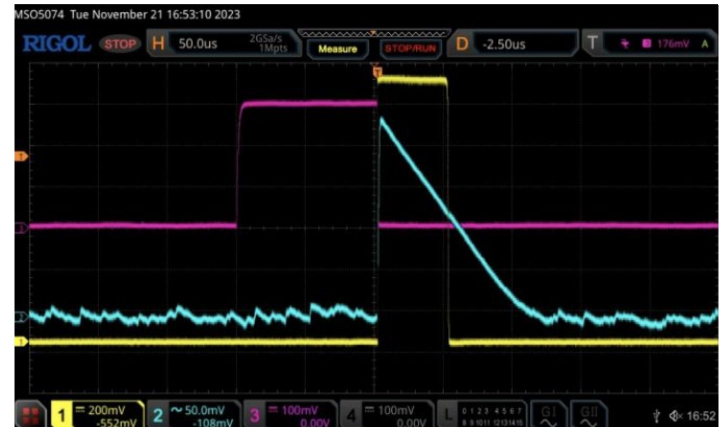
AstroPix v4: Initial validation tests

- FW/SW updated for operation
- Additional bits for ToT measurements
  - 20 µs in v3 changed to up to msec in v4
- Power Consumption - 4 times reduction
  - ~1 mW/cm^2 analog and 3 mW/chip Digital
- PLL clock generation
- On-chip injection configuration
- Flash-TDC is resetting with read clock (fixed in v5)
- Available at 3+ sites for testing

KIT
Karlsruhe Institute of Technology



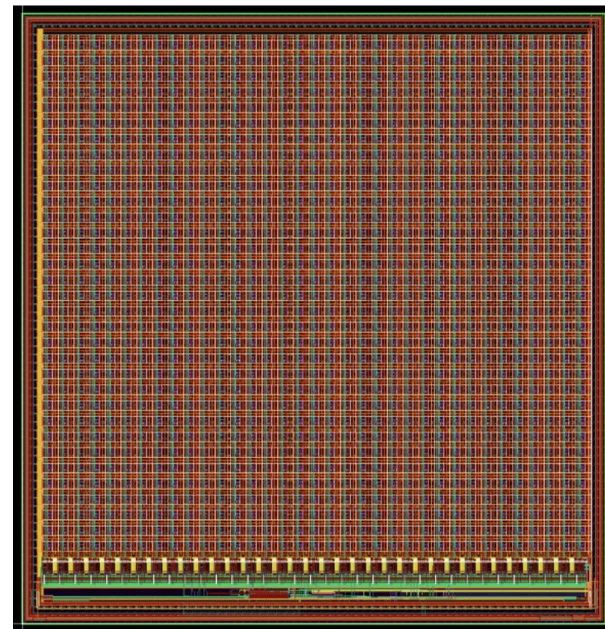




AstroPix Status

AstroPix v5 : Full size design

- No major design changes
- Fix any bug from v4
  - Flash-TDC and SPI noise
- V3 size chip - ~2 × 2 cm²
- Pixel pitch 500 μm,
- 33 × 35 pixel matrix with individual hit buffers
- Wafer resistivity 200-400 Ω.cm and 700-2k Ω.cm
- Integrated voltage register for all needed input power lines
- Improved interrupt and readback config via SPI
- Design review on 29 May 2024
  - First fabrication with new foundry - AMS
  - Submission planned for mid-June 2024
  - Expecting v5 chips in Nov 2024

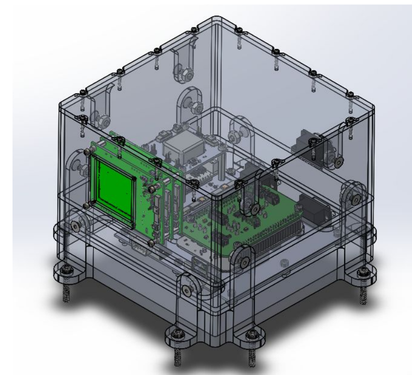


Detailed presentation link here

NASA Payloads

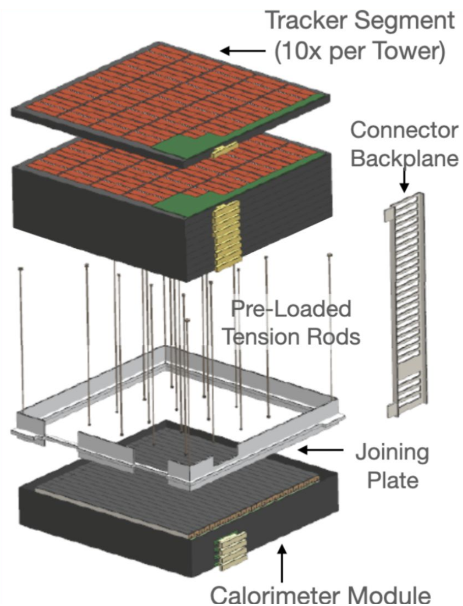
A-STEP - v3 (Ready for testing)

- Sounding Rocket Flight 2025
- 3 quad-chip layers (12 chip arrays, 3 SPI channels)
- Benchmarking AstroPix system development
- Scaled FW/SW and I&T Structure
- Develop selection/test/calibration strategies



ComPair2 - v3 first layer (June 2024), v5 all layers (2025)

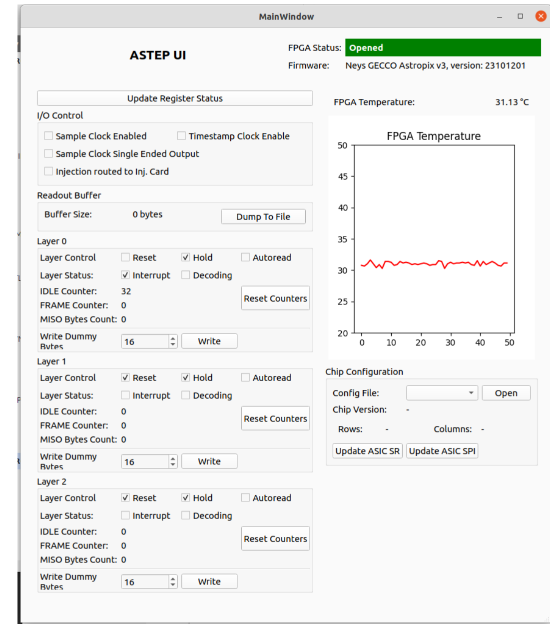
- AMEGO-X prototype - Gamma-ray beam 2026
- 10 layers, 96 quad-chips per layer (3840 chip arrays, 20 SPI channels)
- Mechanical Structures, I&T Readiness
- Develop selection/test/calibration strategies



FW-SW Development for Quad Chip layers

New FW for quad-chip layers

- FW-driven SPI readout to reduce deadtime
  - The self-trigger readout when there is data in buffers without SW check
  - Sensor data frame detection, IDLE discard, Tagging/ reframing, routing to single Readout Buffer
- FW Scale-ability
  - Read through the daisy chain in FW rather than SW
  - Up to 20 daisy-chained SPI inputs have their own interfaces, which feed into the global buffer
- SW speedup to match FW
  - Reduce the chance of incomplete data return
  - Speed-up in analysis scripts, esp. when probing every pixel individually



https://github.com/AstroPix/astep-fw

Test Beam - new schedule 12 June 2024

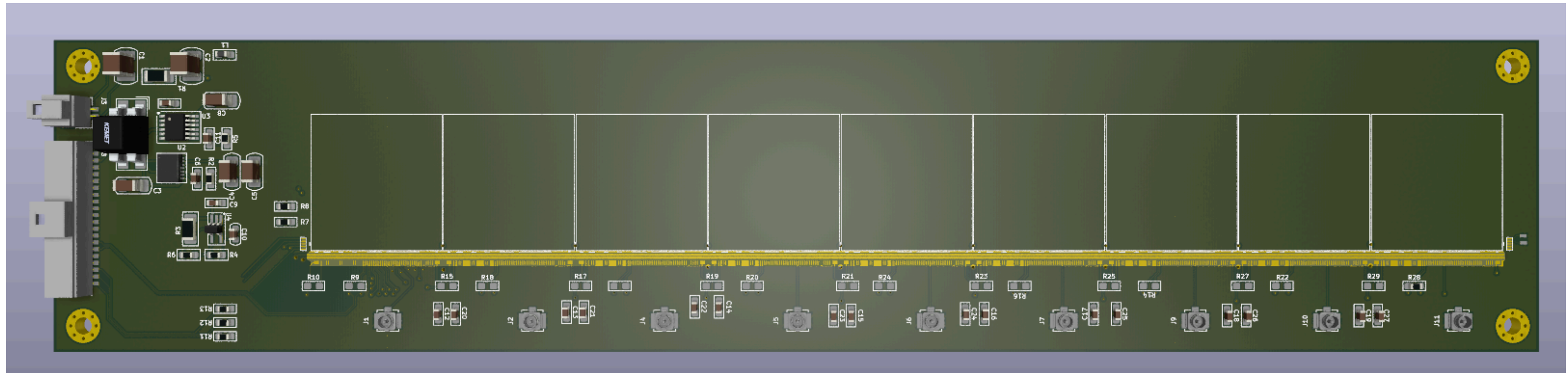
- BIC prototype calorimeter behind existing Argonne ATLAS Pixel telescope with AstroPix setup. at MTest
- Rotating stage to simulate particles incident at angles up to 45° $(\eta{\sim}1)$
- 3 Layers of AstroPix for Tracking efficiency
- Ability to lower BIC setup out of the beam, no need to uninstall for other experiments to run
  - Proximity to Argonne enables occasional opportunistic running

ANL AstroPix Telescope Setup

BIC Setup!

AstroPix Module

- 9 chip Module PCB test structure
- Full readout electronics
- 2 LDOs to regulate Low Voltage
- Data using 20 pin connector

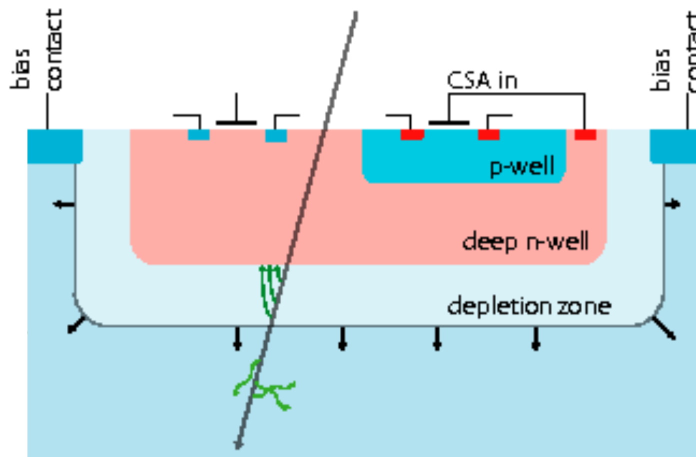


Thank you

AstroPix

HV-CMOS Monolithic Active Pixel Sensor (MAPS):

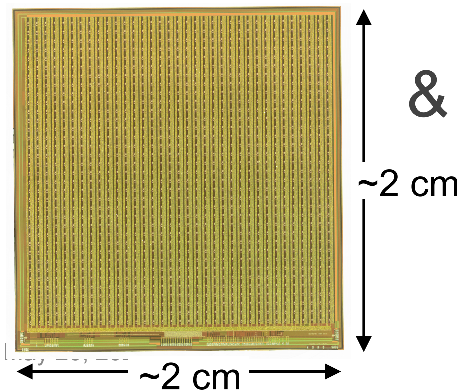
- Combination of silicon pixel and front-end ASIC
- On-pixel charge amplification and digitization
- The technology uses more typical CMOS wafer processing for cost-effective mass production
- Fabrication on a single wafer enables a shorter design cycle
- No need to bump-bond to each pixel - improves yield

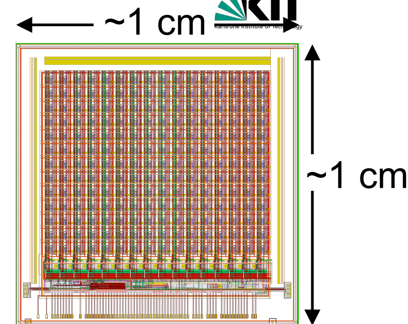


AstroPix (based on **ATLASPix3** **arXiv:2109.13409**)

- 180 nm HV-CMOS MAPS sensor
  designed at KIT (also designed ATLASPix, MuPix, etc.)
- Developed for AMEGO-X GSFC/NASA mission
  (Upgrade to the Fermi's LAT)

AstroPix v3 (Under test)

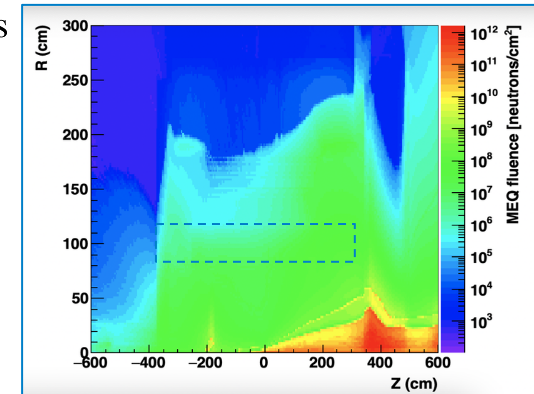




AstroPix v4 (Ready to test, Nicolas' Talk)

AstroPix v3 Iradiation

- IV and CV measurements performed for the v2/v3 chips before irradiations
    - Same measurements will be repeated post irradiation
- 9 v2 & 6 v3 chips irradiated for Passive Irradiation (Al-foil dosimetry)
- Active Irradiation for Latch-up (and SEE) is planned - week of 26th May

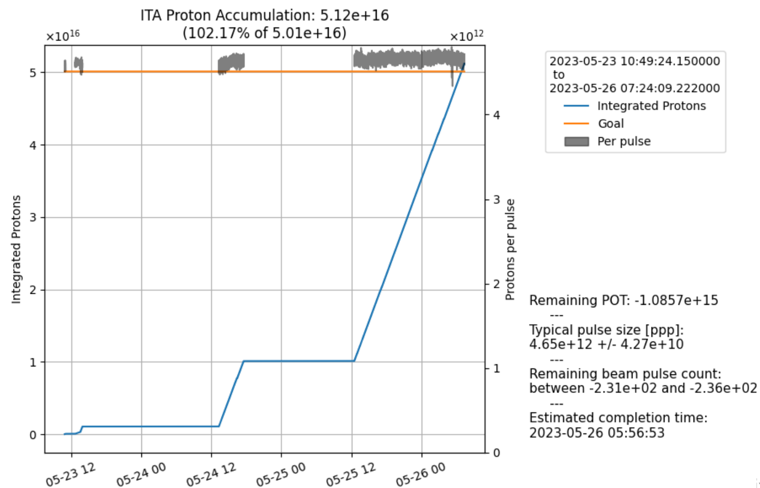


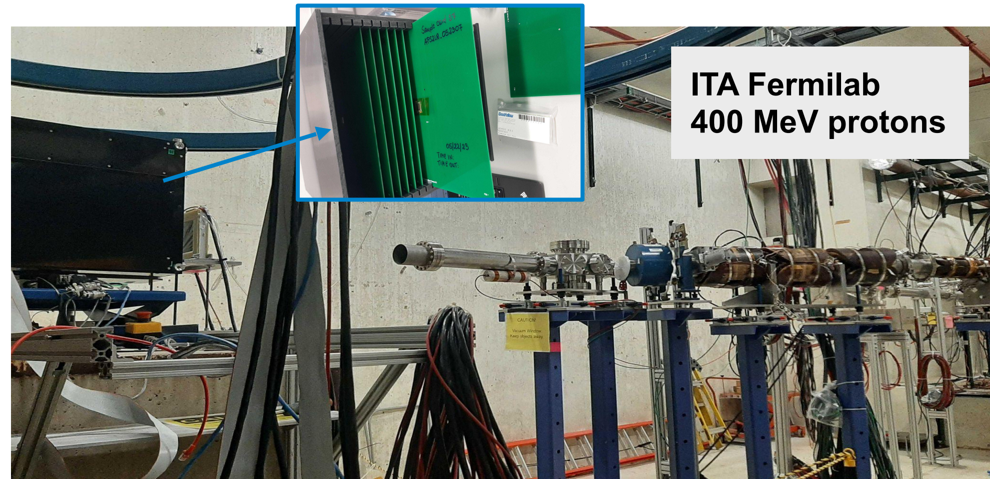
V2 Irradiation

Nb of samples	Doses (400 MeV protons)
3	4.50E+13
3	1.08E+15
2	1.01E+16
1	5.02E+16

V3 Irradiation (low and high ResChips)

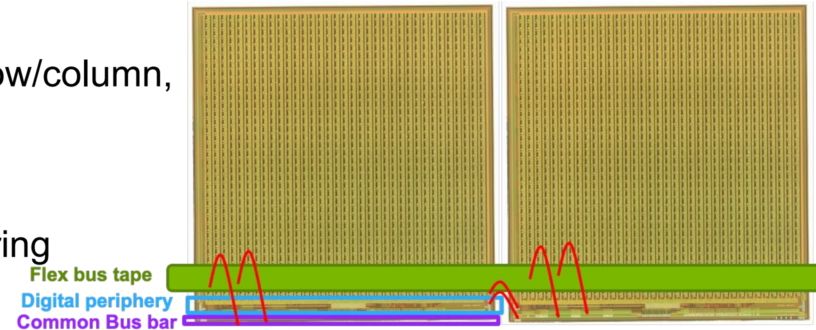
Nb of samples	Doses (400 MeV protons)
2	4.50E+13
1	5.04E+15

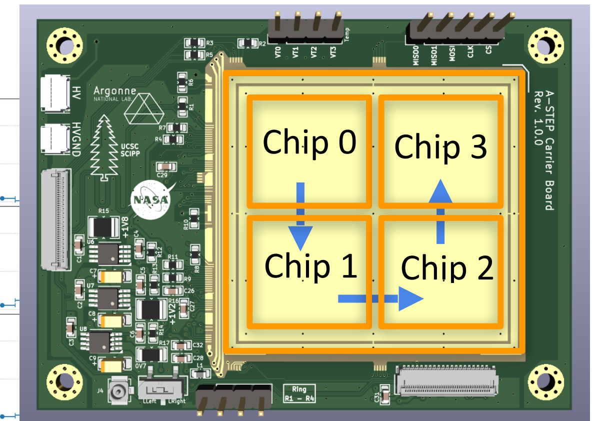




AstroPix Readout

- 10 bytes of data per hit - header (chipID, payload), row/column, timestamp, ToT
- SPI I/O daisy chained - chip-to-chip signal transfer
  - signals are digitized and routed out to the neighboring chip using 5 SPI lines via wire bond
- Power/Logic I/O distribution on the module (through a bus tape)
  - 4 power lines (LV, HV), ~20 Logic I/O (SPI, clk, timestamp, interrupt, digital Injection, etc.)
  - HV, VDDA/VDDD(1.8V), VSSA(1.2V), Vminuspix(0.7V)
  - power distribution can be controlled using voltage regulators
  - mostly part of the end of the stave services
- Data will be received by FPGA at the end of the stave
  - FPGA aggregates data before sending off-detector
- Low heat load at chip, only cooling of end of the stave card
- The operational temperature for AstroPix is at room temperature and considered to be operated at 22 °C





AstroPix v3 quad-chip carrier board
- Demonstrate required services
- Daisy chaining